



September 2000

QFET™

FQD2N80 / FQU2N80

800V N-Channel MOSFET

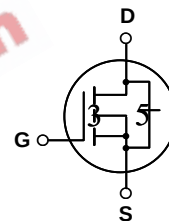
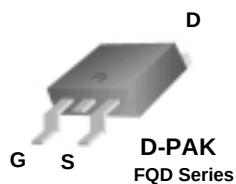
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

Features

- 1.8A, 800V, $R_{DS(on)} = 6.3\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 12 nC)
- Low C_{rss} (typical 5.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD2N80 / FQU2N80	Units
V_{DSS}	Drain-Source Voltage	800	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	1.8	A
		1.14	A
I_{DM}	Drain Current - Pulsed (Note 1)	7.2	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	180	mJ
I_{AR}	Avalanche Current (Note 1)	1.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	50	W
	- Derate above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	800	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.9	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V	--	--	10	μA
		V _{DS} = 640 V, T _C = 125°C	--	--	100	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.9 A	--	4.9	6.3	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 0.9 A (Note 4)	--	2.4	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	425	550	pF
C _{oss}	Output Capacitance		--	45	60	pF
C _{rss}	Reverse Transfer Capacitance		--	5.5	7.0	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 2.4 A, R _G = 25 Ω (Note 4, 5)	--	12	35	ns
t _r	Turn-On Rise Time		--	30	70	ns
t _{d(off)}	Turn-Off Delay Time		--	25	60	ns
t _f	Turn-Off Fall Time		--	28	65	ns
Q _g	Total Gate Charge	V _{DS} = 640 V, I _D = 2.4 A, V _{GS} = 10 V (Note 4, 5)	--	12	15	nC
Q _{gs}	Gate-Source Charge		--	2.6	--	nC
Q _{gd}	Gate-Drain Charge		--	6.0	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.8	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.2	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.8 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2.4 A, dI _F / dt = 100 A/μs (Note 4)	--	480	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.0	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 105\text{ mH}, I_{AS} = 1.8\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.4\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

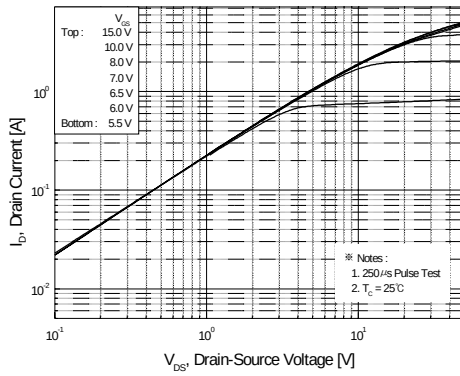


Figure 1. On-Region Characteristics

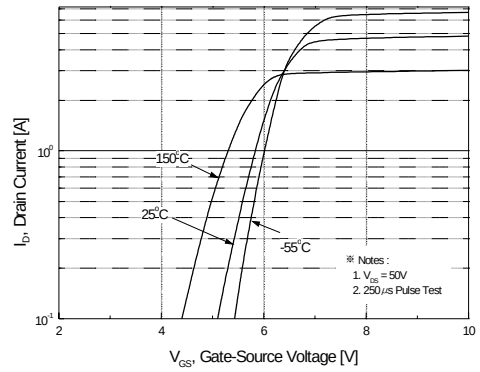


Figure 2. Transfer Characteristics

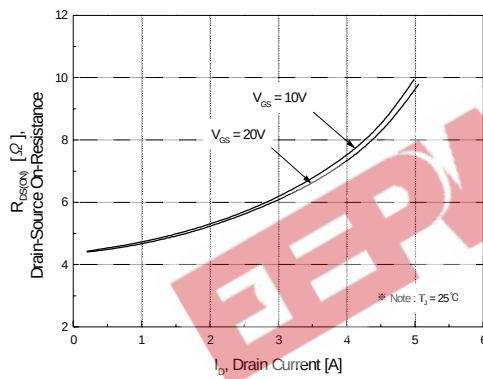


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

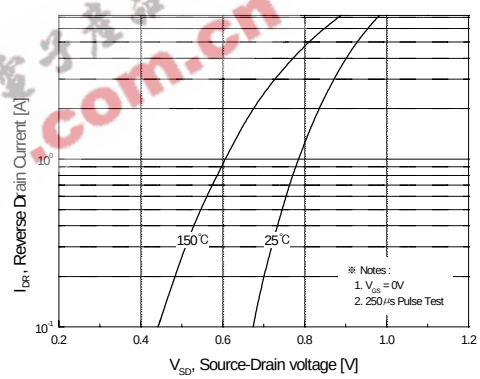


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

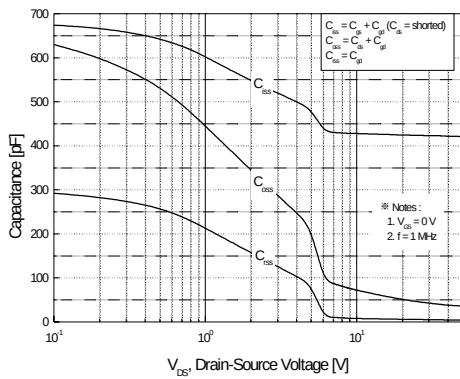


Figure 5. Capacitance Characteristics

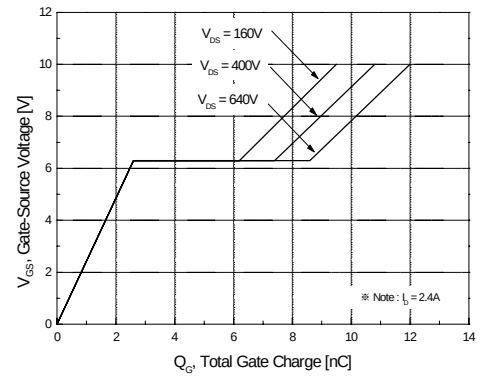


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

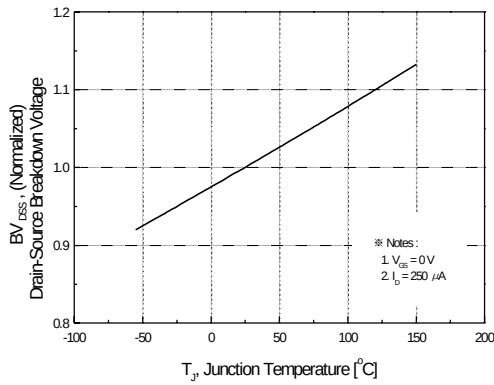


Figure 7. Breakdown Voltage Variation vs Temperature

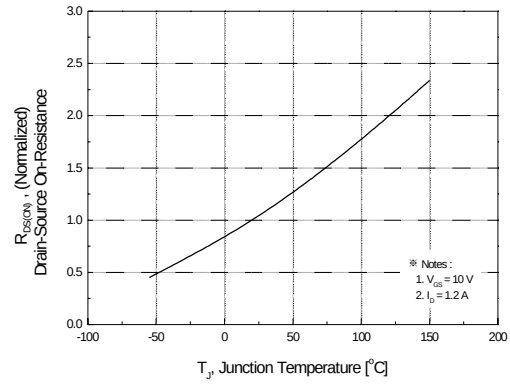


Figure 8. On-Resistance Variation vs Temperature

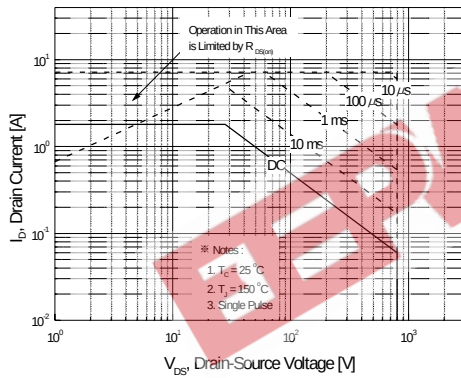


Figure 9. Maximum Safe Operating Area

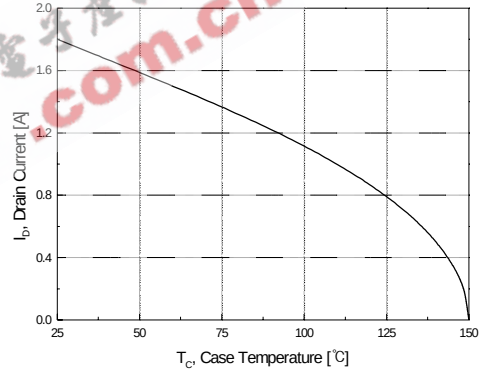


Figure 10. Maximum Drain Current vs Case Temperature

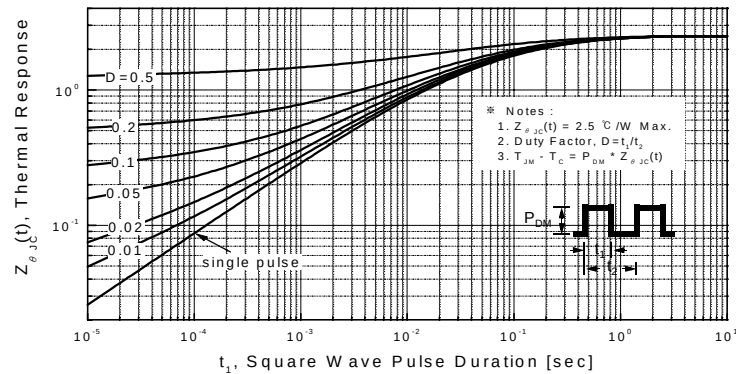
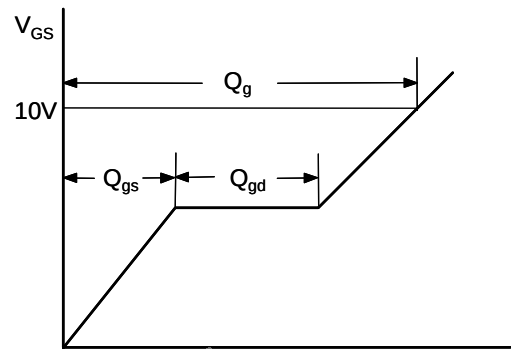
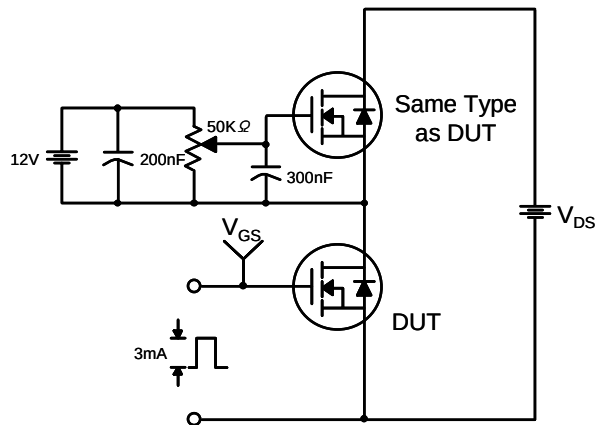


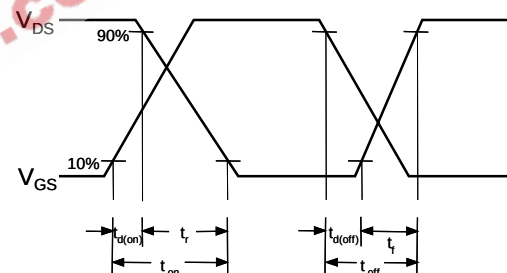
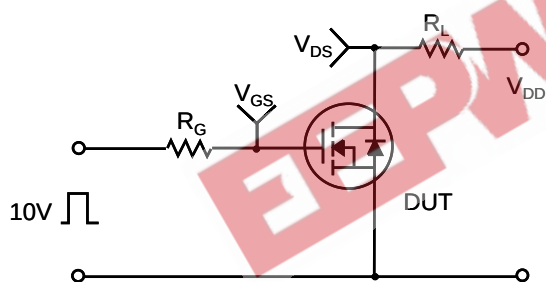
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

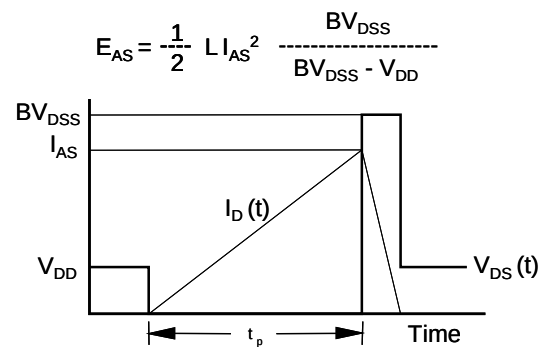
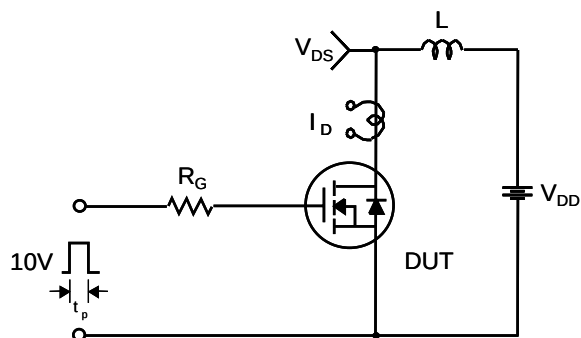


Charge

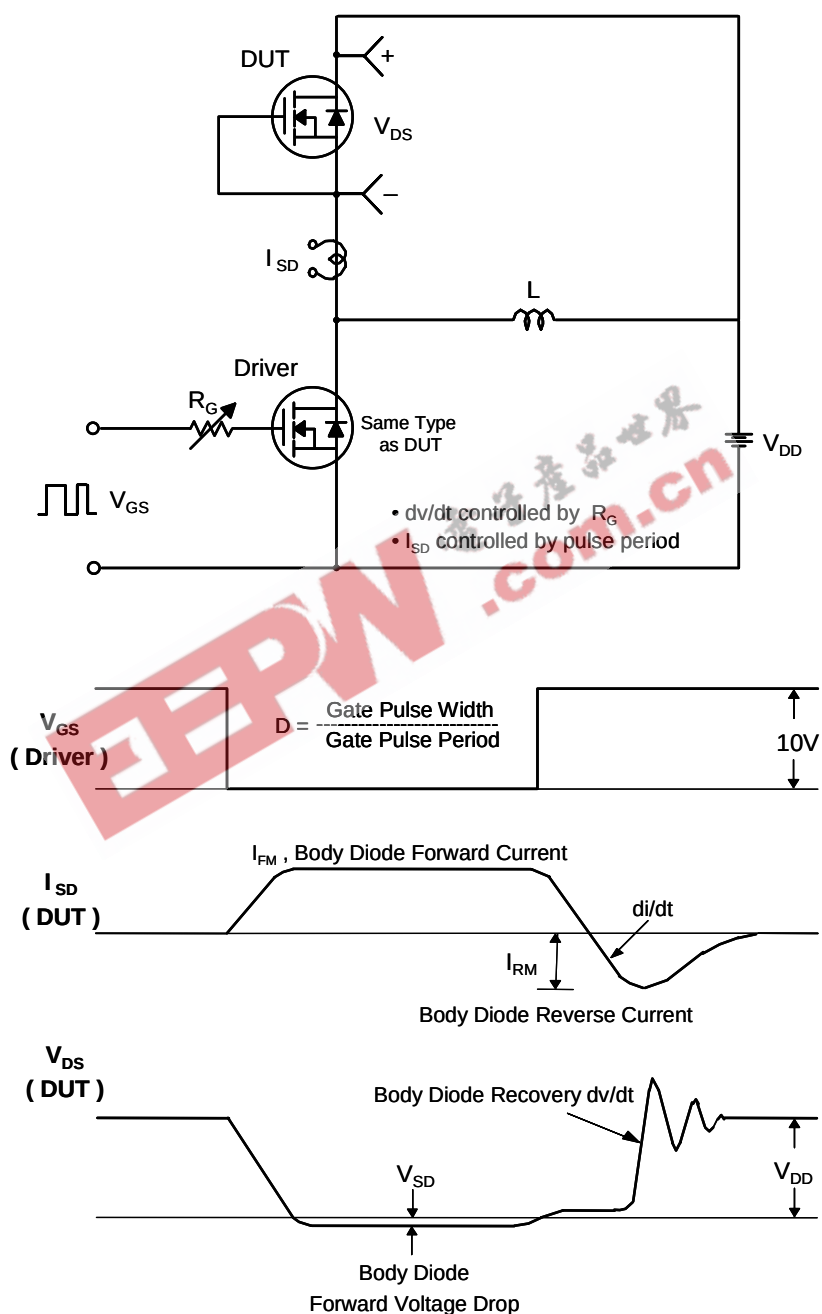
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

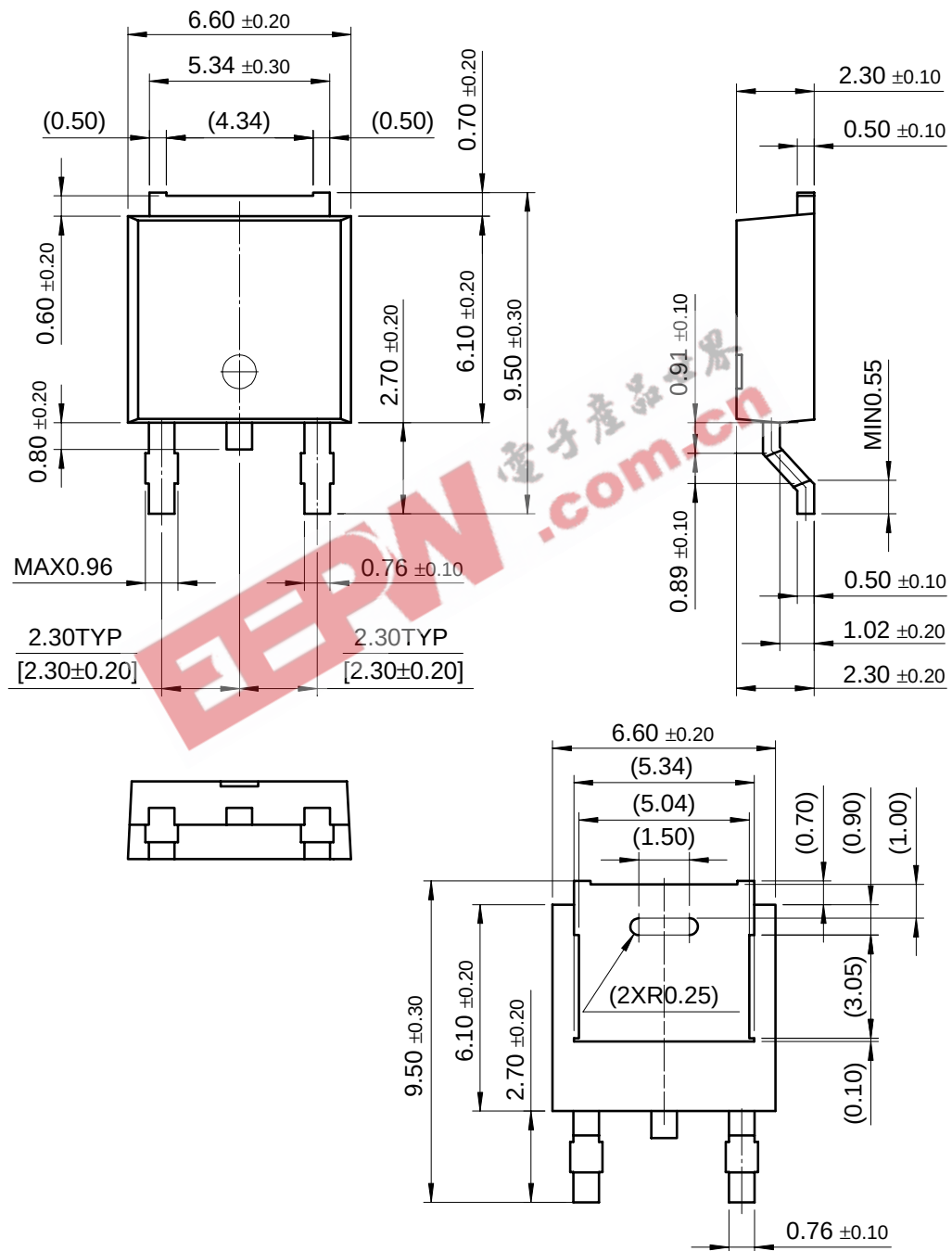


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

DPAK



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