FAIRCHILD SEMICONDUCTOR®

September 2001
Revised July 2002

FSTD32211
40/48-Bit Bus Switch with Level Shifting

General Description

The Fairchild Switch FSTD32211 provides up to 48-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to V_{CC} has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device can be organized as four 12-bit, two 24-bit, or one 48-bit bus switch. When routed as a 40-bit bus switch, the device can be organized as four 10-bit, two 20-bit or one 40-bit bus switch. When $\overline{OE}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{OE}_2$ is LOW, the switch is ON and Port 2A is connected to Port 2B. When $\overline{OE}_3$ is LOW, the switch is ON and Port 3A is connected to Port 3B. When $\overline{OE}_4$ is LOW, the switch is ON and Port 4A is connected to Port 4B. When $\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, or $\overline{OE}_4$ are HIGH, a high impedance state exists between the A and B Ports.

Features

- 4Ω switch connection between two ports
- Voltage level shifting
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

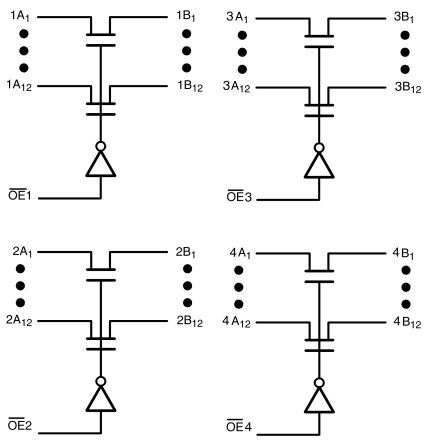
Ordering Code:

Order Number	Package Number	Package Description
FSTD32211G (Note 1)(Note 2)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

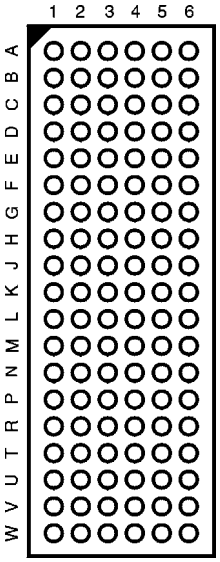
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, $\overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B

FBGA Pin Assignments

(40-Bit Routing)

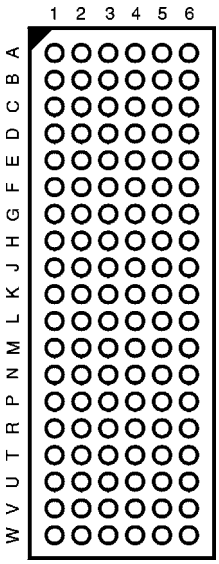
	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	OE_2	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	GND	OE_1	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	GND	$1B_5$	$1B_6$
D	$1A_8$	$1A_7$	GND	GND	$1B_7$	$1B_8$
E	$1A_{10}$	$1A_9$	V_{CC}	V_{CC}	$1B_9$	$1B_{10}$
F	$2A_2$	$2A_1$	V_{CC}	V_{CC}	$2B_1$	$2B_2$
G	$2A_4$	$2A_3$	V_{CC}	GND	$2B_3$	$2B_4$
H	$2A_6$	$2A_5$	GND	GND	$2B_5$	$2B_6$
J	$2A_8$	$2A_7$	$2A_9$	$2B_9$	$2B_7$	$2B_8$
K	$2A_{10}$	$3A_{10}$	GND	GND	$3B_{10}$	$2B_{10}$
L	$3A_9$	$3A_8$	GND	GND	$3B_8$	$3B_9$
M	$3A_7$	$3A_6$	GND	V_{CC}	$3B_6$	$3B_7$
N	$3A_5$	$3A_4$	V_{CC}	V_{CC}	$3B_4$	$3B_5$
P	$3A_3$	$3A_2$	V_{CC}	V_{CC}	$3B_2$	$3B_3$
R	$3A_1$	$4A_{10}$	GND	GND	$4B_{10}$	$3B_1$
T	$4A_9$	$4A_8$	GND	GND	$4B_8$	$4B_9$
U	$4A_7$	$4A_6$	GND	$4B_1$	$4B_6$	$4B_7$
V	$4A_5$	$4A_4$	$4A_1$	OE_4	$4B_4$	$4B_5$
W	$4A_3$	$4A_2$	OE_3	NC	$4B_2$	$4B_3$

Truth Tables

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Inputs		Inputs/Outputs	
$\overline{OE}_3$	$\overline{OE}_4$	3A, 3B	4A, 4B
L	L	3A = 3B	4A = 4B
L	H	3A = 3B	Z
H	L	Z	4A = 4B
H	H	Z	Z

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

(48-Bit Routing)

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	$\overline{OE}_2$	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$1A_7$	$\overline{OE}_1$	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	$1B_7$	$1B_5$	$1B_6$
D	$1A_{10}$	$1A_9$	$1A_8$	$1B_8$	$1B_9$	$1B_{10}$
E	$1A_{12}$	$1A_{11}$	$2A_1$	$2B_1$	$1B_{11}$	$1B_{12}$
F	$2A_4$	$2A_3$	$2A_2$	$2B_2$	$2B_3$	$2B_4$
G	$2A_6$	$2A_5$	V_{CC}	GND	$2B_5$	$2B_6$
H	$2A_8$	$2A_7$	GND	GND	$2B_7$	$2B_8$
J	$2A_{10}$	$2A_9$	$2A_{11}$	$2B_{11}$	$2B_9$	$2B_{10}$
K	$2A_{12}$	$3A_{12}$	GND	GND	$3B_{12}$	$2B_{12}$
L	$3A_{11}$	$3A_{10}$	GND	GND	$3B_{10}$	$3B_{11}$
M	$3A_9$	$3A_8$	GND	V_{CC}	$3B_8$	$3B_9$
N	$3A_7$	$3A_6$	$3A_2$	$3B_2$	$3B_6$	$3B_7$
P	$3A_5$	$3A_4$	$3A_1$	$3B_1$	$3B_4$	$3B_5$
R	$3A_3$	$4A_{12}$	$4A_8$	$4B_8$	$4B_{12}$	$3B_3$
T	$4A_{11}$	$4A_{10}$	$4A_7$	$4B_7$	$4B_{10}$	$4B_{11}$
U	$4A_9$	$4A_6$	GND	$4B_1$	$4B_6$	$4B_9$
V	$4A_5$	$4A_4$	$4A_1$	$\overline{OE}_4$	$4B_4$	$4B_5$
W	$4A_3$	$4A_2$	$\overline{OE}_3$	NC	$4B_2$	$4B_3$

Pin Descriptions

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$, $\overline{OE}_4$	Bus Switch Enables
1A, 2A, 3A, 4A	Bus A
1B, 2B, 3B, 4B	Bus B

Truth Tables

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

Inputs		Inputs/Outputs	
$\overline{OE}_3$	$\overline{OE}_4$	3A, 3B	4A, 4B
L	L	3A = 3B	4A = 4B
L	H	3A = 3B	Z
H	L	Z	4A = 4B
H	H	Z	Z

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	0.5V to +7.0V
DC Switch Voltage (V_S) (Note 4)	−0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN})(Note 5)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50 mA
DC Output (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 6)

Power Supply Operating (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T_A)	-40 °C to +85 °C

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: V_S is the voltage observed/applied at either A or B Ports across the switch.

Note 5: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 6: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 7)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18 mA
V_{IH}	HIGH Level Input Voltage	4.5 - 5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.5 - 5.5			0.8	V	
V_{OH}	HIGH Level	4.5 - 5.5	See Figure 3			V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OZ}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, B ≤ V_{CC}
R_{ON}	Switch On Resistance (Note 8)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		35	50	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			1.5	mA	OE_1 = OE_2 = GND V_{IN} = V_{CC} or GND, I_{OUT} = 0
					10	µA	OE_1 = OE_2 = V_{CC} V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One Input at 3.4V Other Inputs at V_{CC} or GND

Note 7: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 8: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,^{\circ}C$ to $+85\,^{\circ}C$, $C_L = 50pF$, $RU = RD = 500\Omega$ $V_{CC} = 4.5 - 5.5V$		Units	Conditions	Figure Number
		Min	Max			
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus (Note 9)		0.25	ns	V_I = OPEN	Figures 1, 2
t_{PZH}, t_{PZL}	Output Enable Time	1.5	10.0	ns	V_I = 7V for t_{PZL} V_I = OPEN for t_{PZH}	Figures 1, 2
t_{PHZ}, t_{PLZ}	Output Disable Time	1.5	9.0	ns	V_I = 7V for t_{PLZ} V_I = OPEN for t_{PHZ}	Figures 1, 2

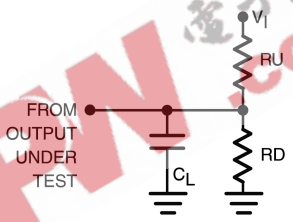
Note 9: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 10)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control Pin Input Capacitance	3		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	6		pF	V_{CC}, $\overline{OE}$ = 5.0V

Note 10: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

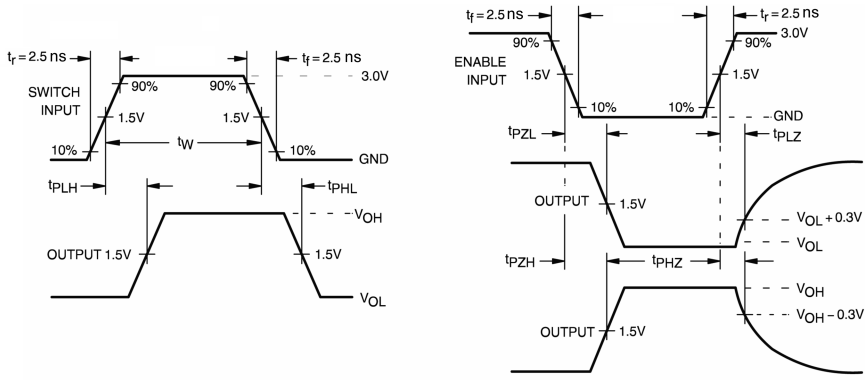


FIGURE 2. AC Waveforms

Output Voltage HIGH vs. Supply Voltage

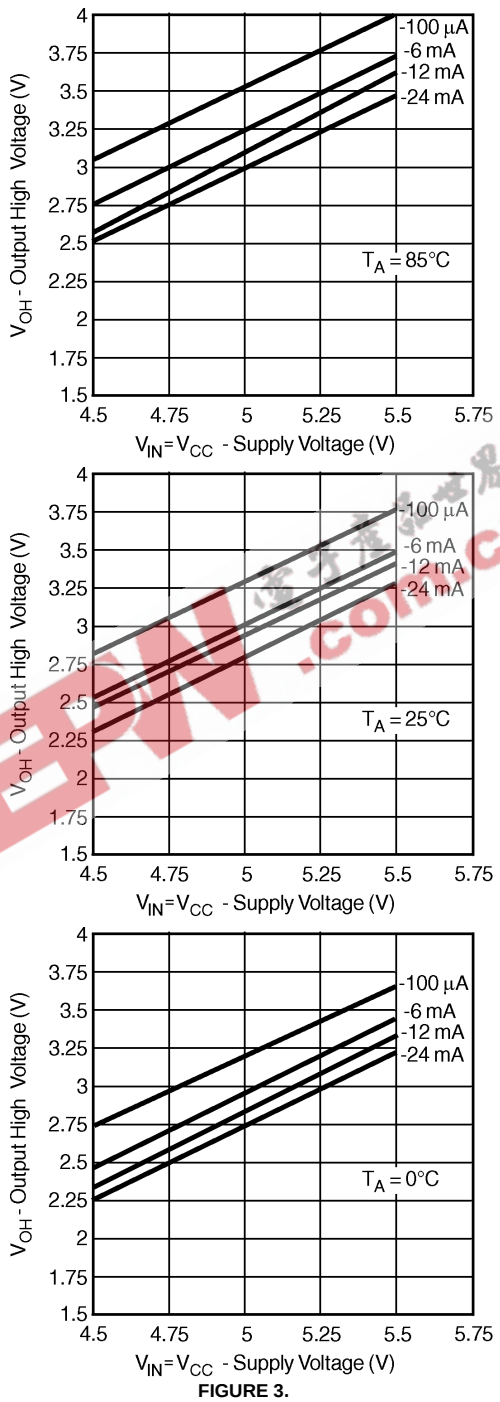
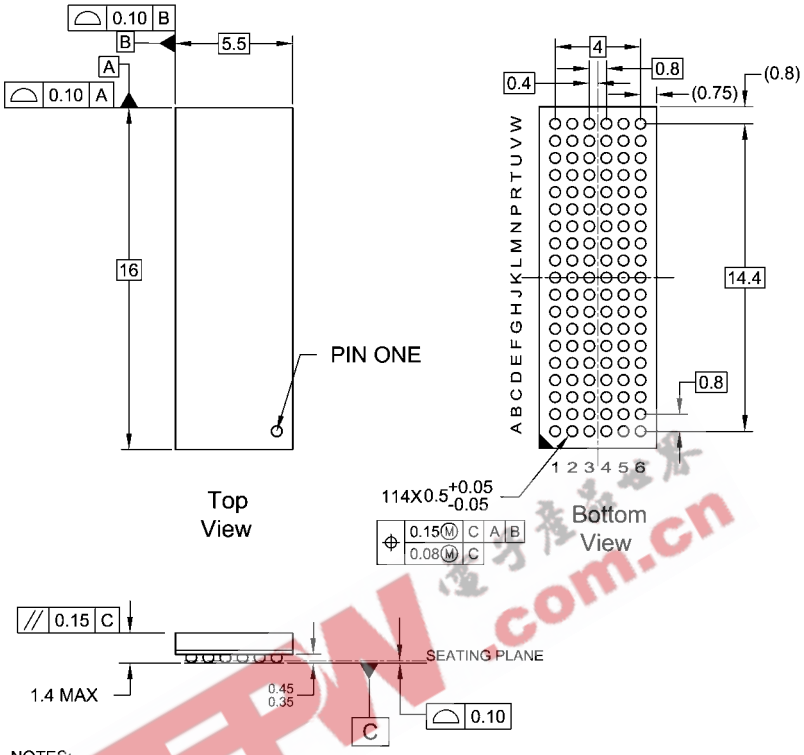


FIGURE 3.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA114A

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.