FAIRCHILD
SEMICONDUCTOR™

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QFET™

FQA10N80

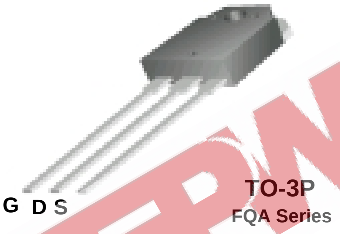
800V N-Channel MOSFET

General Description

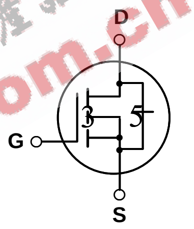
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

Features

- 9.8A, 800V, $R_{DS(on)}$ = 1.05Ω @V_{GS} = 10 V
- Low gate charge (typical 55 nC)
- Low Crss (typical 24 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-3P
FQA Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FQA10N80	Units
V_{DSS}	Drain-Source Voltage		800	V
I_D	Drain Current - Continuous (T_C = 25°C)		9.8	A
	- Continuous (T_C = 100°C)		6.19	A
I_{DM}	Drain Current - Pulsed	(Note 1)	39.2	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	920	mJ
I_{AR}	Avalanche Current	(Note 1)	9.8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	24	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		240	W
	- Derate above 25°C		1.92	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.52	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	800	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.9	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	--	--	10	µA
		V_{DS} = 640 V, T_C = 125°C	--	--	100	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.9 A	--	0.81	1.05	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 4.9 A (Note 4)	--	10	--	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2100	2700	pF
C_{oss}	Output Capacitance		--	215	280	pF
C_{rss}	Reverse Transfer Capacitance		--	24	30	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 9.8 A, R_G = 25 Ω (Note 4, 5)	--	45	100	ns
t_r	Turn-On Rise Time		--	115	240	ns
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	ns
t_f	Turn-Off Fall Time		--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 640 V, I_D = 9.8 A, V_{GS} = 10 V (Note 4, 5)	--	55	71	nC
Q_{gs}	Gate-Source Charge		--	12	--	nC
Q_{gd}	Gate-Drain Charge		--	26	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9.8	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	39.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.8 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 9.8 A, dI_F / dt = 100 A/µs (Note 4)	--	780	--	ns
Q_{rr}	Reverse Recovery Charge		--	9.4	--	µC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 18mH, I_{AS} = 9.8A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 9.8A, di/dt $\leq$ 200A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

Typical Characteristics

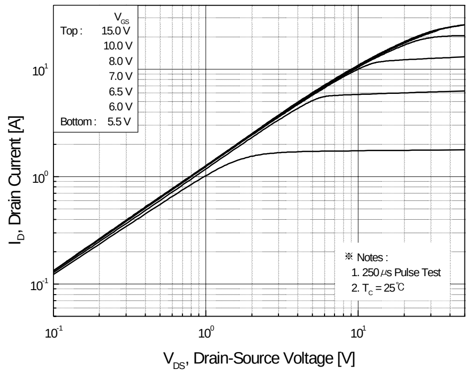


Figure 1. On-Region Characteristics

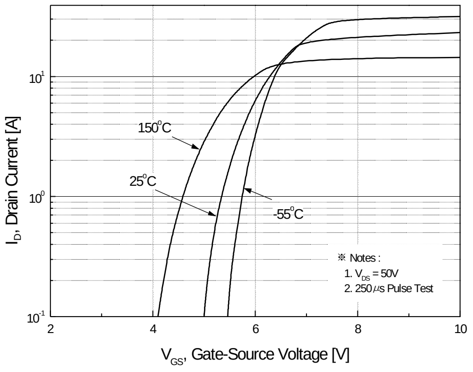


Figure 2. Transfer Characteristics

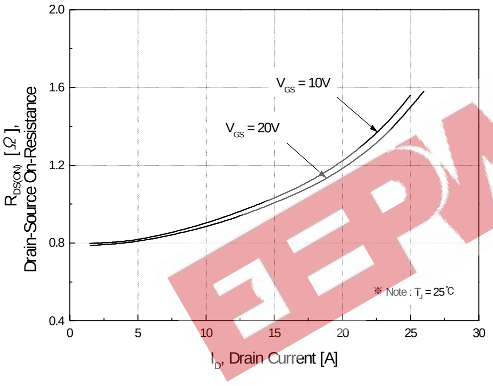


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

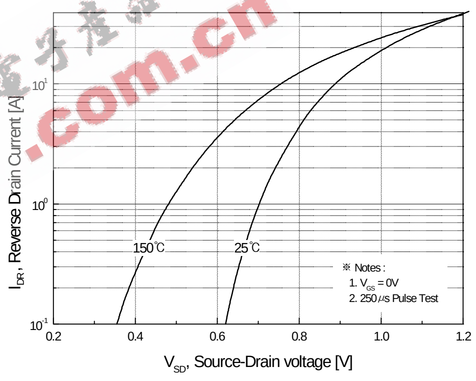


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

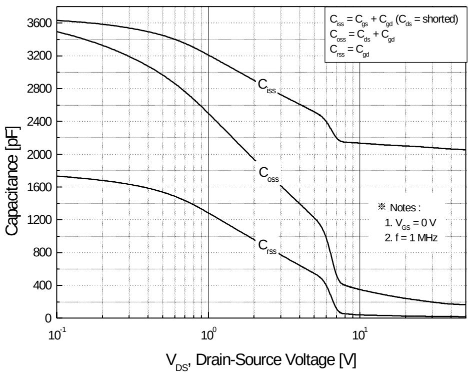


Figure 5. Capacitance Characteristics

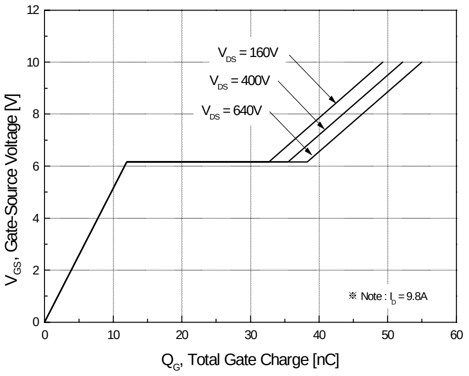


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

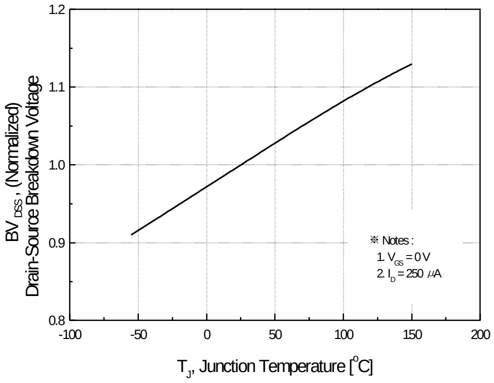


Figure 7. Breakdown Voltage Variation vs. Temperature

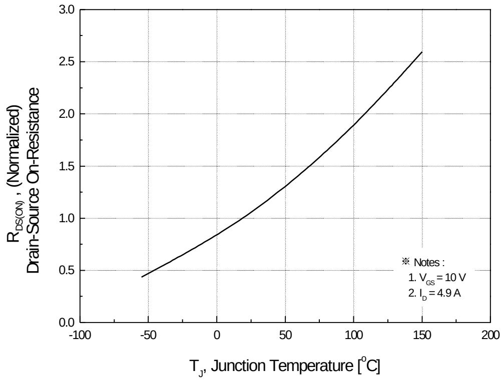


Figure 8. On-Resistance Variation vs. Temperature

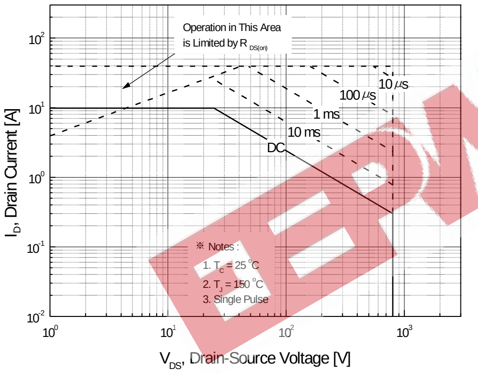


Figure 9. Maximum Safe Operating Area

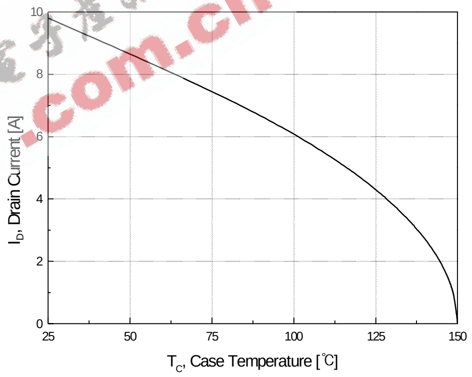


Figure 10. Maximum Drain Current vs. Case Temperature

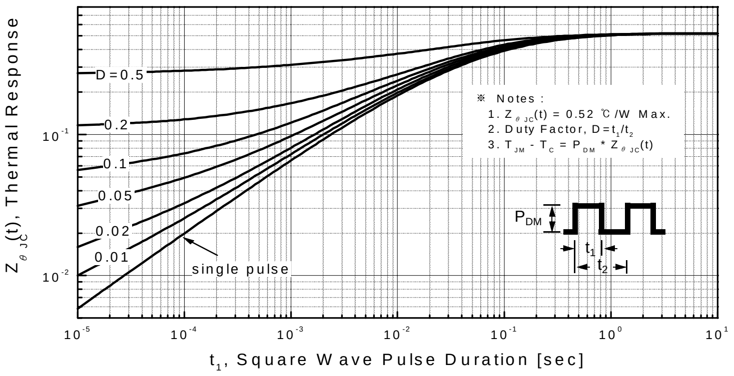
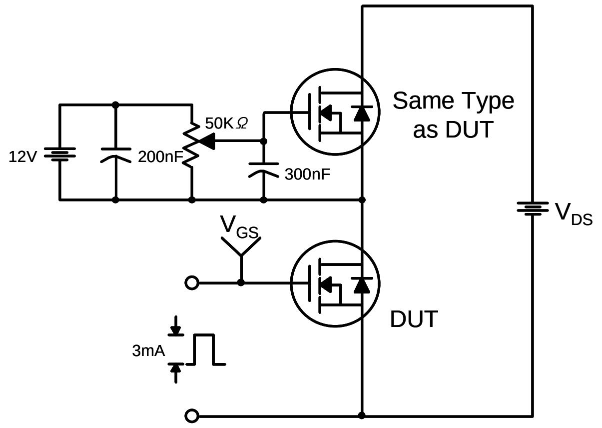
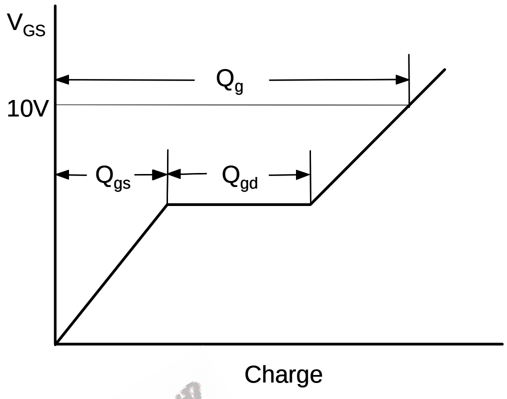


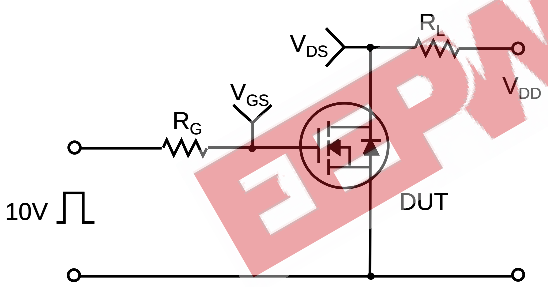
Figure 11. Transient Thermal Response Curve

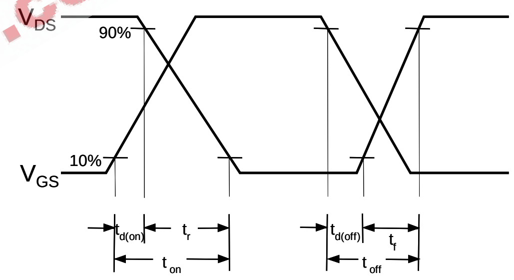
Gate Charge Test Circuit & Waveform



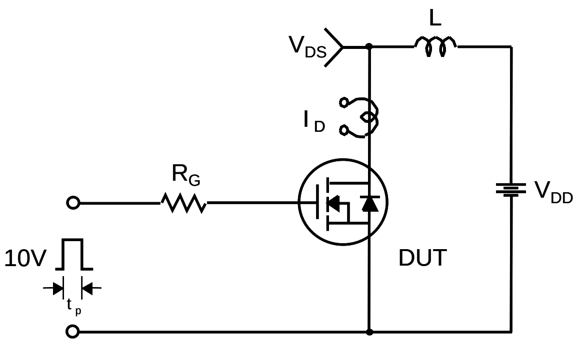


Resistive Switching Test Circuit & Waveforms

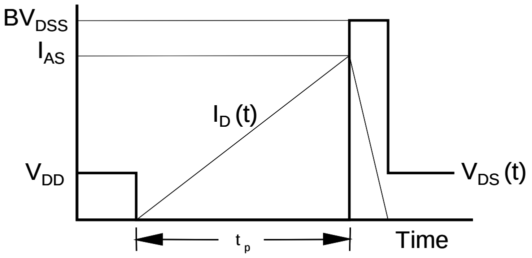




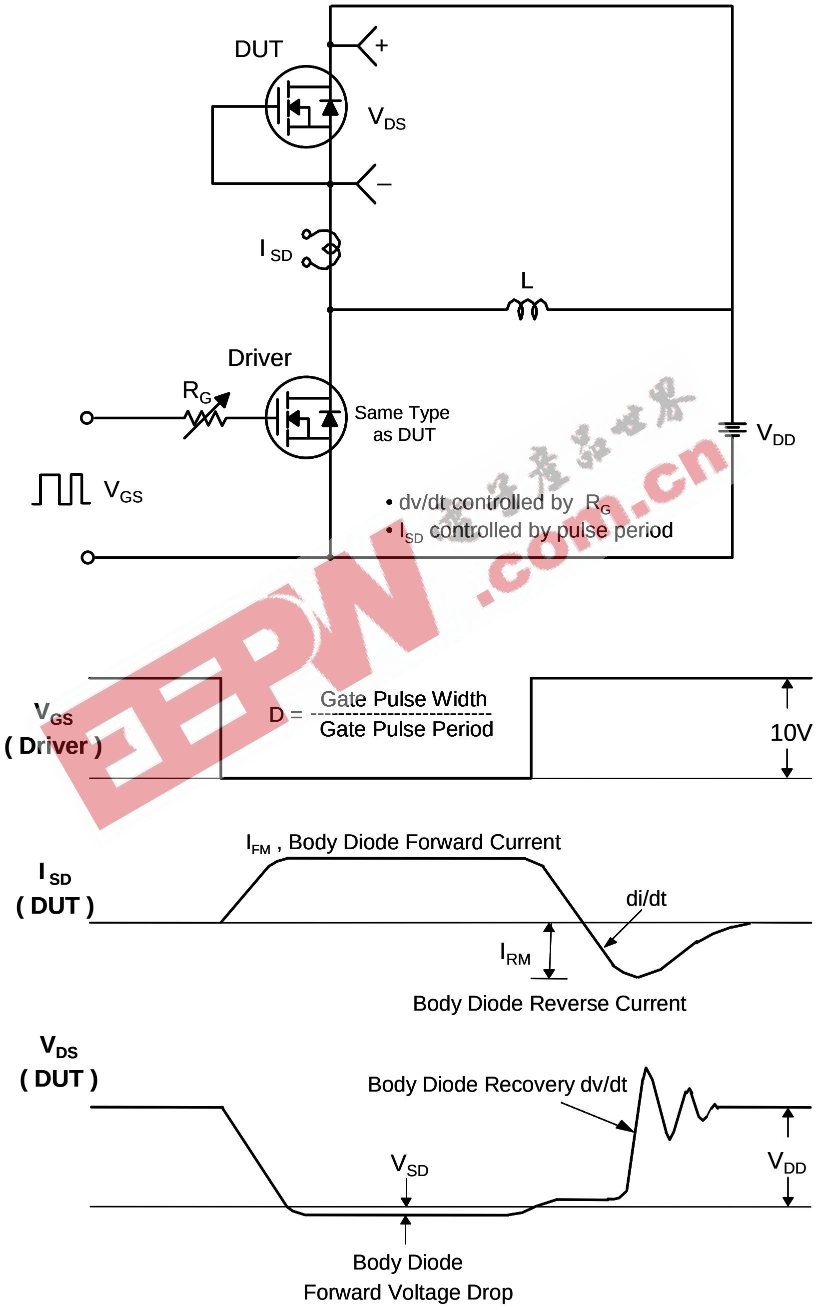
Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms

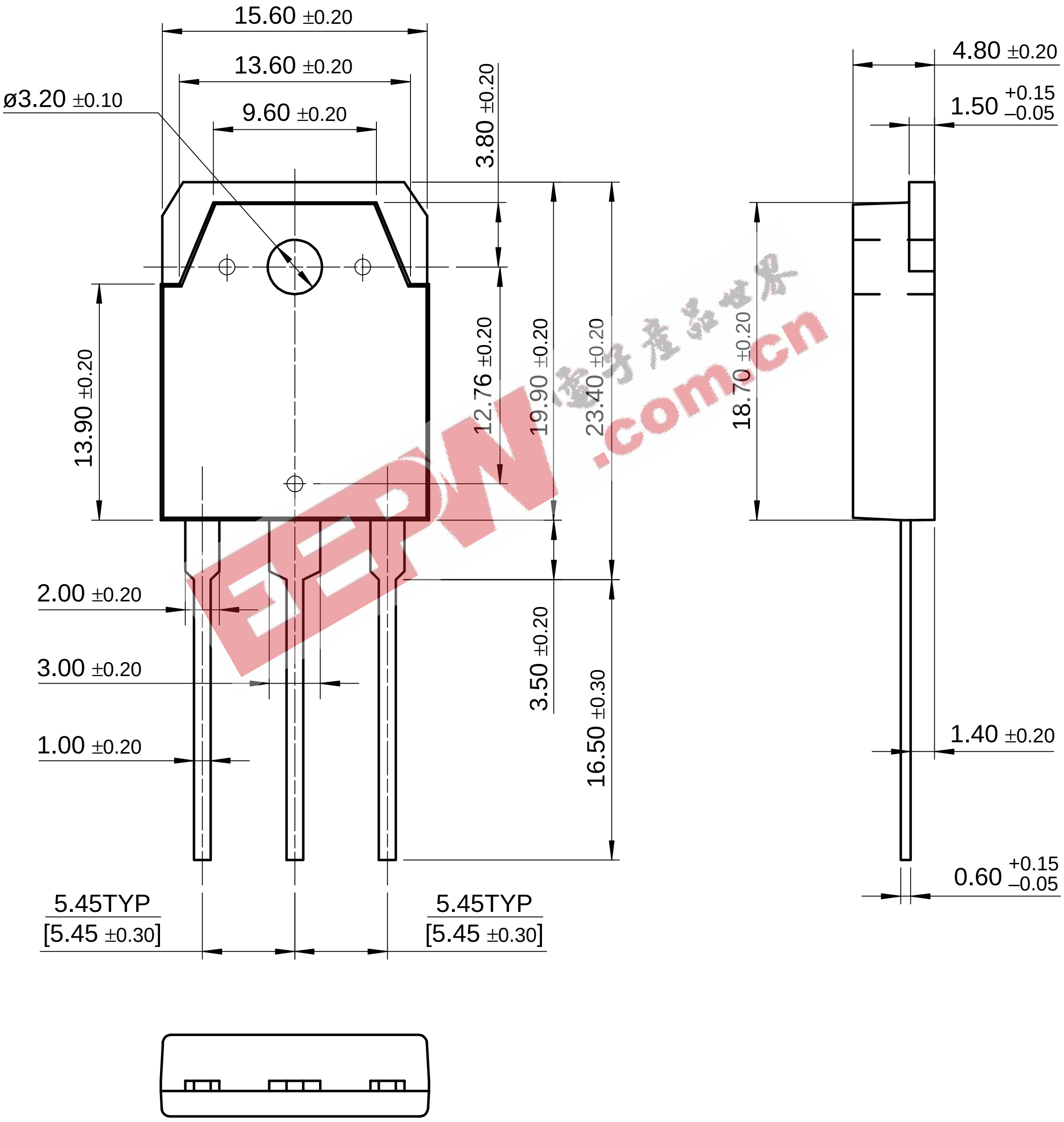


- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

Package Dimensions

TO-3P



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