PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844101I-312

FEMTOCLOCKS™ CRYSTAL-TO-LVDS 312.5MHZ FREQUENCY MARGINING SYNTHESIZER

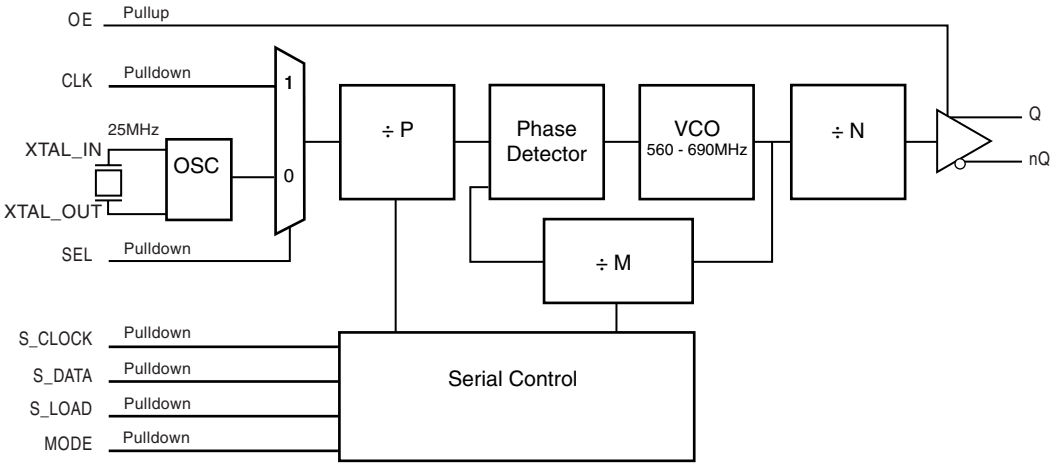
GENERAL DESCRIPTION

The ICS844101I-312 is a low phase-noise frequency margining synthesizer and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. In the default mode, the device nominally generates a 312.5MHz LVDS output clock signal from a 25MHz crystal input. There is also a frequency margining mode available where the device can be programmed, using the serial interface, to vary the output frequency up or down from nominal in 2% steps. The ICS844101I-312 is provided in a 16-pin TSSOP.

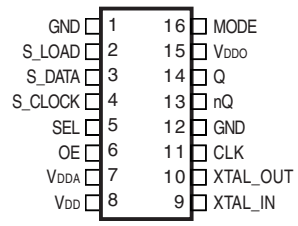
FEATURES

- One 312.5MHz nominal LVDS output
- Selectable crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal or LVCMOS single-ended input
- Output frequency can be varied in 2% steps ± from nominal
- VCO range: 560MHz - 690MHz
- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (1.875MHz-20MHz): 0.52ps (typical)
- Output supply modes
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-complaint packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS844101I-312
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

FUNCTIONAL DESCRIPTION

The ICS844101I-312 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 25MHz fundamental crystal is used as the input to the on chip oscillator. The output of the oscillator is fed into the pre-divider. In frequency margining mode, the 25MHz crystal frequency is divided by 2 and a 12.5MHz reference frequency is applied to the phase detector. The VCO of the PLL operates over a range of 560MHz to 690MHz. The output of the M divider is also applied to the phase detector.

The default mode for the ICS844101I-312 is 312.5MHz output frequency using a 25MHz crystal. The output frequency can be changed by placing the device into the margining mode using the mode pin and using the serial interface to program the M feedback divider. Frequency margining mode operation occurs when the MODE input is HIGH. The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by an output divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1. When changing back from frequency margining mode to nominal mode, the device will return to the default nominal configuration that will provide 312.5MHz output frequency.

Serial operation occurs when S_LOAD is HIGH. Serial data can be loaded in either the default mode or the frequency margining mode. The 6-bit shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. After shifting in the 6-bit M divider value, S_LOAD is transitioned from HIGH to LOW which latches the contents of the shift-register into the M divider control register. When S_LOAD is LOW, any transitions of S_CLOCK or S_DATA are ignored.

TABLE 1. FREQUENCY MARGIN FUNCTION TABLE

XTAL (MHz)	Pre-Divider (P)	Reference Frequency (MHz)	Feedback Divider (M)	M-Data (Binary)	VCO (MHz)	Output Divider (N)	Output Frequency (MHz)	% Change
25	2	12.5	45	101101	562.5	2	281.25	-10.0
25	2	12.5	46	101110	575	2	287.5	-8.0
25	2	12.5	47	101111	587.5	2	293.75	-6.0
25	2	12.5	48	110000	600	2	300	-4.0
25	2	12.5	49	110001	612.5	2	306.25	-2.0
25	2	12.5	50	110010	625	2	312.5	0
25	2	12.5	51	110011	637.5	2	318.75	2.0
25	2	12.5	52	110100	650	2	325	4.0
25	2	12.5	53	110101	662.5	2	331.25	6.0
25	2	12.5	54	110110	675	2	337.5	8.0
25	2	12.5	55	110111	687.5	2	343.75	10.0

SERIAL LOADING

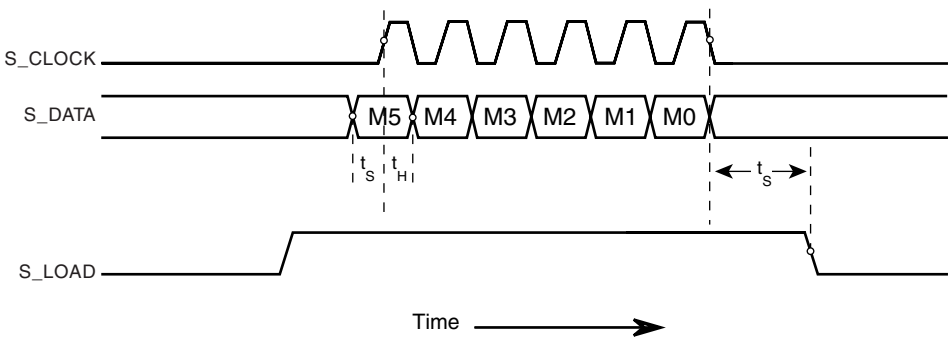


FIGURE 1. SERIAL LOAD OPERATIONS

TABLE 2. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12	GND	Power		Power supply ground.
2	S_LOAD	Input	Pulldown	Controls the operation of the Serial input. LVCMOS/LVTTL interface levels.
3	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
4	S_CLOCK	Input	Pulldown	Clock in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
5	SEL	Input	Pulldown	Select pin. When HIGH, selects CLK input. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
6	OE	Input	Pullup	Output enable pin. Controls enabling and disabling of Q/nQ outputs. LVCMOS/LVTTL interface levels
7	V_{DDA}	Power		Analog supply pin.
8	V_{DD}	Power		Core supply pin.
9, 10	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
11	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
13, 14	nQ, Q	Ouput		Differential output pair. LVPECL interface levels.
15	V_{DDO}	Power		Output supply pin.
16	MODE	Input	Pulldown	MODE pin. LOW = default mode. HIGH = frequency margining mode. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pulldown Resistor			51		kΩ

TABLE 4A. OE CONTROL INPUT FUNCTION TABLE

Input	Outputs
OE	Q, nQ
0	HiZ
1	Enabled

TABLE 4B. SEL CONTROL INPUT FUNCTION TABLE

Input	
SEL	Selected Source
0	XTAL_IN, XTAL_OUT
1	CLK

TABLE 4C. MODE CONTROL INPUT FUNCTION TABLE

Input	Condition
Mode	Q, nQ
0	Default Mode
1	Frequency Margining Mode

TABLE 4D. SERIAL MODE FUNCTION TABLE

Inputs			Conditions
S_LOAD	S_CLOCK	S_DATA	
L	X	X	Serial inputs are ignored.
H	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
↓	L	X	Contents of the shift register are latched.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			85		mA
I_{DDA}	Analog Supply Current			7		mA
I_{DDO}	Output Supply Current			19		mA

TABLE 5B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			85		mA
I_{DDA}	Analog Supply Current			7		mA
I_{DDO}	Output Supply Current			18		mA

TABLE 5C. LVCMOS / LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	CLK, SEL, S_LOAD, S_CLOCK, S_DATA, MODE	V_{DD} = V_{IN} = 3.465			150	µA
		OE	V_{DD} = V_{IN} = 3.465			5	µA
I_{IL}	Input Low Current	CLK, SEL, S_LOAD, S_CLOCK, S_DATA, MODE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
Δt/Δv	Input Transistion Rise/Fall Rate	OE, SEL, S_CLOCK, S_DATA, S_LOAD, MODE				20	ns/v

TABLE 5D. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			375		mV
Δ V_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.42		V
Δ V_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5E. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDA} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			365		mV
Δ V_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.37		V
Δ V_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				100	µW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 7. INPUT FREQUENCY CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK			25		MHz
		XTAL_IN/XTAL_OUT			25		MHz
		S_CLOCK				50	MHz

TABLE 8A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				312.5		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1		Mode = LOW 312.5MHz, (1.875MHz - 20MHz)		0.52		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		360		ps
odc	Output Duty Cycle				50		%
t_S	Setup Time	S_DATA to S_CLOCK		10			ns
		S_CLOCK to S_LOAD		10			ns
t_H	Hold Time	S_DATA to S_CLOCK		10			ns

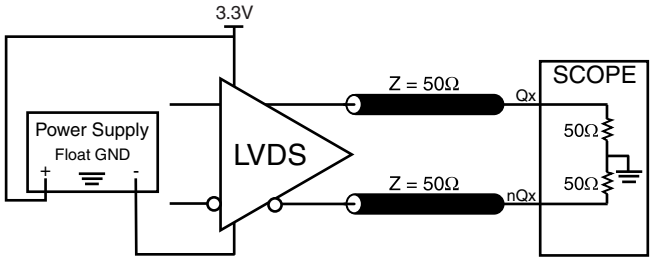
NOTE 1: Characterized using a 25MHz crystal.

TABLE 8B. AC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

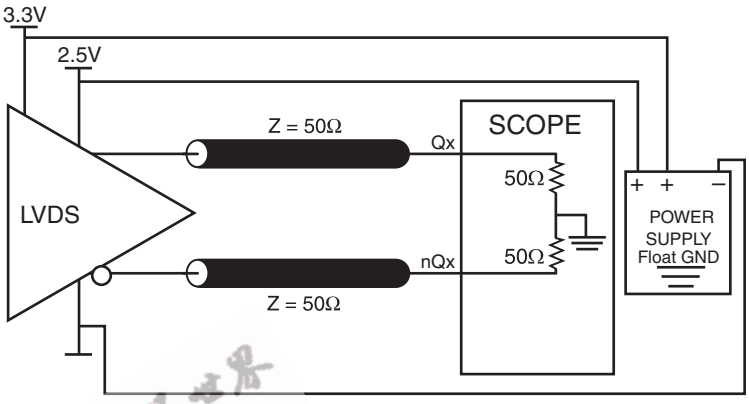
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				312.5		MHz
*t*jit(Ø)	RMS Phase Jitter; NOTE 1		Mode = LOW 312.5MHz, (1.875MHz - 20MHz)		0.50		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		375		ps
odc	Output Duty Cycle				50		%
t_S	Setup Time	S_DATA to S_CLOCK		10			ns
		S_CLOCK to S_LOAD		10			ns
t_H	Hold Time	S_DATA to S_CLOCK		10			ns

NOTE 1: Characterized using a 25MHz crystal.

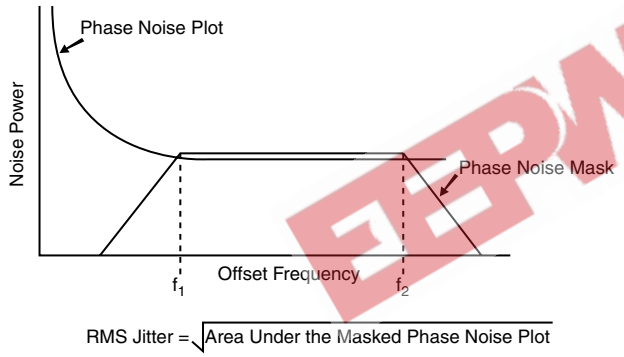
PARAMETER MEASUREMENT INFORMATION



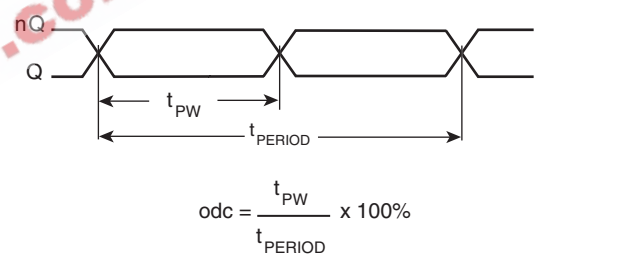
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



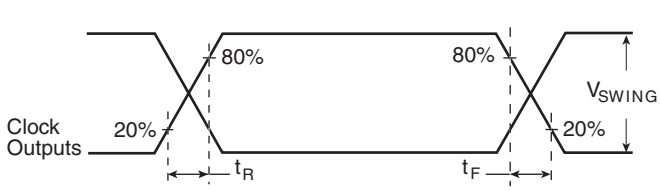
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



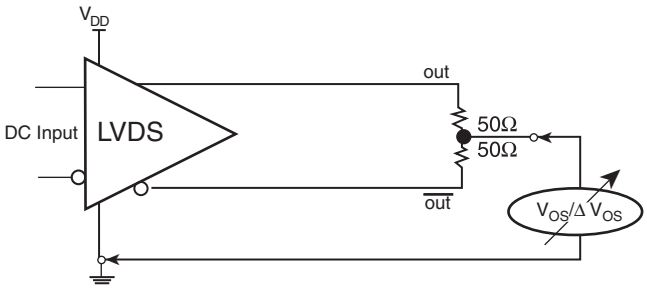
RMS PHASE JITTER



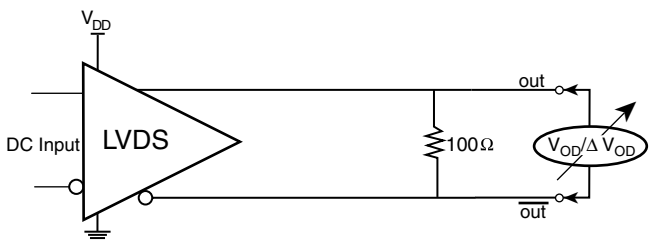
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844101I-312 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}. The 10Ω resistor can also be replaced by a ferrite bead.

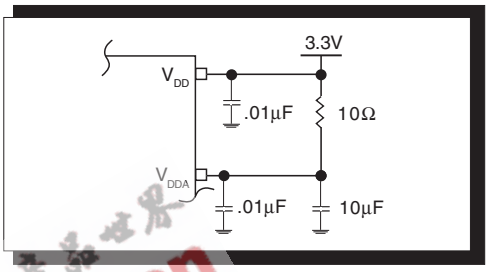


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844101I-312 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

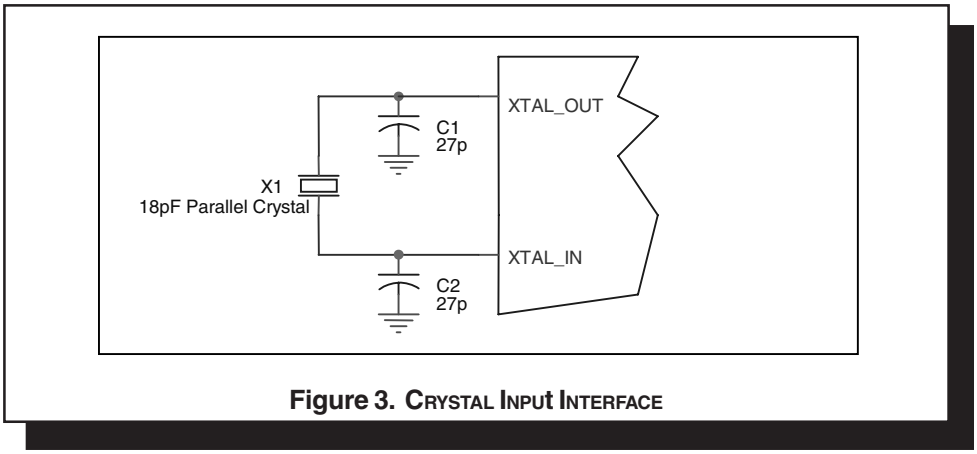


Figure 3. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

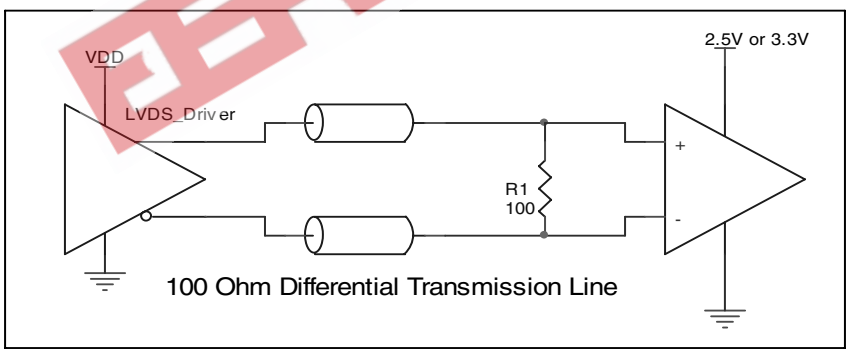


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS844101I-312 is: 4093

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

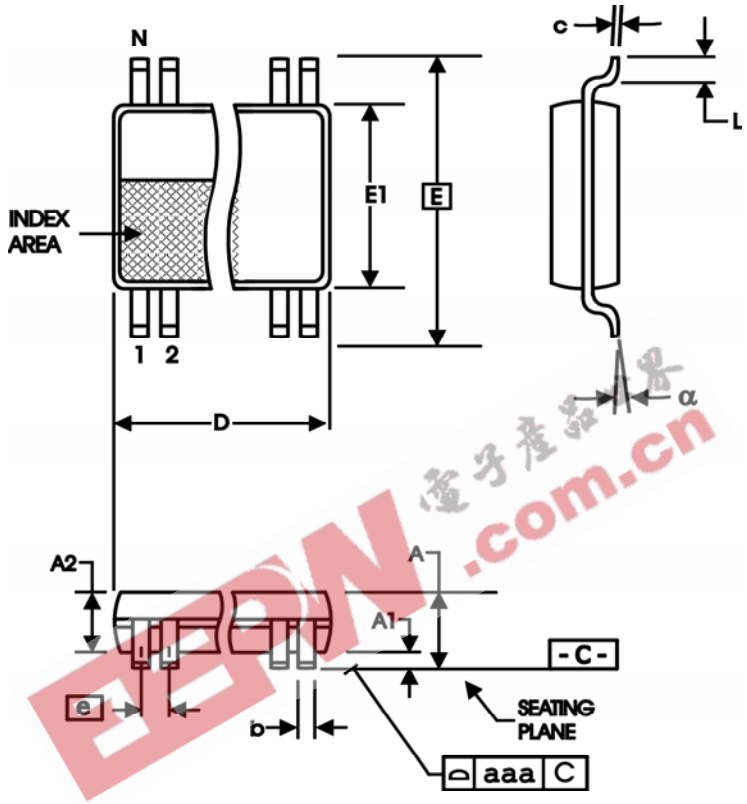


TABLE 10. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844101AGI-312	TBD	16 Lead TSSOP	tube	-40°C to 85°C
ICS844101AGI-312T	TBD	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS844101AGI-312LF	TBD	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844101AGI-312LFT	TBD	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS complaint.