IA82050
ASYNCHRONOUS SERIAL CONTROLLER

Data Sheet

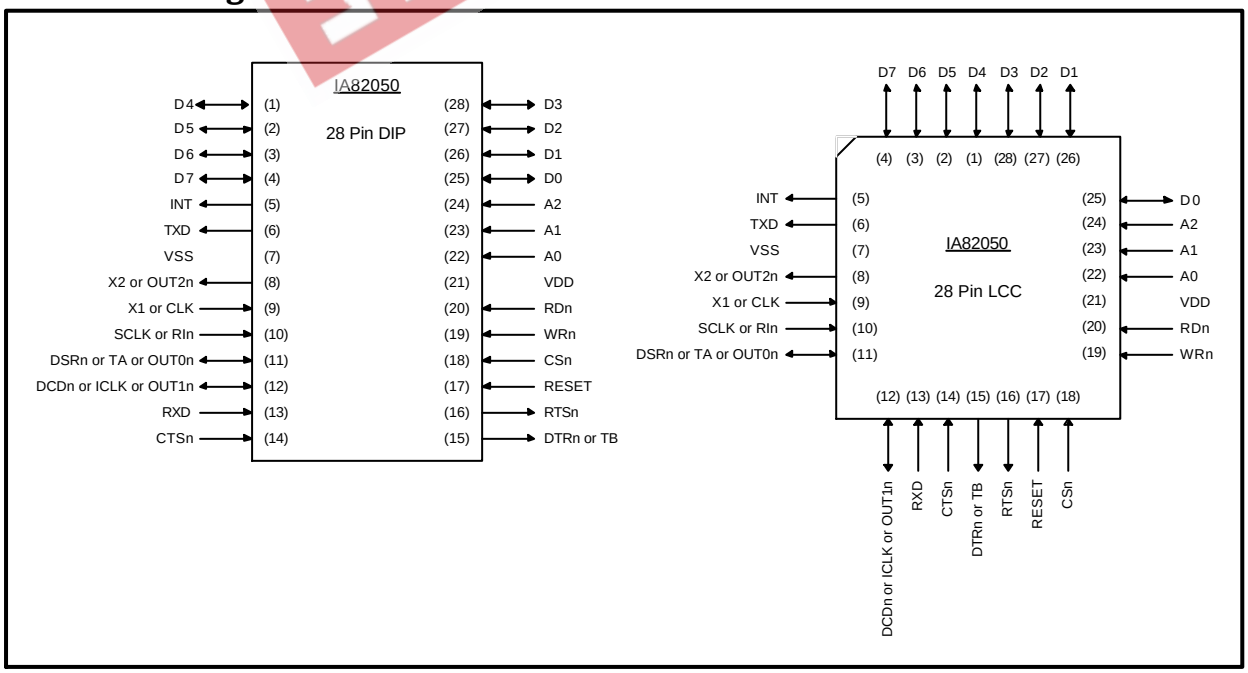
As of Production Ver. 01

FEATURES

- **Form, Fit, and Function Compatible with the Intel® 82050 and 82510**
- **Packaging options available: 28 Pin Plastic DIP and 28 Lead Plastic Leaded Chip Carrier**
- **Asynchronous Serial Channel Operation**
- **Separate Transmit and Receive FIFOs with Programmable Threshold**
- **Programmable Baud Rate Generators up to 288K Baud**
- **Special Protocol Features**
  - **Control Character Recognition**
  - **Auto Echo and Loopback Modes**
  - **9-Bit Protocol Support**
  - **5 to 9 Bit Character Format**

The IA82050 is a "plug-and-play" drop-in replacement for the original IC. innovASIC produces replacement ICs using its MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA82050 including functional and I/O descriptions, electrical characteristics, and applicable timing.

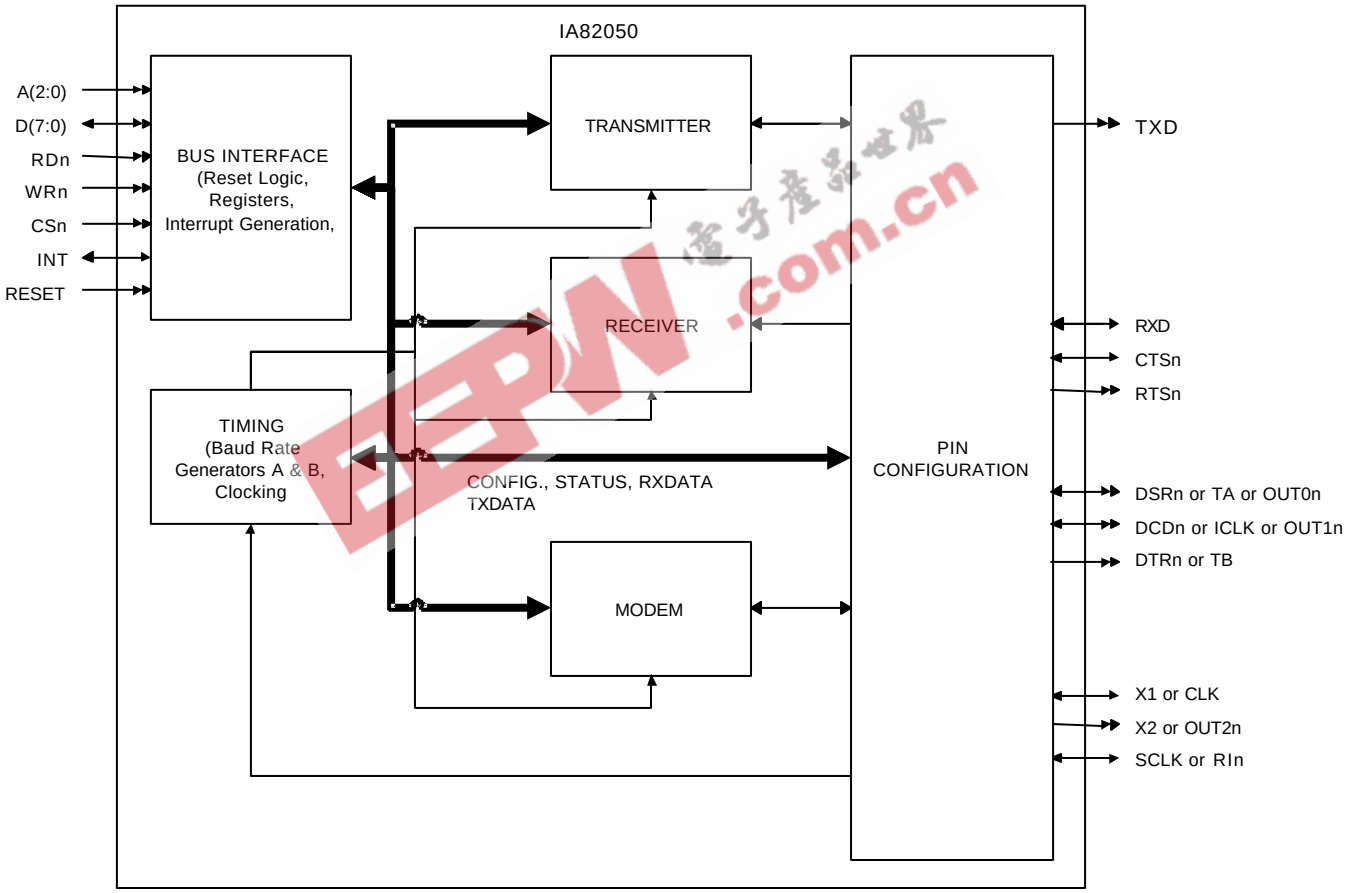
IA82050 Package Pinout



DESCRIPTION

The IA82050 is an asynchronous serial controller that provides a CPU interface to one transmit and one receive channel. It is Form, Fit, and Function compatible with the Intel® 82050 and 82510. Configuration registers are used to control the serial channel, interrupts, and modes of operation. The CPU controls this device via address and data lines with read/write control. The CPU also uses this interface to read and write data to receive and transmit data through the serial channel. FIFOs and various serial modes can be used to help off-load the CPU from transmitting and receiving data. An interrupt line provides an indication to the CPU that the device requires servicing. The device can be configured for 8250A/16450 compatibility.

Functional Block Diagram



Functional Overview

Transmitter

The Transmit function consists of a 4 × 11 bit FIFO, and a Transmit Engine. The 4 × 11 FIFO is configurable as any depth between one and four words inclusive. The transmit engine is responsible for reading the data out of the FIFO and placing it in the proper order on the TXD pin. The transmit engine is highly configurable to be compatible with numerous formats, including 16450 and 8250 modes of communication. Transmit Communication parameters that can be programmed include:

- Parity modes
- Stop Bits
- Character Length
- FIFO Depth
- Clocking Options
- RTS and CTS modes

See the Register Description for more details.

Receiver

The Receiver function consists of a 4 × 11 configurable FIFO and a Receive Engine. The receive engine is responsible for sampling the data on the RXD input pin, formatting the data, and placing the data in the FIFO. The receive engine is highly configurable with parameters that include:

- Parity modes
- Stop Bits
- Character Length
- FIFO Depth
- Clocking Options
- Address Matching Options
- Control Character Detection
- RTS and CTS modes

See the Register Description for more details.

Bus Interface

The Bus Interface is a simple interface that allows a micro-processor or micro-controller to read and write the IA82050 Registers. It consists of the following I/O lines:

- A0, A1, A2 : 3 Bit Address
- D0-D7 : 8 Bit Data
- RDn: Active Low Read Enable
- WRn: Active Low Write Enable
- CSn: Active Low Chip Select
- INT: Interrupt Output
- RESET: Chip Reset

Register Description

Table 1 – IA82050 Register Summary

Register	ADDR	Bank	DLAB	Mode	Default
ACR0	111	00	X	R/W	00000000
ACR1	101	10	X	R/W	00000000
BACF	001	11	0	R/W	00000100
BAH	001	00	1	R/W	00000000
BAL	000	00	1	R/W	00000010
BANK	010	X	X	W	00000000
BBCF	011	11	X	R/W	10000100
BBH	001	11	1	R/W	00000000
BBL	000	11	1	R/W	00000101
CLCF	000	11	0	R/W	00000000
FLR	100	01	X	R	00000000
FMD	001	10	X	R/W	00000000
GER	001	00	0	R/W	00000000
GIR_BANK	010	X	X	R	00000001
GSR	111	01	X	R	00010010
ICM	111	01	X	W	N/A
IMD	100	10	X	R/W	00001100
LCR	011	00	X	R/W	00000000
LSR	101	00	X	R/W	01100000
MCR	100 100	00 01	X X	R/W W	00000000
MIE	101	11	X	R/W	00001111
MSR	110 110	00 01	X X	R/W R	00000000
PMD	100	11	X	R/W	11111100
RCM	101	01	X	W	N/A
RIE	110	10	X	R/W	00011110
RMD	111	10	X	R/W	00000000
RST	101	01	X	R	00000000
RXDATA	000	00 01	0 X	R	Unknown
RXF	001	01	X	R	Unknown
TCM	110	01	X	W	N/A
TMCR	011	01	X	W	N/A
TMD	011	10	X	R/W	00000000
TMIE	110	11	X	R/W	00000000
TMST	011	01	X	R	00110000
TXDATA	000	00 01	0 X	W	N/A
TXF	001	01	X	W	N/A

AC/DC Parameters

Absolute maximum ratings:

Supply Voltage, V_{DD}……..…-0.3V to +6.0V
Input Voltage, V_{IN}…….-0.3V to V_{DD} +0.3V
Input Pin Current, IIN……..±10 mA, 25° C
Operating Temperature Range……..-40° C to +85°C
Ambient temperature under bias.....……..-40°C to +85°C *
Storage temperature.....….....….- 55°C to +150°C
Lead Temperature…….+300°C, 10 sec.
Power dissipation.....155 mW, 125°C, 25MHz, 15% Toggle

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Operating the device beyond the conditions indicated in the "recommended operating conditions" section is not recommended. Operation at the "absolute maximum ratings" may adversely affect device reliability.

* The input and output parametric values in section VII-B, parts 1, 2, and 3, are directly related to ambient temperature and DC supply voltage. A temperature or supply voltage range other than those specified in the Operating Conditions above will affect these values and part performance is not guaranteed by innovASIC.

DC Characteristics

Symbol	Parameter	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage	(1)	-0.5	0.7	V
V_{IH1}	Input High Voltage-Cerdip	(1)	2.1	V_{DD}+.07	V
V_{IH2}	Input High Voltage-LCC	(2)	2.1	V_{DD}+.07	V
V_{OL}	Output Low Voltage	(2), (8)		0.4	V
V_{OH}	Output High Voltage	(3), (8)	2.4		V
I_{LI}	Input Leakage Current	(4)		±1	µA
I_{LO}	3-State Leakage Current	(5)		±1	µA
I_{CC}	Power Supply Current	(6)		1.12	mA/MHz
I_{PU}	Strapping Pullup Resistor	(12)	-283	-137	A
I_{STBY}	Standby Supply Current	(9)		100	µA
I_{OHR}	RTSn, DTRn Strapping Current	(10)		1.92	mA
I_{OLR}	RTSn, DTRn Strapping Current	(11)	N/A		mA
C_{IN}	Input Capacitance	(7)		5	pF
C_{IO}	I/O Capacitance	(7)		6	pF
C_{XTAL}	X1, X2 Load			6	pF

NOTES:

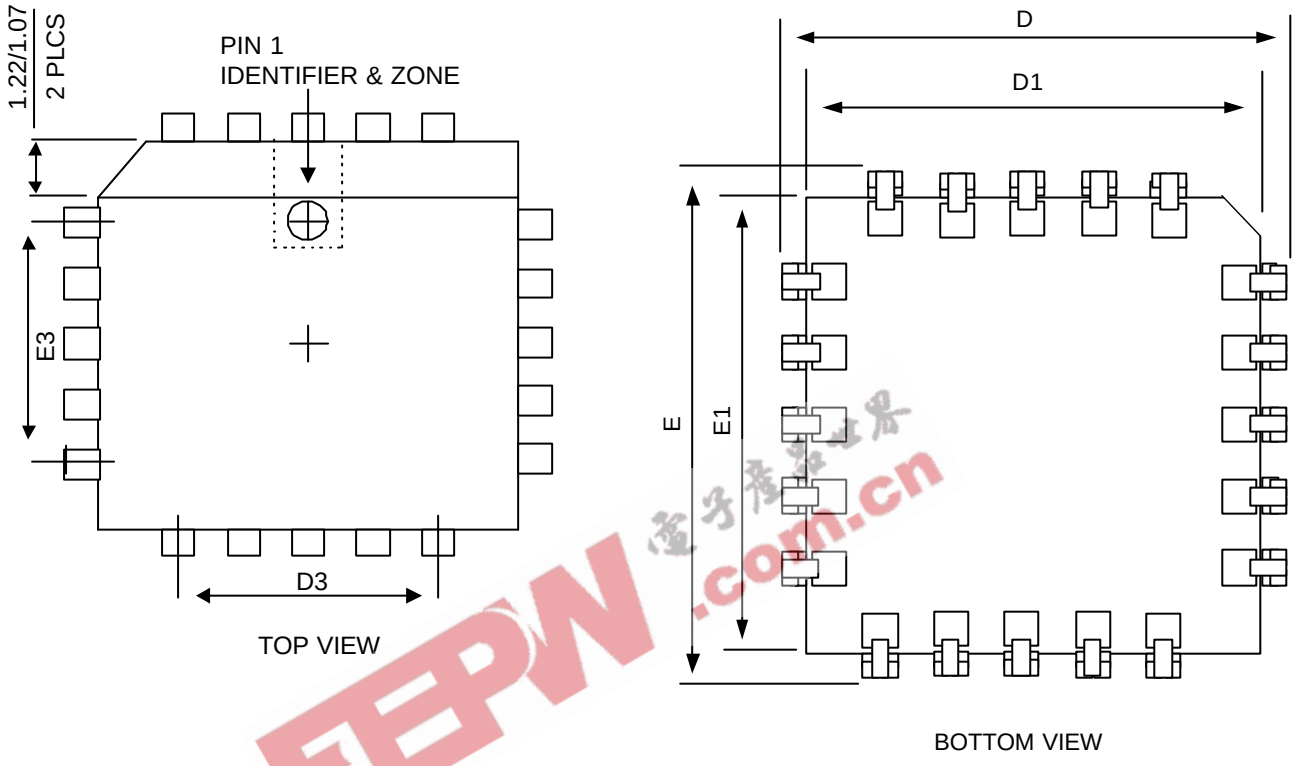
1. Does not apply to CLK/X1 pin, when configured as crystal oscillator input (X1).
2. @ I_{OL} = 1.92 mA
3. @ I_{OH} = 1.92 mA
4. $0 < V_{IN} < V_{CC}$.
5. $0.4V < V_{OUT} < V_{CC} - 0.4V$
6. V_{DD} = 5.5V, V_{IL} = 0.7V (max), V_{IH} = V_{DD} - 0.7V (min), Typ. Val = 1.12 mA/MHz (Not Tested), Ext. 1X CLK, $I_{OL} = I_{OH} = 0$.
7. Freq. = 1MHz.
8. Does not apply to OUT2/X2 pin, when configured as crystal oscillator output (X2).
9. Freq. = 1MHz. But, input clock not running. Static IDD current is exclusive of input/output drive requirements and is measured with the clocks stopped and all inputs tied to VDD or VSS, configured to draw minimum current.
10. Applies only during hardware reset for clock configuration options. Strapping current for logic HIGH.
11. Applies only during hardware reset for clock configuration options. Strapping current for logic LOW
12. Inputs (RTSn, DTRn, TB) with Pullups tested @ V_{in} = 0.0V V_{DD} = 5.5V

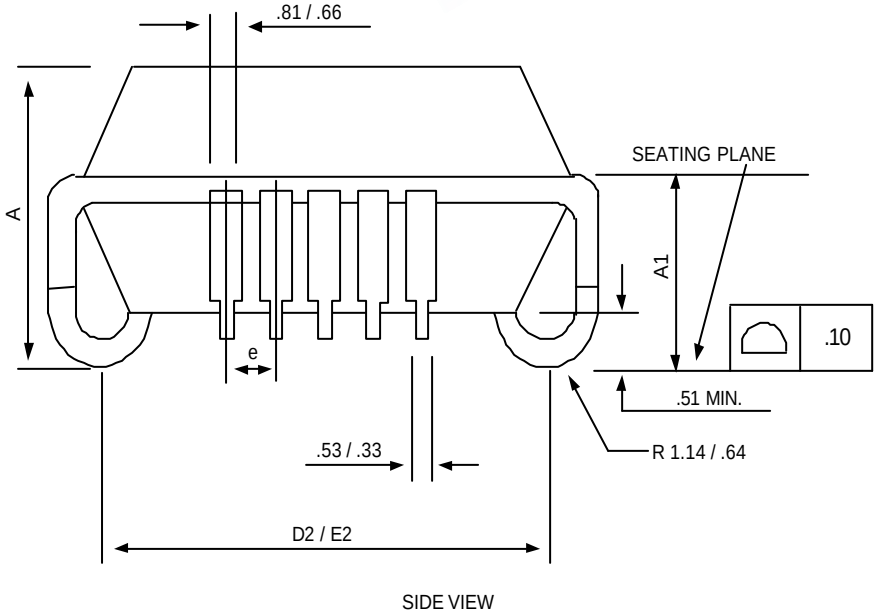
AC Characteristics

Parameter	Min	Max	Notes
CLK period	54 ns	250 ns	Divide by Two
CLK period	54 ns	108 ns	No Divide by
CLK Low Time	25 ns		
CLK High Time	25 ns		
CLK Rise Time		10 ns	Divide by Two Measured between 0.3 * VDD and 0.7 * VDD
CLK Fall Time		10 ns	Divide by Two Measured between 0.3 * VDD and 0.7 * VDD
CLK Rise Time		15 ns	No Divide by
CLK Fall Time		15 ns	No Divide by
Crystal Frequency	1 Mhz	20 Mhz	
Reset Width	8 * Clock Period		
RTS/DTR Low Setup to Reset inactive	6 * Clock Period		
RTS/DTR Low Hold after Reset inactive		Clock Period – 20 ns	
RDn Active Width	2* clock period + 65 ns		
Address/CSn Setup Time to RDn Active	7 ns		
Address/CSn Hold after RDn Inactive	0 ns		
RDn or WRn Inactive to Active Delay	Clock Period + 15 ns		
Data Out Float Delay after RDn Inactive		40 ns	
WRn Active Width	2 * Clock Period + 15 ns		
Address CSn Setup Time to WRn Active	7 ns		
Address and CSn hold Time after WRn	0 ns		
Data in Setup Time to WRn Inactive	90 ns		
Data In Hold Time after WRn Inactive	12 ns		
SCLK Period	216 ns		16x Clocking Mode
SCLK Period	3500 ns		1x Clocking Mode
RXD Setup Time to SCLK High	250 ns		
RXD Hold Time after SCLK High	250 ns		
TXD Valid after SCLK Low		170 ns	
TXD Delay after RXD		170 ns	Remote Loopback

Packaging Information

PLCC Package

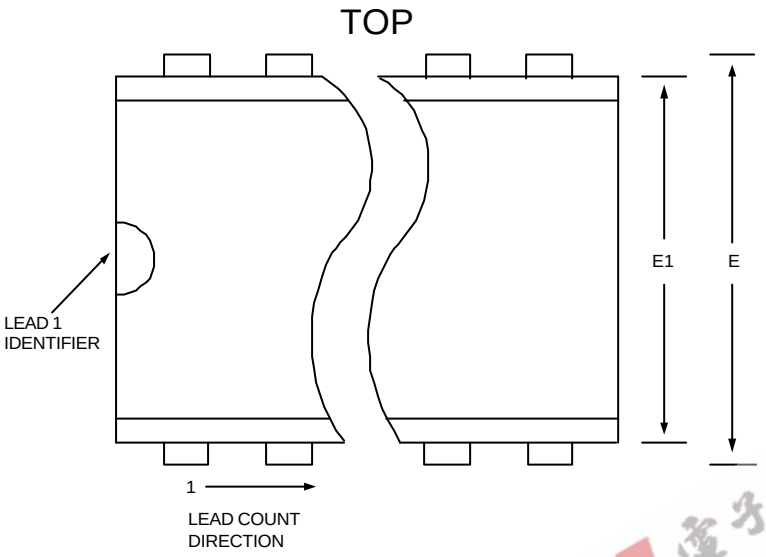


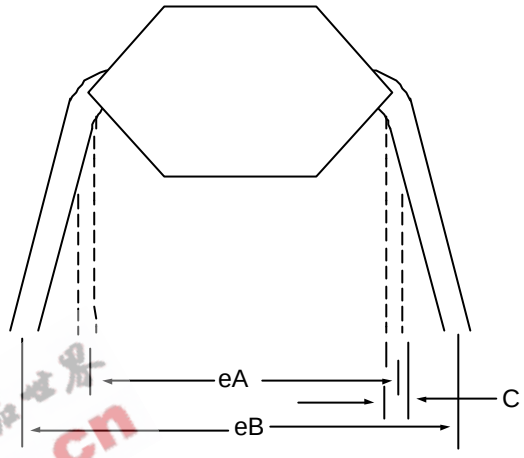


LEAD COUNT

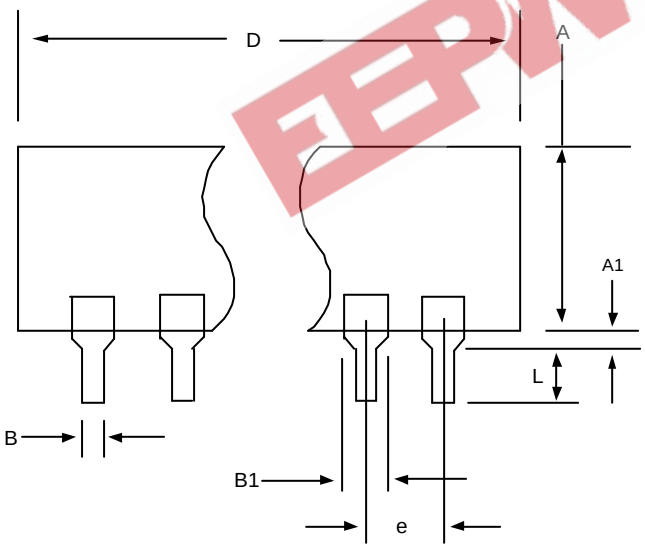
Symbol	28 (in Millimeters)	
	MIN	MAX
A	4.20	4.57
A1	2.29	3.04
D1	11.43	11.58
D2	9.91	10.92
D3	7.62 BSC	
E1	11.43	11.58
E2	9.91	10.92
E3	7.62 BSC	
e	1.27 BSC	
D	12.32	12.57
E	12.32	12.57

PDIP Package





SIDE VIEW (WIDTH)



SIDE VIEW (LENGTH)

Lead Count

Symbol	28 (in Inches)	
	MIN	MAX
A	-	.200
A1	.015	-
B	.015	.020
B1	.050	.070
C	.008	.012
D	1.380	1.470
E	.580	.610
E1	.520	.560
e	.100 TYP	
eA	.580	-
eB	-	.686
L	.100 MIN	
B2	-	-
S	-	-

Ordering Information

Production Version 01

Order Number	Environment	Package Type
IA82050-PDW28I-01	Industrial	28 Lead Plastic DIP, 600 mil wide
IA82050-PDW28C-01	Commercial	
IA82050-PLC28I-01	Industrial	28 Lead Plastic Leaded Chip Carrier
IA82050-PLC28C-01	Commercial	

ERRATA

Production Version 01

1. **Issue**: Issuing more than one command via the Receive Command register (RCM) may result in an unintended lock of the RX FIFO.

   Workaround: If multiple commands via the RCM are required, execute them individually.

2. **Issue**: In semi-automatic and automatic transmit mode, RTS will assert at the same time as the beginning of the start bit on TXD. If RTS is used to turn on the TXD line driver, the width of the start bit could be distorted.

   Workaround: Manual assertion of RTS and initiation of the transmit will avoid this issue.