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**PRELIMINARY**

# ICS840014I FEMTOCLOCKS™ CRYSTAL-TO- LVCMOS/LVTTL FREQUENCY SYNTHESIZER

## GENERAL DESCRIPTION



The ICS840014I is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Fibre Channel reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. This device uses a 26.5625MHz, 18pF parallel resonant crystal to synthesize 106.25MHz. Using FemtoClock's™ ultra-low phase noise VCO technology, the ICS840014I can achieve 1ps or lower typical random rms phase jitter, easily meeting Fibre Channel jitter requirements. The ICS840014I is packaged in a small 20-pin TSSOP package.

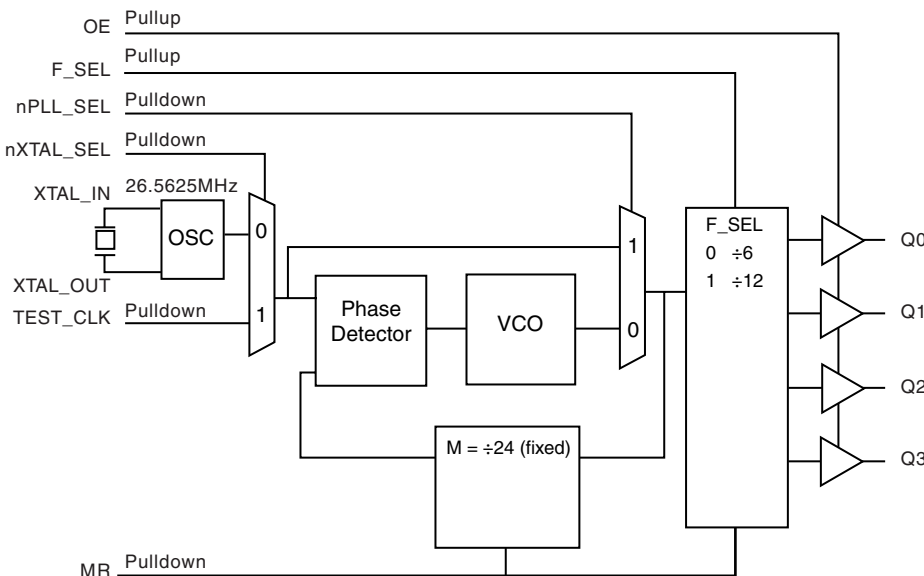
## FEATURES

- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS single-ended input
- Output frequency: 106.25MHz or 53.125MHz
- RMS phase jitter @ 106.25MHz (637KHz - 5MHz): 0.72ps (typical)
- Output supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V  
2.5V/2.5V
- -40°C to 85°C ambient operating temperature

FREQUENCY SELECT FUNCTION TABLE

Input Frequency	Inputs				Output Frequency Range
	F_SEL1	M Divider Value	N Divider Value	M/N Ratio Value	
26.5625	0	24	6	4	106.25
26.5625	1	24	12	2	53.125

## BLOCK DIAGRAM



## PIN ASSIGNMENT

F_SEL	1	20	nc
nc	2	19	GND
nXTAL_SEL	3	18	Q0
TEST_CLK	4	17	Q1
OE	5	16	VDDO
MR	6	15	Q2
nPLL_SEL	7	14	Q3
VDDA	8	13	GND
nc	9	12	XTAL_IN
VDD	10	11	XTAL_OUT

### ICS840014I

#### 20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm  
package body  
**G Package**  
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



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**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	F_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2, 9, 20	nc	Unused		No connect.
3	nXTAL_SEL	Input	Pulldown	Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inpus. LVCMOS/LVTTL interface levels.
4	TEST_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL clock input.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the opututs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
8	V <sub>DDA</sub>	Power		Analog supply pin.
10	V <sub>DD</sub>	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
13, 19	GND	Power		Power supply ground.
14, 15, 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
16	V <sub>DDO</sub>	Power		Output supply pin.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V		TBD		pF
		V <sub>DD</sub> , V <sub>DDA</sub> = 3.465V, V <sub>DDO</sub> = 2.625V		TBD		pF
		V <sub>DD</sub> , V <sub>DDA</sub> , V <sub>DDO</sub> = 2.625V		TBD		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ
R <sub>OUT</sub>	Output Impedance			15		Ω



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**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			75		mA
$I_{DDA}$	Analog Supply Current			6		mA
$I_{DDO}$	Output Supply Current			5		mA

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			75		mA
$I_{DDA}$	Analog Supply Current			6		mA
$I_{DDO}$	Output Supply Current			4		mA

**TABLE 3C. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			70		mA
$I_{DDA}$	Analog Supply Current			6		mA
$I_{DDO}$	Output Supply Current			4		mA



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**TABLE 3D. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	nPLL_SEL, nXTAL_SEL, F_SEL, OE, MR	2		$V_{DD} + 0.3$	V
		TEST_CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	nPLL_SEL, nXTAL_SEL, F_SEL, OE, MR	-0.3		0.8	V
		TEST_CLK	-0.3		1.3	V
$I_{IH}$	Input High Current	F_SEL, OE	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		5	$\mu\text{A}$
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	F_SEL, OE	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150		$\mu\text{A}$
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-15		$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1	$V_{DDO} = 3.3V \pm 5\%$	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1	$V_{DDO} = 3.3V$ or $2.5V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information, Output Load Test Circuit.

**TABLE 4. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pf parallel resonant crystal.



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**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			106.25		MHz
				53.125		MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3			TBD		ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	106.25MHz (637KHz - 5MHz)		0.75		ps
		53.125MHz (637KHz - 5MHz)		0.63		ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		550		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.  
Measured at  $V_{DDO}/2$ .

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			106.25		MHz
				53.125		MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3			TBD		ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	106.25MHz (637KHz - 5MHz)		0.72		ps
		53.125MHz (637KHz - 5MHz)		0.63		ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		500		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.  
Measured at  $V_{DDO}/2$ .

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5C. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency			106.25		MHz
				53.125		MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 3			TBD		ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 2	106.25MHz (637KHz - 5MHz)		0.72		ps
		53.125MHz (637KHz - 5MHz)		0.67		ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		500		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.  
Measured at  $V_{DDO}/2$ .

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

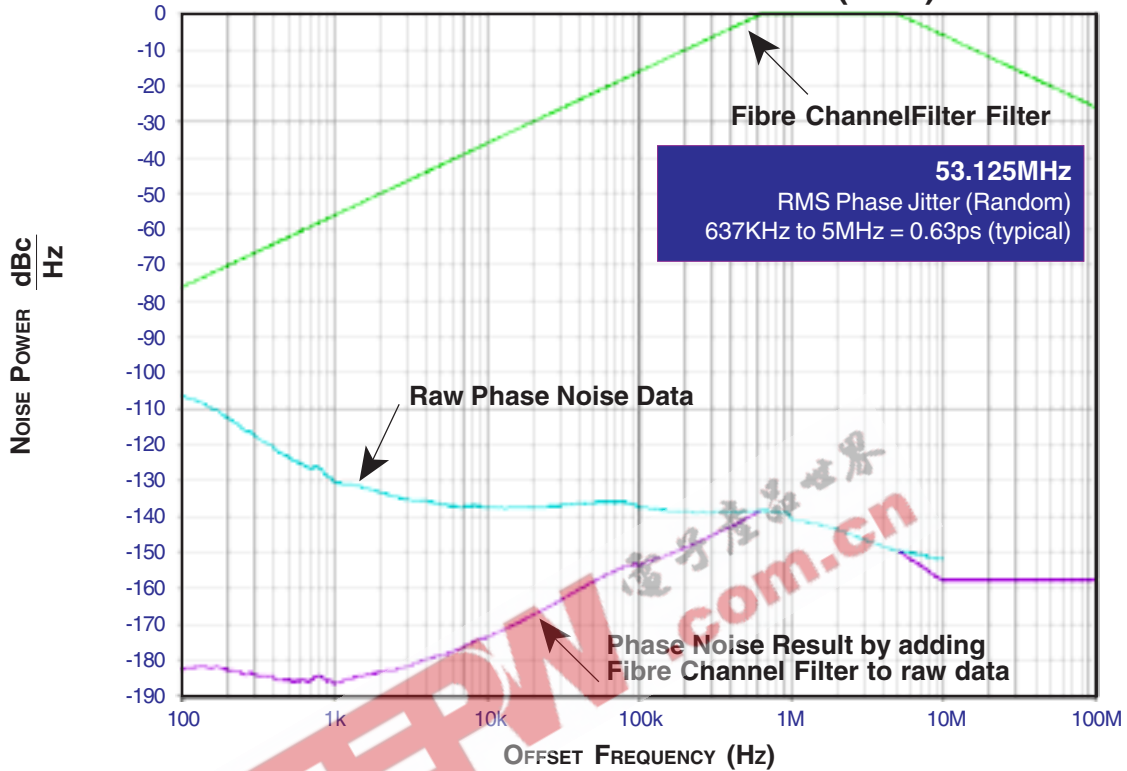


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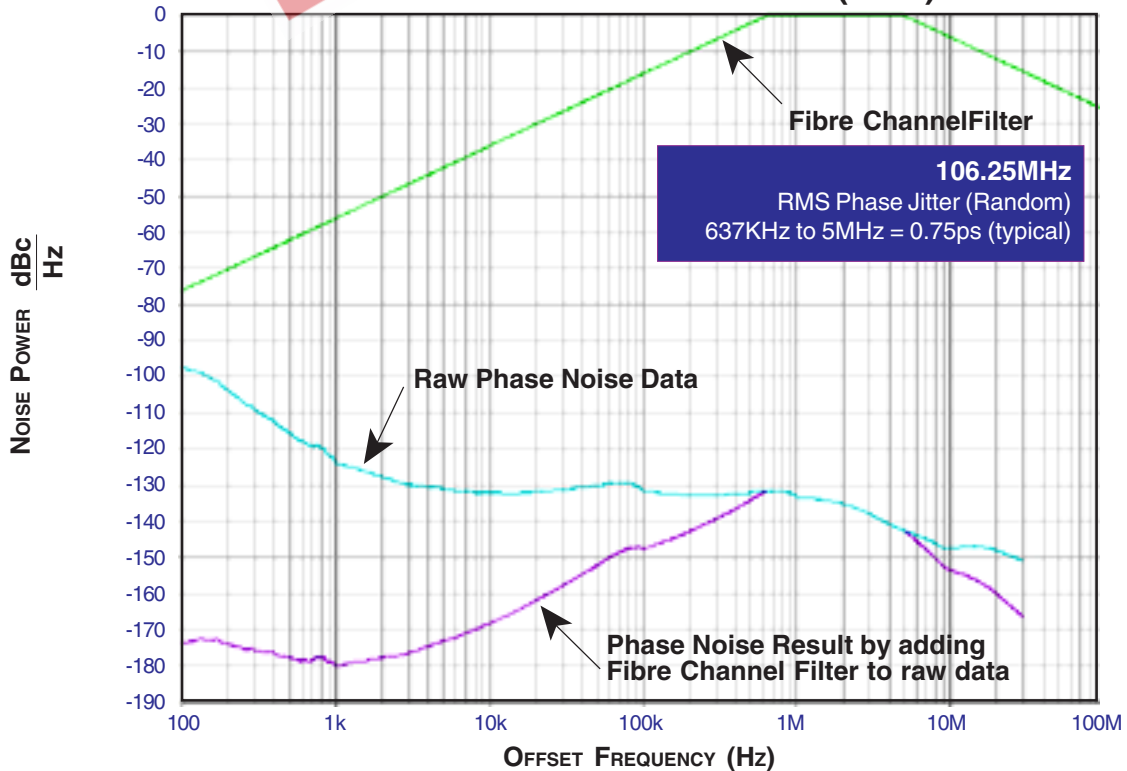
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**TYPICAL PHASE NOISE AT 53.125MHz (3.3V)**



**TYPICAL PHASE NOISE AT 106.25MHz (3.3V)**



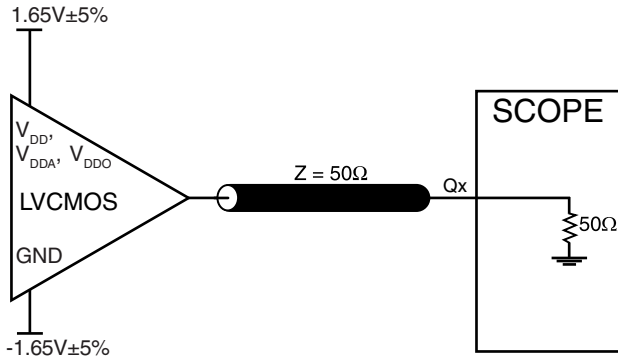


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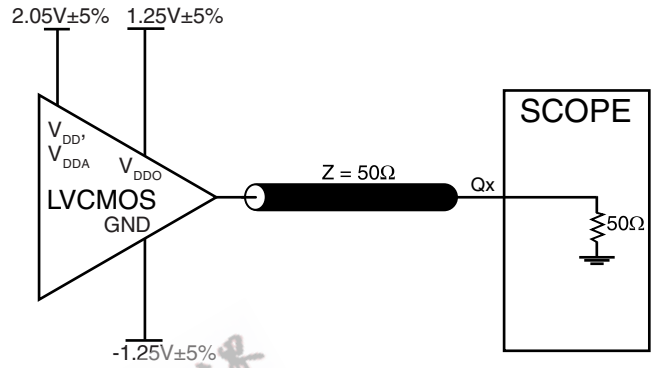
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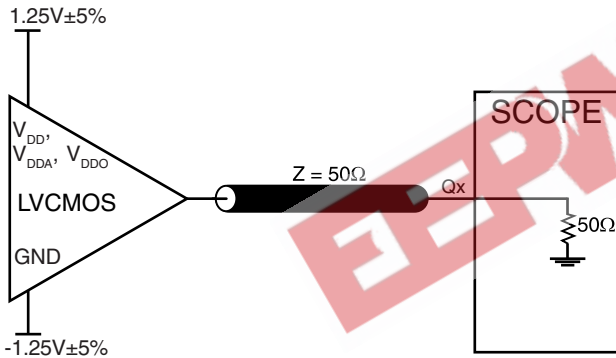
**PARAMETER MEASUREMENT INFORMATION**



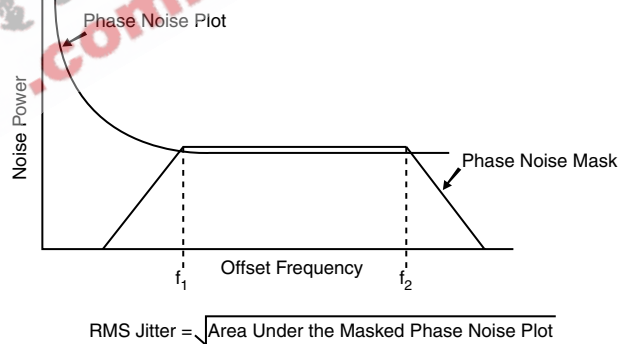
**3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT**



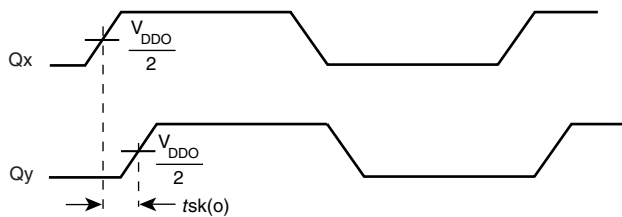
**3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



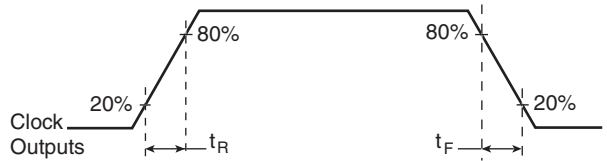
**2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT**



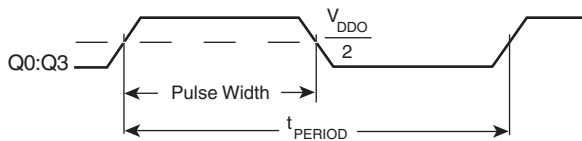
**RMS PHASE JITTER**



**OUTPUT SKEW**



**OUTPUT RISE/FALL TIME**



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**





## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840014I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each  $V_{DDA}$ .

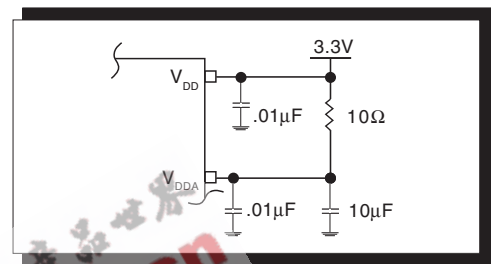


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS840014I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were

determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

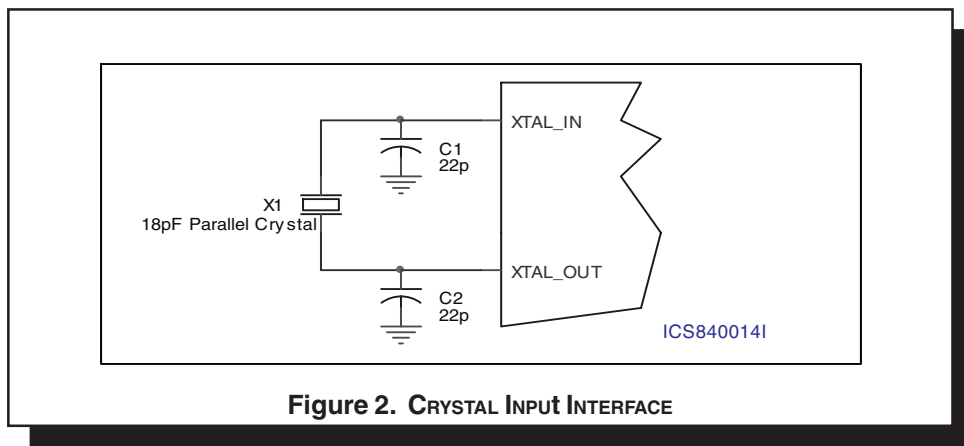


Figure 2. CRYSTAL INPUT INTERFACE





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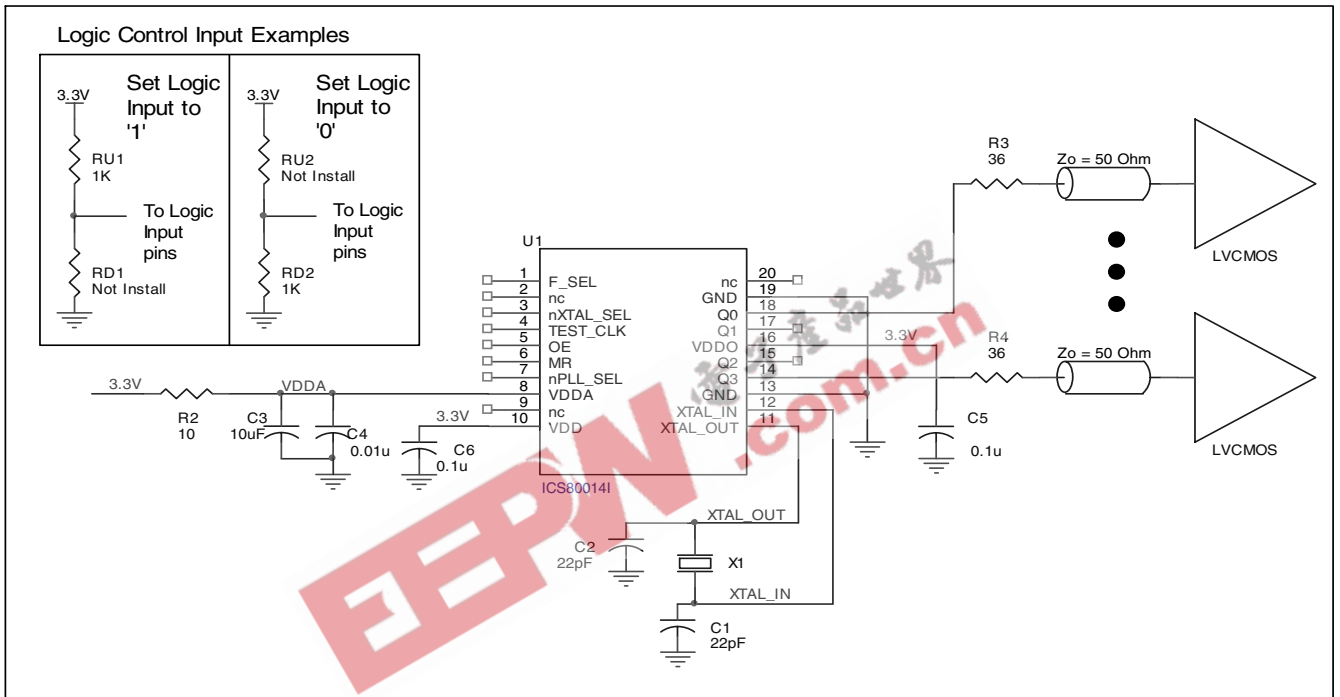
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**LAYOUT GUIDELINE**

Figure 3 shows a schematic example of the ICS840014I. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 26.5625MHz crystal is used. The

C1=22pF and C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. 1KΩ pullup or pulldown resistors can be used for the logic control input pins.



**FIGURE 3. ICS840014I SCHEMATIC EXAMPLE**

**RELIABILITY INFORMATION**

**TABLE 6.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 20 LEAD TSSOP**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TRANSISTOR COUNT**

The transistor count for ICS840014I is: 3085

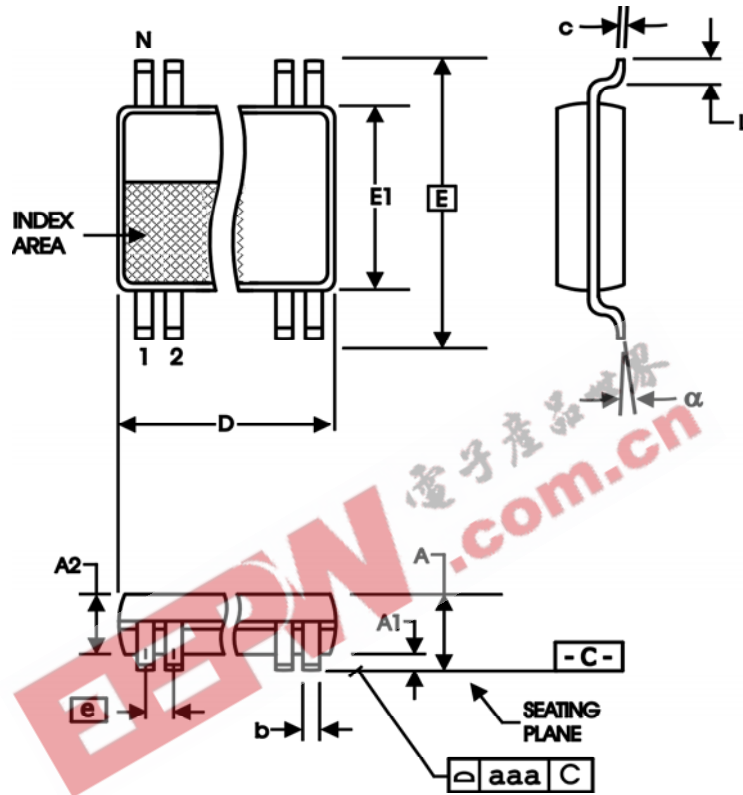


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**PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP**



**TABLE 7. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



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TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS840014AGI	TBD	20 Lead TSSOP	72 per tube	-40°C to 85°C
ICS840014AGIT	TBD	20 Lead TSSOP on Tape and Reel	2500	-40°C to 85°C

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