PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840001-32

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840001-32 is a two output LVCMOS/LVTTL Synthesizer and is a member of the HiPerClocks™ family of high performance devices from ICS. The device uses a 40MHz crystal to provide a 40MHz reference clock output and to synthesize a 100MHz or 106.25MHz output. The ICS840001-32 has excellent <1ps phase jitter performance over the 637kHz – 5MHz integration range. The ICS840001-32 is packaged in a 3mm x 3mm 16-pin VFQFN, making it ideal for use on space constrained boards.

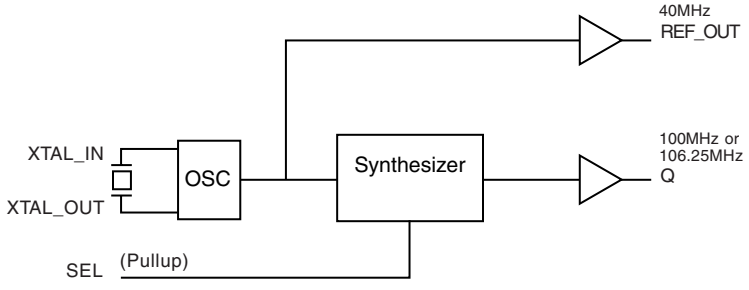
FEATURES

- One LVCMOS/LVTTL output, 15Ω typical output impedence and one reference clock output
- 40MHz, 10pF parallel resonant crystal
- Output frequencies: 100MHz or 106.25MHz
- RMS phase jitter @ 106.25MHz, using a 40MHz crystal (637kHz - 5MHz): 0.78ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Availabe in both standard and lead-free RoHS-compliant packages

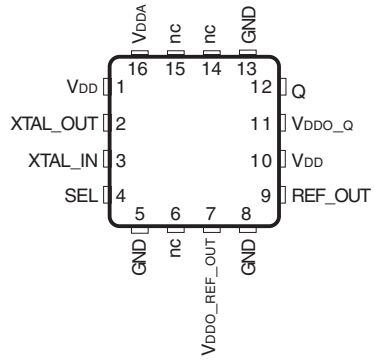
FUNCTION TABLE

Inputs		Outputs	
Crystal Frequency (MHz)	SEL Input	Q Output Frequency (MHz)	REF_OUT Frequency (MHz)
40	0	100	40
40	1	106.25	40

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840001-32
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 10	V_{DD}	Power		Core supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
4	SEL	Input	Pullup	Select input. LVCMOS/LVTTL interface levels.
5, 8, 13	GND	Power		Power supply ground.
6, 14, 15	nc	Unused		No connect.
7	$V_{DDO\_REF\_OUT}$	Power		Output supply pin for REF_OUT output
9	REF_OUT	Output		Single-ended three-state reference clock output. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
11	V_{DDO_Q}	Power		Output supply pin for Q output.
12	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω typical output impedance.
16	V_{DDA}	Power		Analog supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA}, $V_{DDO\_REF\_OUT}$, V_{DDO_Q} = 3.465V		8		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	51.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_REF\_OUT} = V_{DDO\_Q} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			70		mA
I_{DDA}	Analog Supply Current			25		mA
I_{DDO}	Output Supply Current			12		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_REF\_OUT} = V_{DDO\_Q} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO\_x}/2$ See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 4. CRYSTAL CHARACTERISTICS

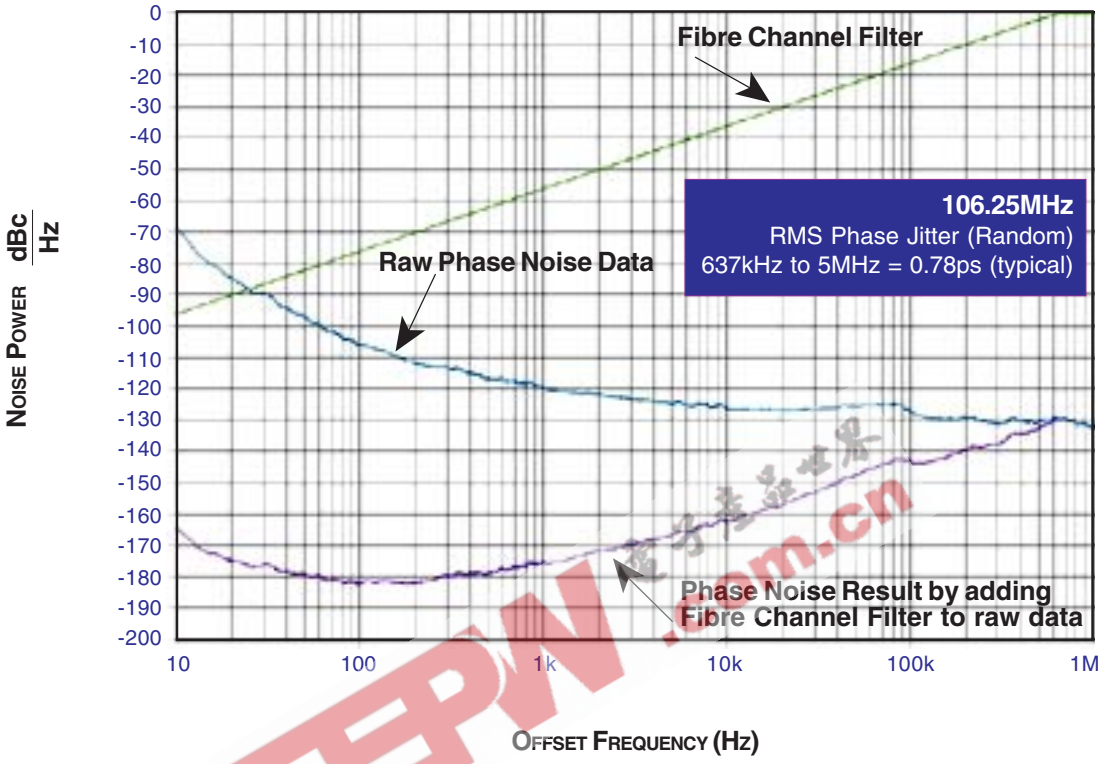
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			40		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level			10	100	µW

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_REF\_OUT} = V_{DDO\_Q} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

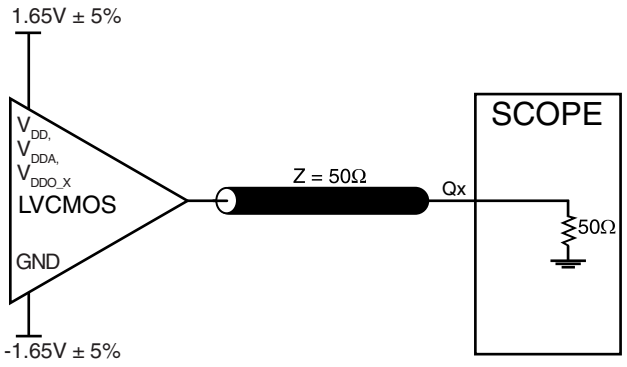
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	REF_OUT	f_SEL = 0		100		MHz
		Q	f_SEL = 1		106.25		MHz
*t*jit(Ø)	RMS Phase Jitter (Random)		100MHz, Integration Range: 637kHz to 5MHz		0.83		ps
			106.25MHz, Integration Range: 637kHz to 5MHz		0.78		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		900		ps
odc	Output Duty Cycle				50		%

All parameters are characterized @ 100MHz and 106.25MHz.

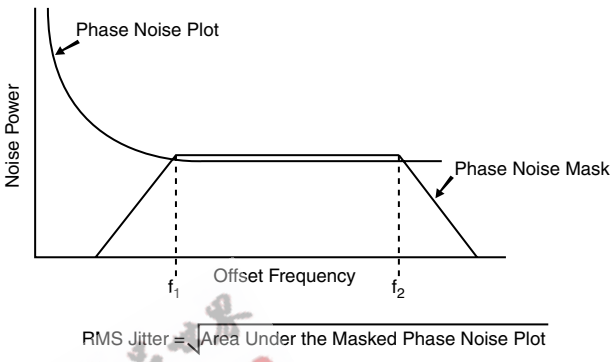
TYPICAL PHASE NOISE AT 106.25MHZ



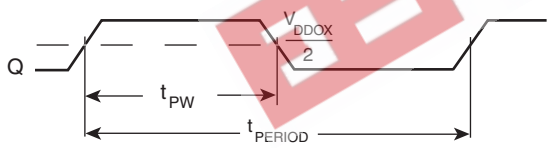
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

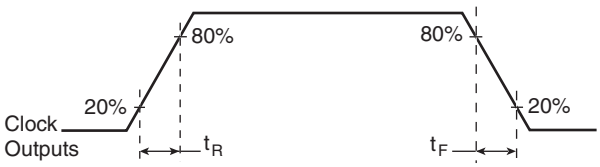


RMS PHASE JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840001-32 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO_X} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

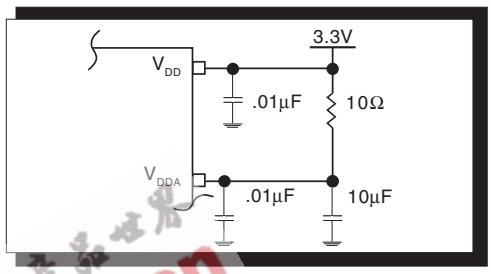


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840001-32 has been characterized with 10pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 40MHz, 10pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

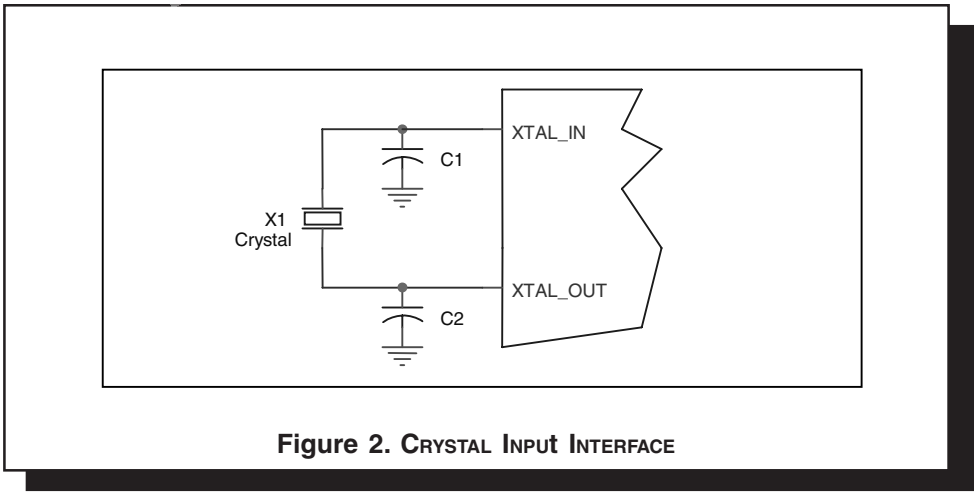


Figure 2. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS840001-32 is: 2121

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

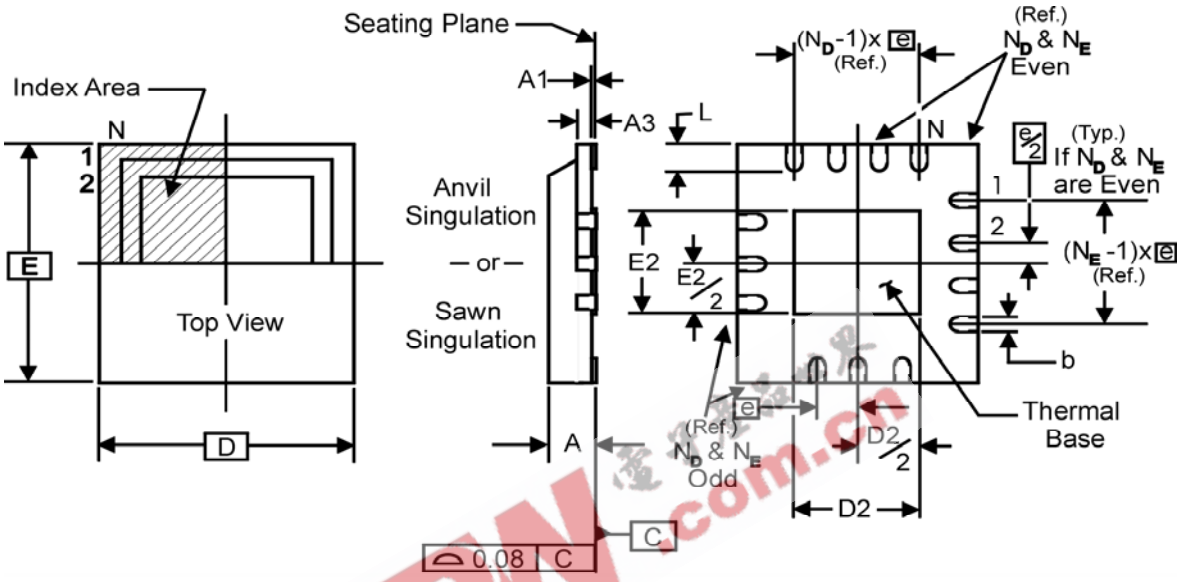


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840001CK-32	1C32	16 Lead VFQFN	tray	0°C to 70°C
ICS840001CK-32T	1C32	16 Lead VFQFN	2500 tape & reel	0°C to 70°C
ICS840001CK-32LF	TBD	16 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS840001CK-32LFT	TBD	16 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS complaint.