PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840008-01

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

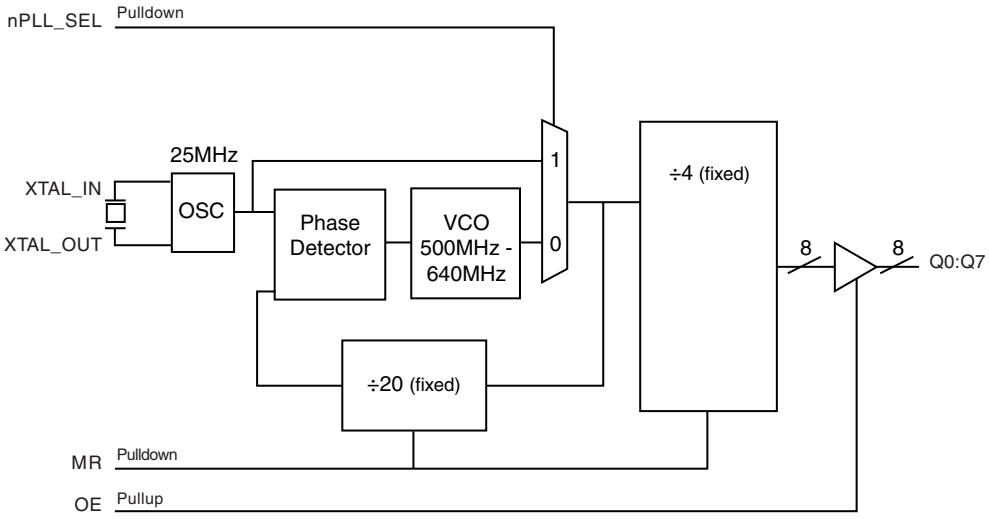
GENERAL DESCRIPTION

The ICS840008-01 is an 8 output LVCMOS/LVTTL Synthesizer designed to generate 125MHz for Gigabit Ethernet applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The ICS840008-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Gigabit Ethernet jitter requirements. The ICS840008-01 is packaged in a small 24-pin SSOP package.

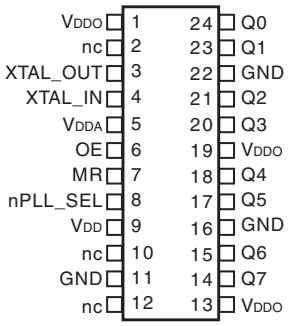
FEATURES

- Eight LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Output frequency range: 125MHz - 160MHz
- Crystal oscillator interface, 25MHz - 32MHz crystal
- VCO range: 500MHz - 640MHz
- RMS phase jitter (1.875MHz - 20MHz): 0.52ps (typical)
- Output skew: 150ps (maximum) (design target)
- Voltages supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840008-01
24-Lead SSOP, 150MIL
3.9mm x 8.65mm x 1.5mm
package body
R Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 13, 19	V_{DDO}	Power		Output supply pins.
2, 10, 12	nc	Unused		No connect.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
5	V_{DDA}	Power		Analog supply pin.
6	OE	Input	Pullup	Output enable. LVCMOS/LVTTL interface levels
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	nPLL_SEL	Input	Pulldown	Selects between the PLL and XTAL as the input to the dividers. When HIGH, selects XTAL. When LOW, selects PLL. LVCMOS/LVTTL interface levels.
9	V_{DD}	Power		Core supply pin.
11, 16, 22	GND	Power		Power supply ground.
14, 15, 17, 18, 20, 21, 23, 24	Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Ouput		Single-ended outputs.15Ω impedance. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DDO} = 3.63V		TBD		pF
		V_{DDO} = 2.625V		TBD		pF
		V_{DDO} = 1.89V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.63V or 2.625V		15		Ω
		V_{DDO} = 1.89V		TBD		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	73.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±10\%$, $V_{DDO} = 3.3V±10\%$ OR $2.5V±5\%$ OR $1.8V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{DDO}	Output Supply Voltage		2.97	3.3	3.63	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current			65		mA
I_{DDA}	Analog Supply Current			5		mA
I_{DDO}	Output Supply Current			4		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V±5\%$, $V_{DDO} = 2.5V±5\%$ OR $1.8V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current			60		mA
I_{DDA}	Analog Supply Current			5		mA
I_{DDO}	Output Supply Current			4		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OE, MR, PLL_SEL	V_{DD} = 3.3V ±10%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OE, MR, PLL_SEL	V_{DD} = 3.3V ±10%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	MR, nPLL_SEL	V_{DD} = 3.3V ±10%			150	µA
			V_{DD} = 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V ±10%			5	µA
			V_{DD} = 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	MR, nPLL_SEL	V_{DD} = 3.3V ±10%	-5			µA
			V_{DD} = 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V ±10%	-150			µA
			V_{DD} = 2.5V ± 5%	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 10%	2.6			V
			V_{DDO} = 2.5V ± 5%	1.8			V
			V_{DDO} = 1.8V ± 5%	1.5			V
V_{OL}	Output Low Voltage: NOTE 1		V_{DDO} = 3.3V±10% or 2.5V±5%			0.5	V
			V_{DDO} = 1.8V ± 5%			0.4	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		25		32	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±10\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125		160	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 1.875MHz - 20MHz		0.52		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		550		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot which will follow the AC Characteristics Tables.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±10\%$, $V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125		160	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 1.875MHz - 20MHz		0.53		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		600		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot which will follow the AC Characteristics Tables.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±10\%$, $V_{DDO} = 1.8V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125		160	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 1.875MHz - 20MHz		0.49		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		630		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot which will follow the AC Characteristics Tables.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125		160	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 1.875MHz - 20MHz		0.53		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		600		ps
odc	Output Duty Cycle			50		%

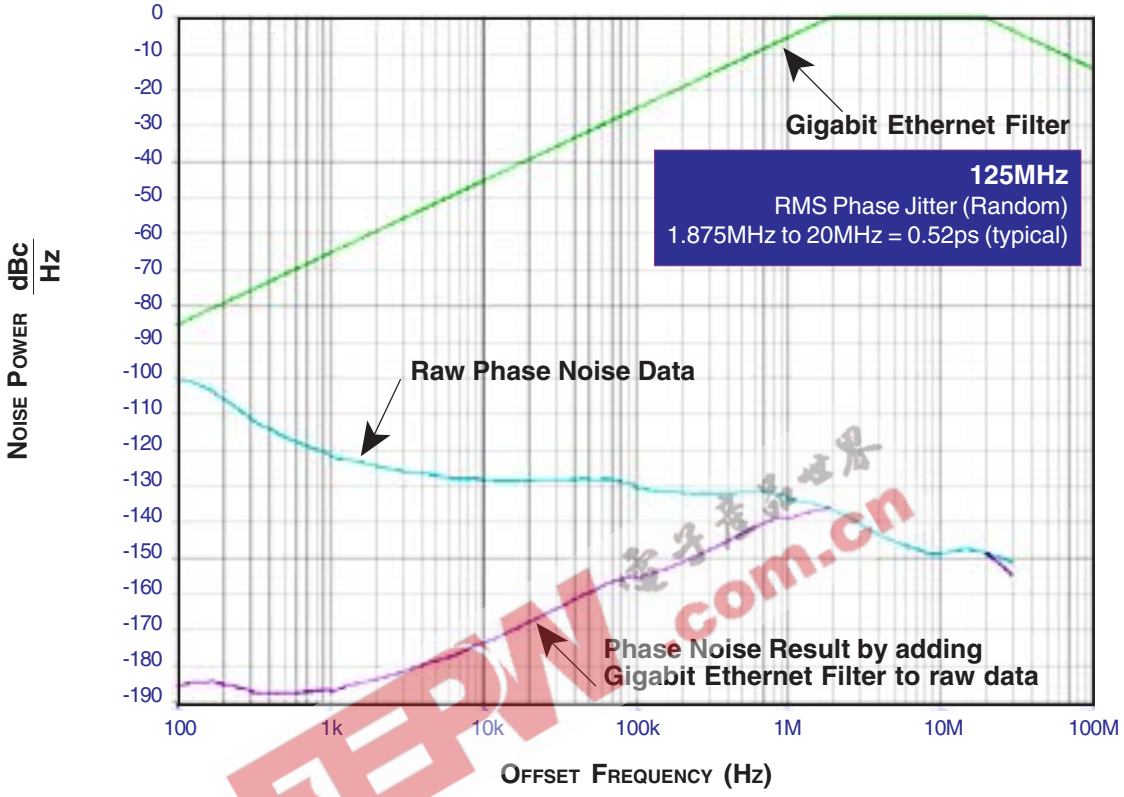
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot which will follow the AC Characteristics Tables.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5E. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V±5\%$, $V_{DDO} = 1.8V±5\%$, $T_A = 0°C$ TO $70°C$

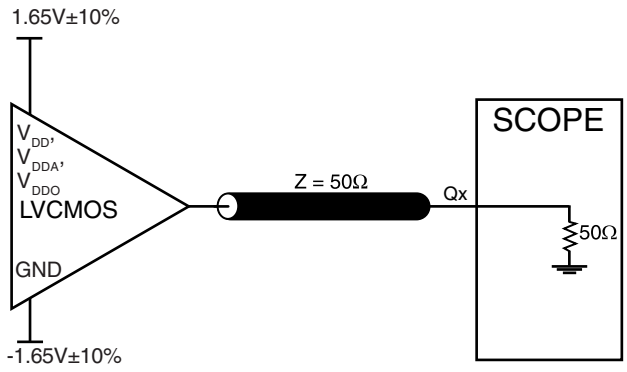
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		125		160	MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	Integration Range: 1.875MHz - 20MHz		0.49		ps
t_L	PLL Lock Time			TBD		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		630		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot which will follow the AC Characteristics Tables.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

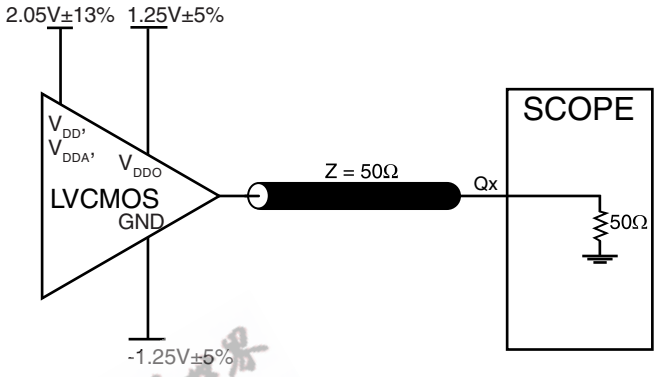
TYPICAL PHASE NOISE AT 125MHZ (3.3V)



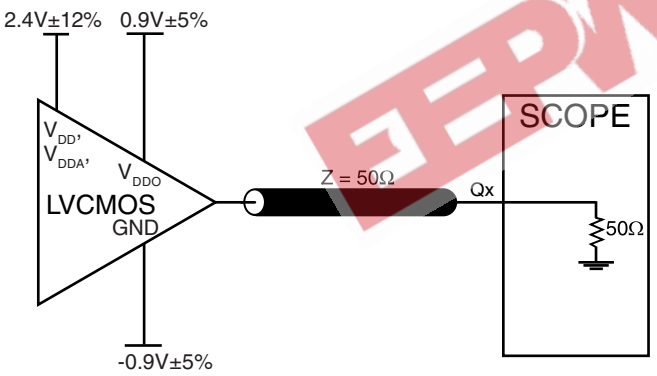
PARAMETER MEASUREMENT INFORMATION



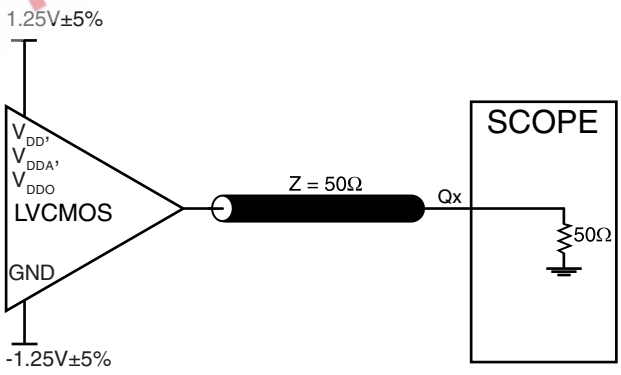
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



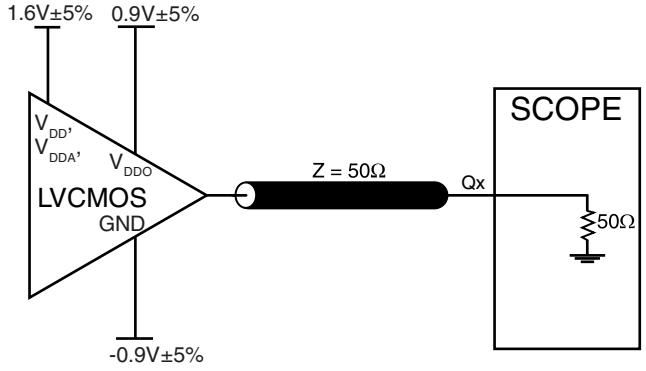
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



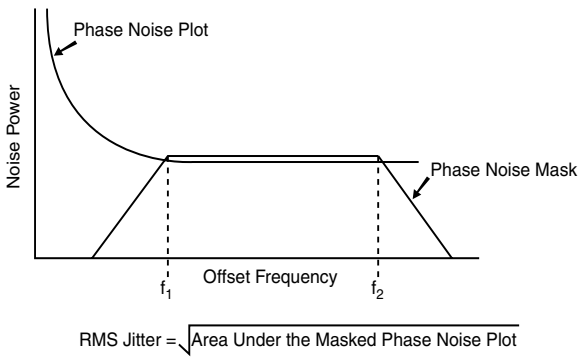
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



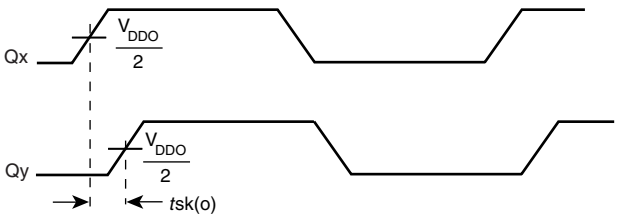
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



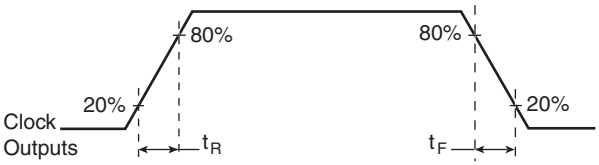
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



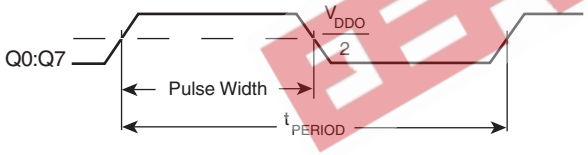
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840008-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

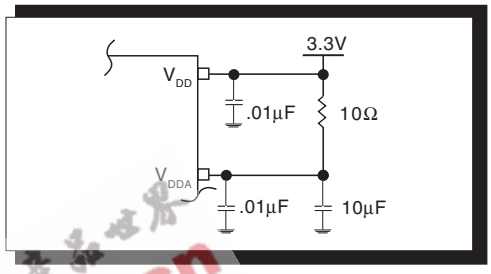


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840008-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

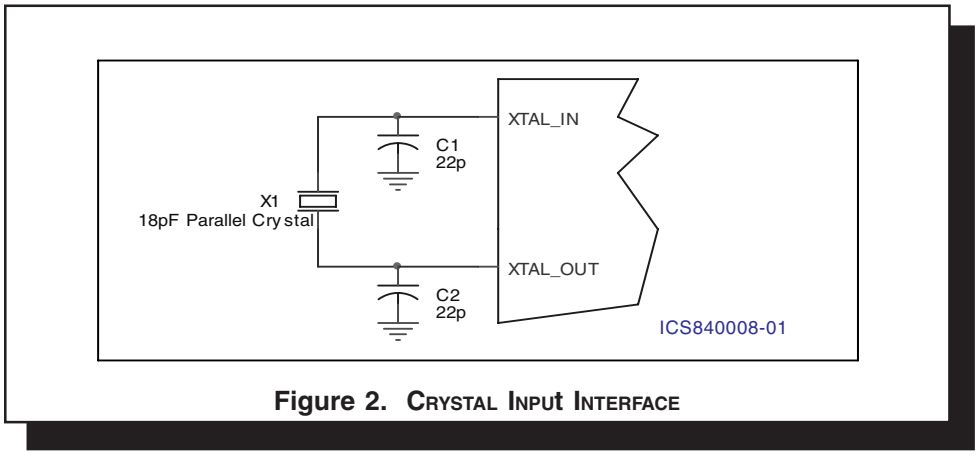


Figure 2. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD SSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	73.1°C/W	65.9°C/W	60.5°C/W

TRANSISTOR COUNT

The transistor count for ICS840008-01 is: 3378

PACKAGE OUTLINE - R SUFFIX FOR 24 LEAD SSOP

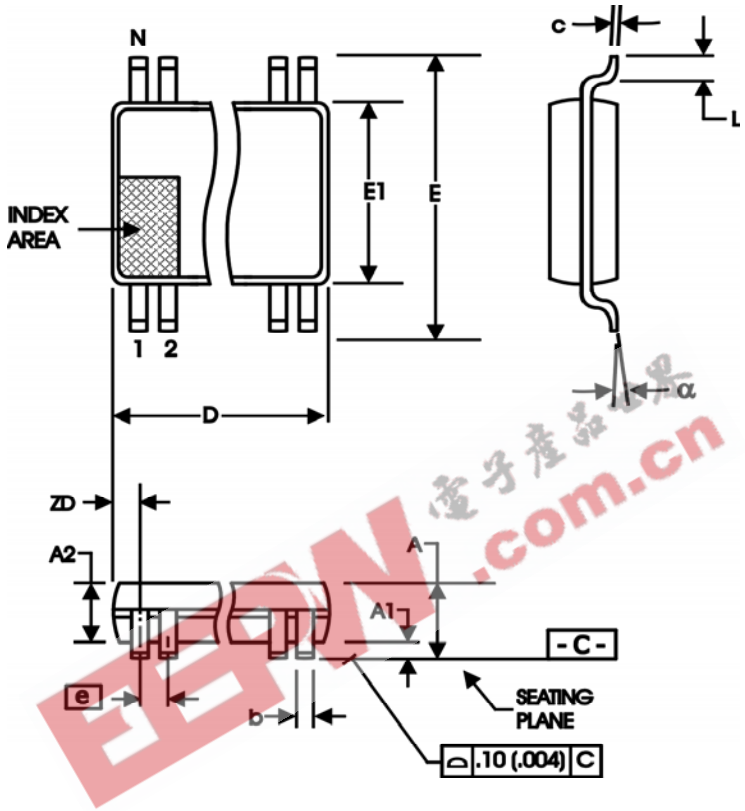


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	1.35	1.75
A1	0.10	0.25
A2		1.50
b	0.20	0.30
c	0.18	0.25
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	0.635 BASIC	
L	0.40	1.27
α	0°	8°
ZD	0.84 REF	

Reference Document: JEDEC Publication 95, MO-137

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840008AR-01	ICS840008AR01	24 Lead SSOP	tube	0°C to 70°C
ICS840008AR-01T	ICS840008AR01	24 Lead SSOP	2500 tape & reel	0°C to 70°C