



GENERAL DESCRIPTION



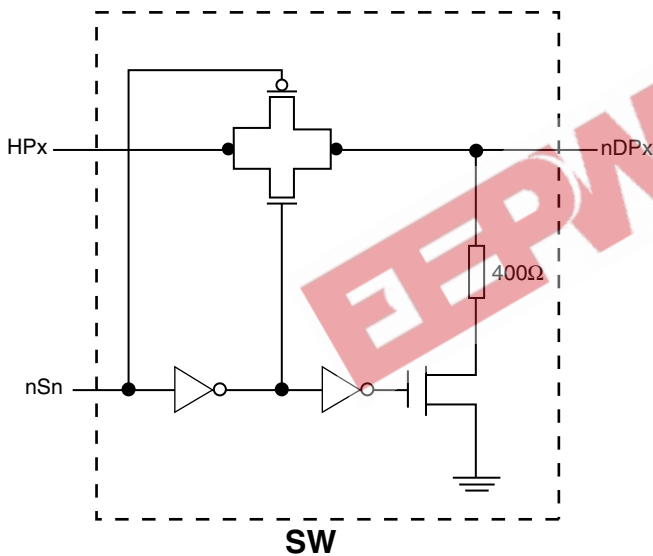
The ICS83840 is a DDR SDRAM MUX and is a member of the HiPerClockSM family of High Performance Clock Solutions from ICS. The device has 10 Host Lines and each host line can be passed to 4 Data Ports. The 10 channels are allocated as follows in the DDR SDRAM application: 8 data lines, 1 strobe line and 1 DQm line. The Host/Data Ports are compatible with single-ended SSTL-2 and the device operates from a 2.5V supply.

Guaranteed low output skew makes the ICS83840 ideal for demanding applications which require well defined performance and repeatability.

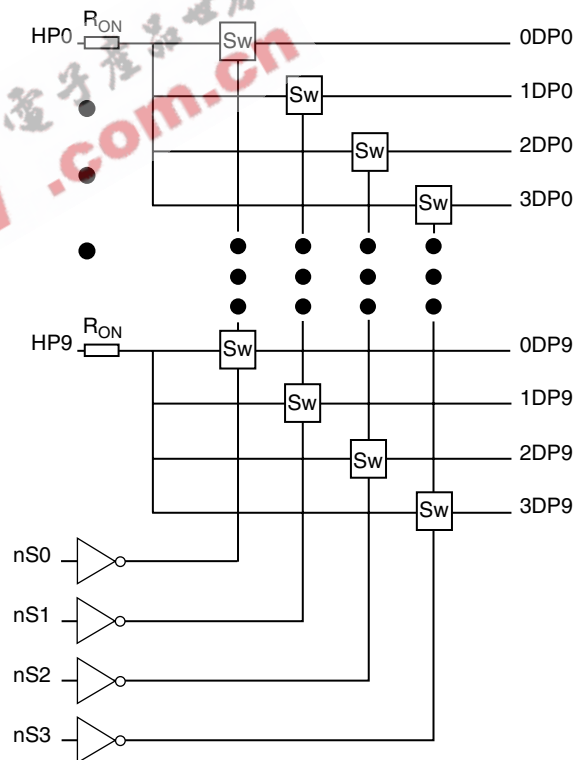
FEATURES

- 40 low skew single-ended DIMM ports
- 4 SSTL-2 compatible enable inputs
- Maximum Switching Speed: 3ns
- Output skew: 120ps (maximum)
- Bank skew: 45ps (maximum)
- $r_{on} = 8\Omega$ (typical)
- Full 2.5V supply modes
- 0°C to 70°C ambient operating temperature
- Pin compatible with the CBTV4010

SIMPLIFIED SCHEMATIC



LOGIC DIAGRAM



PIN ASSIGNMENT

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|-----------------|-----------------|------|------|------|------|------|------|------|------|------|
| A | V _{DD} | nS1 | nc | | 1DP0 | 2DP0 | 3DP0 | | 2DP1 | 3DP1 | 0DP2 |
| B | nS2 | V _{DD} | nS0 | GND | 0DP0 | HP0 | 0DP1 | 1DP1 | HP1 | GND | 1DP2 |
| C | nc | nS3 | | | | | | | | HP2 | 2DP2 |
| D | | GND | | | | | | | | 3DP2 | |
| E | 2DP9 | 3DP9 | | | | | | | | 0DP3 | 1DP3 |
| F | 1DP9 | HP9 | | | | | | | | HP3 | 2DP3 |
| G | 0DP9 | 3DP8 | | | | | | | | GND | 3DP3 |
| H | | 2DP8 | | | | | | | | 0DP4 | |
| J | 1DP8 | HP8 | | | | | | | | HP4 | 1DP4 |
| K | 0DP8 | GND | HP7 | 0DP7 | 3DP6 | HP6 | GND | 3DP5 | HP5 | 3DP4 | 2DP4 |
| L | 3DP7 | 2DP7 | 1DP7 | | 2DP6 | 1DP6 | 0DP6 | | 2DP5 | 1DP5 | 0DP5 |

ICS83840
64-Ball TFBGA
 7mm x 7mm x 1.2mm
 package body
H Package
 Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | Description |
|--|---|--------|-----------------------|
| A1, B2 | V_{DD} | Power | Positive supply pins. |
| B4, B10, D2, G10, K2, K7 | GND | Power | Power supply ground. |
| A3, C1 | nc | Unused | No connect. |
| A2, B1, C2, B3 | nS1, nS2, nS3, nS0 | Port | Select pins. |
| B6, B9, C10, F2, F10, J2, J10, K3, K6, K9 | HP0, HP1, HP2, HP9, HP3, HP8, HP4, HP7, HP6, HP5 | Port | Host ports. |
| A5, A6, A7, B5 | 1DP0, 2DP0, 3DP0, 0DP0 | Port | DIMM ports. |
| A9, A10, B7, B8 | 2DP1, 3DP1, 0DP1, 1DP1 | Port | DIMM ports. |
| A11, B11, C11, D10 | 0DP2, 1DP2, 2DP2, 3DP2 | Port | DIMM ports. |
| E10, E11, F11, G11 | 0DP3, 1DP3, 2DP3, 3DP3 | Port | DIMM ports. |
| H10, J11, K10, K11 | 0DP4, 1DP4, 3DP4, 2DP4 | Port | DIMM ports. |
| K8, L9, L10, L11 | 3DP5, 2DP5, 1DP5, 0DP5 | Port | DIMM ports. |
| K5, L5, L6, L7 | 3DP6, 2DP6, 1DP6, 0DP6 | Port | DIMM ports. |
| K4, L1, L2, L3 | 0DP7, 3DP7, 2DP7, 1DP7 | Port | DIMM ports. |
| G2, H2, J1, K1 | 3DP8, 2DP8, 1DP8, 0DP8 | Port | DIMM ports. |
| E1, E2, F1, G1 | 2DP9, 3DP9, 1DP9, 0DP9 | Port | DIMM ports. |

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|------------------------|-------------------------------|---------|---------|---------|-------|
| C_{IN} | Input Capacitance | nSx $V_I = 0V$ or V_{DD} | | | 5 | pF |
| C_{ON} | Channel on Capacitance | HPx $V_{IN} = 1.5V$ | | | 12 | pF |

NOTE: Capacitance values are measured at 10MHz and a bias voltage 3V. Capacitance is not production tested.

TABLE 3. FUNCTION TABLE

| Control Input | Function |
|---------------|---|
| nSx | |
| L | Host Port = DIMM Port |
| H | Host Port = Disconnected DIMM Port = 400Ω to GND |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{DD} | -0.5V to +3.3V |
| Inputs, V_I | -0.3V to $V_{DD} + 0.3V$ |
| Ports | |
| DC Input Clamp Current, I_{IK} | -50mA |
| Package Thermal Impedance, θ_{JA} | 50.04°C/W (0 mfps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|---------|
| V_{DD} | Positive Supply Voltage | | 2.3 | 2.5 | 2.7 | V |
| I_{DD} | Power Supply Current | | | | 50 | μA |

TABLE 4B. DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------------|---|---|------------------------------|-----------|-----------|
| V_{IH} | Input High Voltage | nSx | 1.6 | | | V |
| V_{IL} | Input Low Voltage | nSx | | | 0.9 | V |
| V_{IK} | Input Clamp Voltage | $V_{DD} = 2.3V$; $I_I = -18mA$ | | | -1.2 | V |
| I_L | Input Leakage Current | nSx | $V_{DD} = 2.5V$; $V_I = V_{DD}$ or GND; $nS = V_{DD}$ | | ± 100 | μA |
| | | Host Port | | | ± 100 | μA |
| | | DIMM Port | | $nS = GND$ for $I_{L(test)}$ | | ± 100 |
| r_{ON} | On Resistance; NOTE 1 | $V_{DD} = 2.5V$; $V_A = 0.8V$; $V_B = 1.0V$ | 5 | 8 | 13 | Ω |
| | | $V_{DD} = 2.5V$; $V_A = 1.7V$; $V_B = 1.5V$ | 5 | 8 | 13 | Ω |

NOTE 1: Measured by the current between the Host and the DIMM terminals at the indicated voltages on each side of the switch.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---------------------------------|--|---------|---------|---------|-------|
| t_{PD} | Propagation Delay; NOTE 1, 4 | From HPx or xDPx to xDPx or HPx | 85 | 150 | 220 | ps |
| t_{EN} | Output Enable Time | From nSx to HPx or nDPx | 1.7 | | | ns |
| t_{DIS} | Output Disable Time | From nSx to HPx or nDPx | 1.6 | | | ns |
| t_{OSK} | Output Skew; NOTE 2, 4 | Any Port to any Port | | | 120 | ps |
| t_{BSK} | Bank Skew; NOTE 3, 4 | Any Port to any Port within the same bank | | | 45 | ps |

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

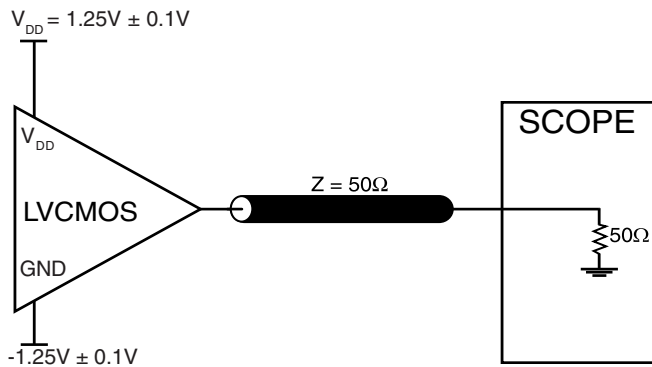
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew within a bank with equal load conditions.

NOTE 4: Not production tested, guaranteed by characterization.

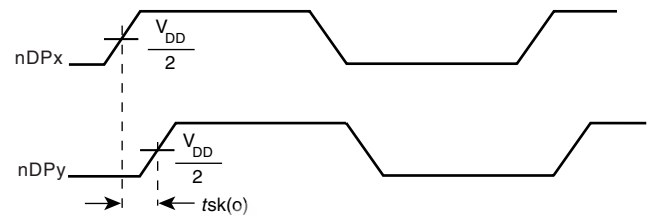


PARAMETER MEASUREMENT INFORMATION

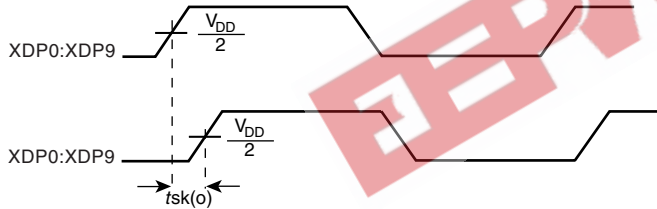


This circuit is used for test purposes only,
not intended for application use.

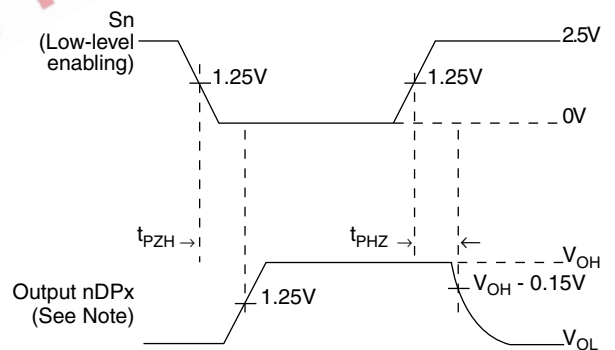
2.5V OUTPUT LOAD AC TEST CIRCUIT



OUTPUT SKEW

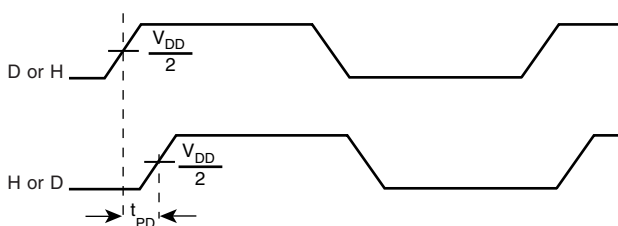


BANK SKEW (where X denotes outputs in the same bank)



NOTE: The output is high except when disabled by the Sn control.

3-STATE OUTPUT ENABLE/DISABLE TIMES



PROPAGATION DELAY



RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

| θ_{JA} by Velocity (Millimeter Feet per Second) | | | |
|--|-----------|-----------|-----------|
| | 0 | 1 | 2 |
| Two-Layer PCB, JEDEC Standard Test Boards | 50.04°C/W | 43.18°C/W | 41.17°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS83840 is: 320

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PACKAGE OUTLINE - H SUFFIX

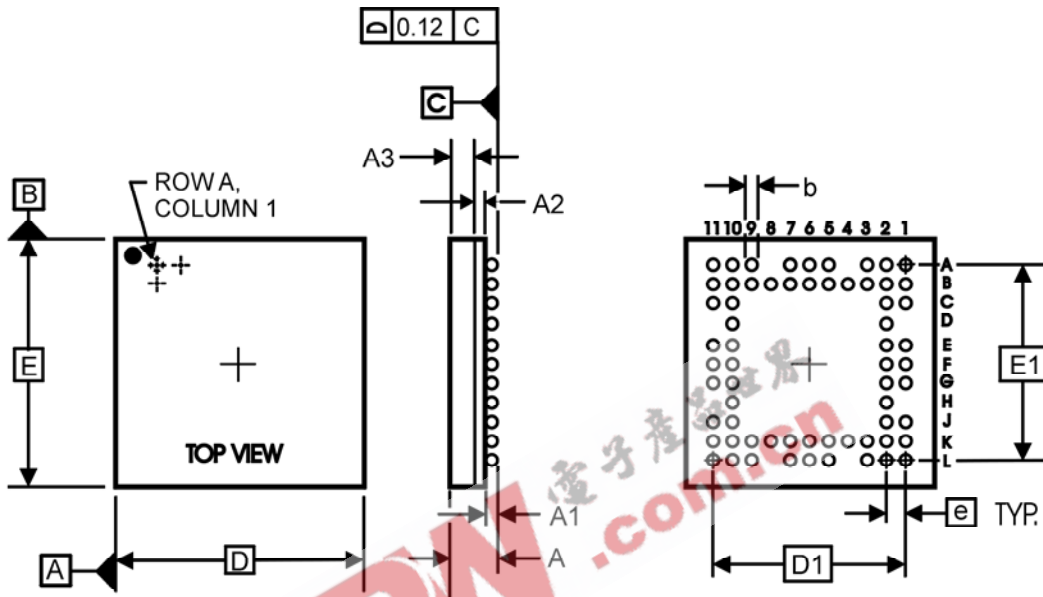


TABLE 7. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|--------------------------------|---------|---------|
| SYMBOL | FBGA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| | 64 Balls, 7x7mm, 11x11 Pattern | | |
| A | 1.0 | 1.1 | 1.2 |
| A1 | 0.165 | 0.2 | 0.235 |
| A2 | 0.16 | 0.2 | 0.24 |
| A3 | 0.675 | 0.7 | 0.725 |
| b | 0.25 | 0.3 | 0.35 |
| D | 7.00 BSC | | |
| D1 | 5.00 BSC | | |
| E | 7.00 BSC | | |
| E1 | 5.00 BSC | | |
| e | 0.50 BSC | | |

REFERENCE DOCUMENT: JEDEC PUBLICATION 95



Integrated
Circuit
Systems, Inc.

ICS83840

DDR SDRAM MUX

TABLE 8. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|-------------------|------------|--|--------------|-------------|
| ICS83840AH | ICS83840AH | 64-Ball TFBGA | 416 per tray | 0°C to 70°C |
| ICS83840AHT | ICS83840AH | 64-Ball TFBGA on Tape and Reel | 1000 | 0°C to 70°C |
| ICS83840AHLF | ICS3840ALF | 64-Ball, Lead Free, TFBGA | 416 per tray | 0°C to 70°C |
| ICS83840AHLFT | ICS3840ALF | 64-Ball, Lead Free, TFBGA on Tape and Reel | 1000 | 0°C to 70°C |

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Integrated
Circuit
Systems, Inc.

ICS83840
DDR SDRAM MUX

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|---|----------|
| A | | 1 | Changed dimension on Pin Assignment from 0.7mm to 1.2mm. | 12/22/03 |
| | | 6 | Updated Package Outline Drawing and Package Dimensions Table. | |
| | | 7 | Added "Lead Free" marking. | |
| | | | | |
| | | | | |

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