intersil

ICL7665S

Data Sheet April 1999 File Number 3182.4

CMOS Micropower Over/Under Voltage Detector

The ICL7665S Super CMOS Micropower Over/Under Voltage Detector contains two low power, individually programmable Voltage detectors on a single CMOS chip. Requiring typically 3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The ICL7665S, Super Programmable Over/Under Voltage Detector is a direct replacement for the industry standard ICL7665B offering ***wider*** operating voltage and temperature ranges, ***improved*** threshold accuracy (ICL7665SA), and temperature coefficient, and ***guaranteed*** maximum supply current. All improvements are highlighted in the electrical characteristics section. ***All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.***

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICL7665SCBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7665SCPA	0 to 70	8 Ld PDIP	E8.3
ICL7665SACBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7665SACPA	0 to 70	8 Ld PDIP	E8.3
ICL7665SIBA	-40 to 85	8 Ld SOIC (N)	M8.15
ICL7665SIPA	-40 to 85	8 Ld PDIP	E8.3
ICL7665SAIBA	-40 to 85	8 Ld SOIC (N)	M8.15
ICL7665SAIPA	-40 to 85	8 Ld PDIP	E8.3

Features

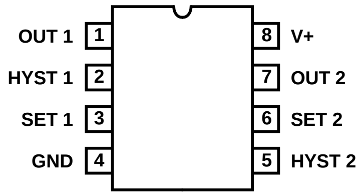
- Guaranteed 10μA Maximum Quiescent Current Over Temperature
- Guaranteed Wider Operating Voltage Range Over Entire Operating Temperature Range
- 2% Threshold Accuracy (ICL7665SA)
- Dual Comparator with Precision Internal Reference
- 100ppm/^{o}C Temperature Coefficient of Threshold Voltage
- 100% Tested at 2V
- Output Current Sinking Ability . . . . Up to 20mA
- Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels

Applications

- Pocket Pagers
- Portable Instrumentation
- Charging Systems
- Memory Power Back-Up
- Battery Operated Systems
- Portable Computers
- Level Detectors

Pinout

ICL7665S
(SOIC, PDIP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (Note 2)	-0.3 to +18V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2)	-0.3V to 18V
Output Voltages HYST1 and HYST2 (with respect to V+) (Note 2)	-0.3V to +18V
Input Voltages SET1 and SET2 (Note 2)	(GND -0.3V) to (V+ V- +0.3V)
Maximum Sink Output OUT1 and OUT2	25mA
Maximum Source Output Current HYST1 and HYST2	-25mA

Operating Conditions

Temperature Range

ICL7665SC	0°C to 70°C
ICL7665SI	-40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	150	N/A
Plastic SOIC Package	180	N/A

Maximum Junction Temperature (Plastic)	150°C
Maximum Junction Temperature (CERDIP)	175°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only)	300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, current into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Electrical Specifications

The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = 25°C, Test Circuit Figure 7. Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+	ICL7665S	$T_A = 25^oC$	1.6	-	16	V
			$0^oC \le T_A \le 70^oC$	1.8	-	16	V
			$-25^oC \le T_A \le 85^oC$	1.8	-	16	V
		ICL7665SA	$0^oC \le T_A \le 70^oC$	1.8	-	16	V
			$-25^oC \le T_A \le 85^oC$	1.8	-	16	V
Supply Current	I+	GND ≤ V_{SET1}, V_{SET2} ≤ V+, All Outputs Open Circuit					
		$0^oC \le T_A \le 70^oC$	V+ = 2V	-	2.5	10	μA
			V+ = 9V	-	2.6	10	μA
			V+ = 15V	-	2.9	10	μA
		$-40^oC \le T_A \le 85^oC$	V+ = 2V	-	2.5	10	μA
			V+ = 9V	-	2.6	10	μA
			V+ = 15V	-	2.9	10	μA
Input Trip Voltage	V_{SET1}	ICL7665S		1.20	1.30	1.40	V
	V_{SET2}			1.20	1.30	1.40	V
	V_{SET1}	ICL7665SA		1.275	1.30	1.325	V
	V_{SET2}			1.275	1.30	1.325	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$	ICL7665S		-	200	-	ppm
		ICL7665SA		-	100	-	ppm
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{2HYST2} = 1MΩ, 2V ≤ V+ ≤ 10V		-	0.03	-	%/V

Electrical Specifications

The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = 25°C, Test Circuit Figure 7. Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Leakage Currents of OUT and HYST	I_{OLK}	V_{SET} = 0V or $V_{SET} \geq$ 2V		-	10	200	nA
	I_{HLK}			-	-10	-100	nA
	I_{OLK}	V+ = 15V, T_A = 70°C		-	-	2000	nA
	I_{HLK}			-	-	-500	nA
Output Saturation Voltages	V_{OUT1}	V_{SET1} = 2V, I_{OUT1} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.1	0.3	V
			V+ = 15V	-	0.06	0.2	V
Output Saturation Voltages	V_{HYST1}	V_{SET1} = 2V, I_{HYST1} = -0.5mA	V+ = 2V	-	-0.15	-0.30	V
			V+ = 5V	-	-0.05	-0.15	V
			V+ = 15V	-	-0.02	-0.10	V
Output Saturation Voltages	V_{OUT2}	V_{SET2} = 0V, I_{OUT2} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.15	0.3	V
			V+ = 15V	-	0.11	0.25	V
Output Saturation Voltages	V_{HYST2}	V_{SET2} = 2V	V+ = 2V, I_{HYST2} = -0.2mA	-	-0.25	-0.8	V
			V+ = 5V, I_{HYST2} = -0.5mA	-	-0.43	-1.0	V
			V+ = 15V, I_{HYST2} = -0.5mA	-	-0.35	-0.8	V
V_{SET} Input Leakage Current	I_{SET}	GND $\leq V_{SET} \leq$ V+		-	0.01	10	nA
Δ Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ, V_{OUT}LO = 1% V+, V_{OUT}HI = 99% V+	ICL7665S	-	1.0	-	mV
			ICL7665SA	-	0.1	-	mV
Difference in Trip Voltages	V_{SET1} - V_{SET2}	R_{OUT}, R_{HYST} = 1mW		-	±5	±50	mV
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1mW	ICL7665S	-	±1	-	mV
			ICL7665SA	-	±0.1	-	mV

NOTES:

3. Derate above 25°C ambient temperature at 4mW/°C
4. All significant improvements over the industry standard ICL7665 are highlighted.

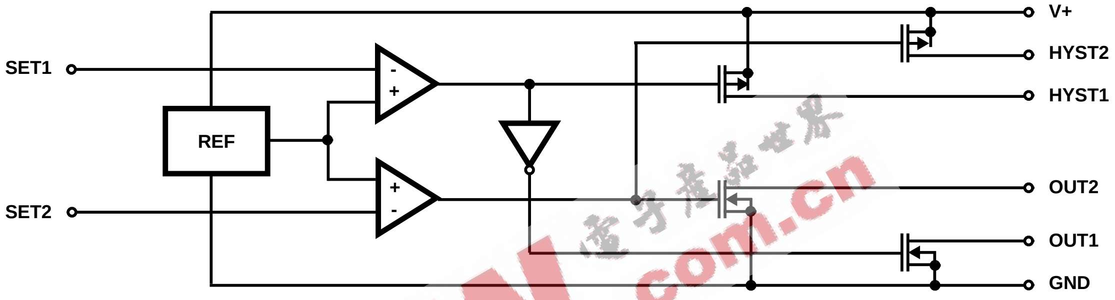
AC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DELAY TIMES						
Input Going HI	t_{SO1D}	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	85	-	µs
	t_{SH1D}		-	90	-	µs
	t_{SO2D}		-	55	-	µs
	t_{SH2D}		-	55	-	µs
Input Going LO	$t_{\overline{S}O1D}$	V_{SET} Switched between 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	75	-	µs
	$t_{\overline{S}H1D}$		-	80	-	µs
	$t_{\overline{S}O2D}$		-	60	-	µs
	$t_{\overline{S}H2D}$		-	60	-	µs

AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise Times	t_{O1R}	V_{SET} Switched between 1.0V to 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$	-	0.6	-	µs
	t_{O2R}		-	0.8	-	µs
	t_{H1R}		-	7.5	-	µs
	t_{H2R}		-	0.7	-	µs
Output Fall Times	t_{O1F}	V_{SET} Switched between 1.0V to 1.6V $R_{OUT} = 4.7k\Omega$, $C_L = 12pF$ $R_{HYST} = 20k\Omega$, $C_L = 12pF$	-	0.6	-	µs
	t_{O2F}		-	0.7	-	µs
	t_{H1F}		-	4.0	-	µs
	t_{H2F}		-	1.8	-	µs

Functional Block Diagram



CONDITIONS (Note 5)
$V_{SET1} > 1.3V$, OUT1 Switch ON, HYST1 Switch ON
$V_{SET1} < 1.3V$, OUT1 Switch OFF, HYST1 Switch OFF
$V_{SET2} > 1.3V$, OUT2 Switch OFF, HYST2 Switch ON
$V_{SET2} < 1.3V$, OUT2 Switch ON, HYST2 Switch OFF

NOTE:

5. See Electrical Specifications for exact thresholds.

Typical Performance Curves

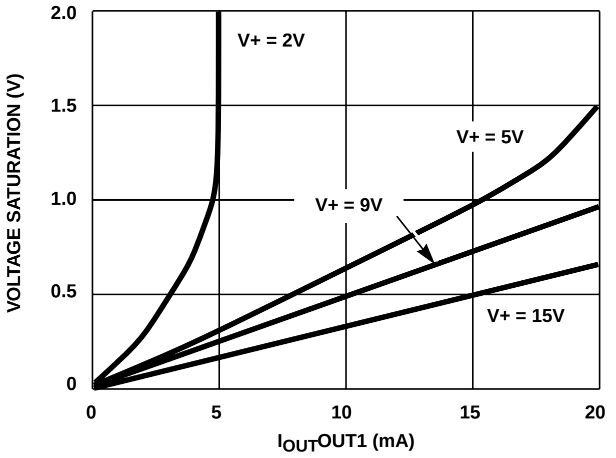


FIGURE 1. OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

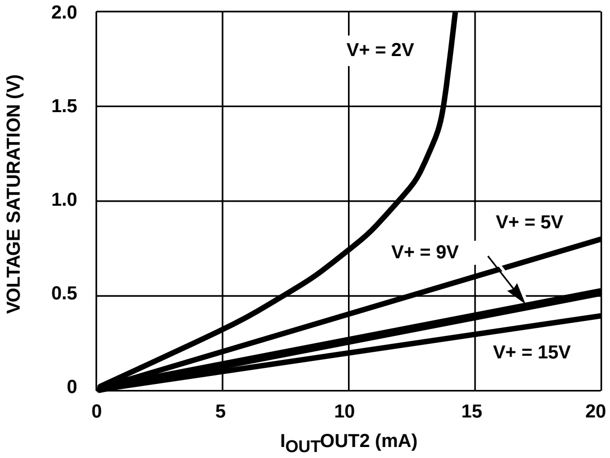


FIGURE 2. OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

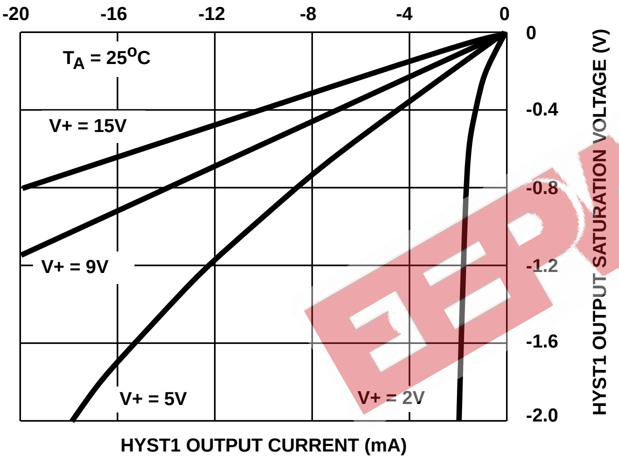


FIGURE 3. HYST1 OUTPUT SATURATION VOLTAGE vs HYST1 OUTPUT CURRENT

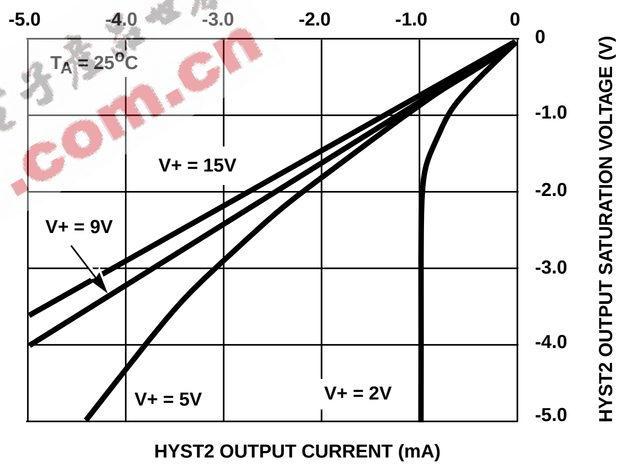


FIGURE 4. HYST2 OUTPUT SATURATION VOLTAGE vs HYST2 OUTPUT CURRENT

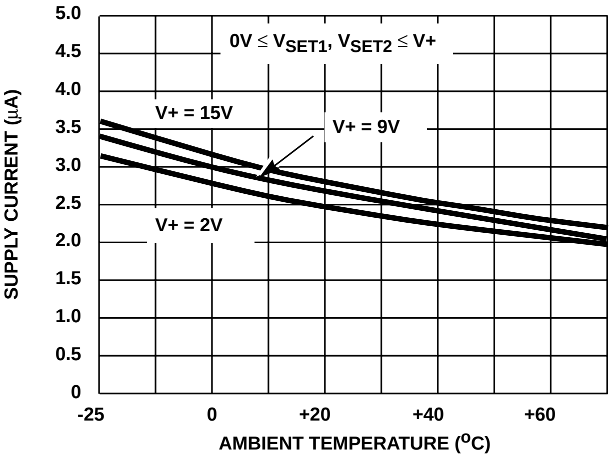


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

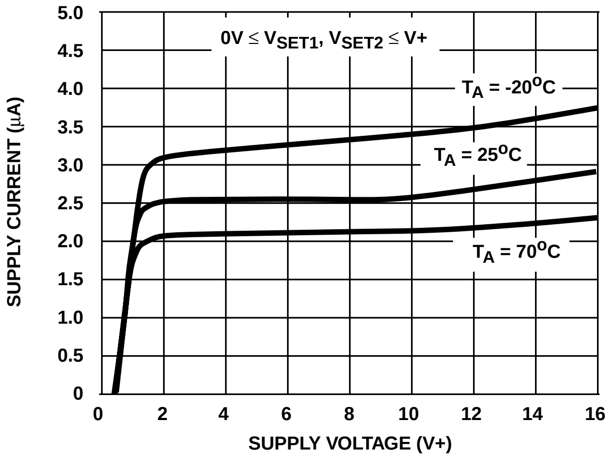


FIGURE 6. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

Detailed Description

As shown in the Functional Diagram, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V bandgap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under Voltage Detector and the Over Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so V_{SET1} will generally not quite equal V_{SET2}.

The input impedance of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

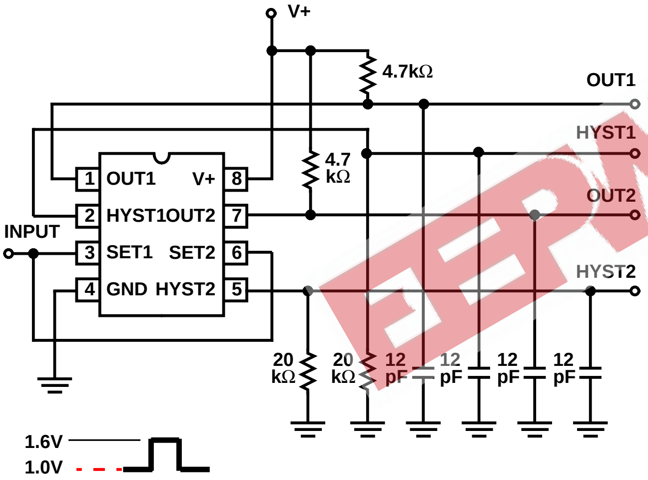


FIGURE 7. TEST CIRCUITS

Precautions

Junction isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly (“instantaneously”), e.g., through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/µs in such a circuit. A low impedance capacitor (e.g., 0.05µF disc ceramic) between the V+ and GND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time.

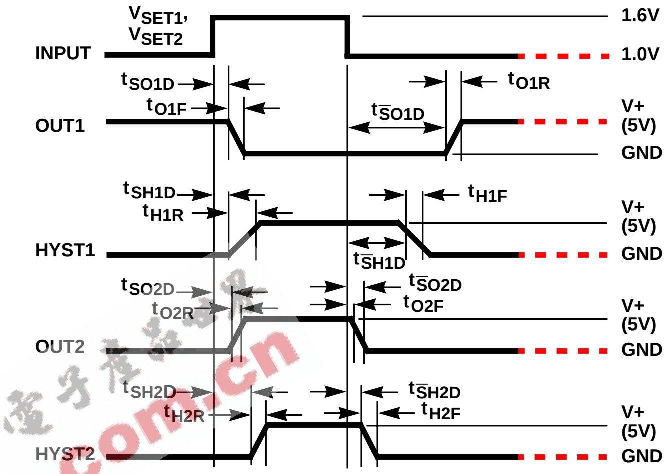


FIGURE 8. SWITCHING WAVEFORMS

Simple Threshold Detector

Figure 9 shows the simplest connection of the ICL7665S for threshold detection. From the graph 9B, it can be seen that at low input voltage OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g., at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equation giving V_{SET1} and V_{SET2} are from Figure 9A:

$$V_{SET1} = V_{IN}\frac{R_{11}}{(R_{11}+R_{21})} \;;\; V_{SET2} = V_{IN}\frac{R_{12}}{(R_{12}+R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1}\frac{(R_{11}+R_{21})}{R_{11}} = 1.3\frac{(R_{11}+R_{21})}{R_{11}} \quad \text{for detector 1}$$

and

$$V_{TR2} = V_{SET2}\frac{(R_{12}+R_{22})}{R_{12}} = 1.3\frac{(R_{12}+R_{22})}{R_{12}} \quad \text{for detector 2}$$

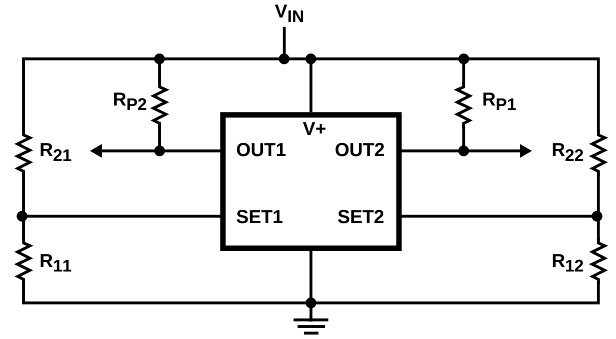


FIGURE 9A. CIRCUIT CONFIGURATION

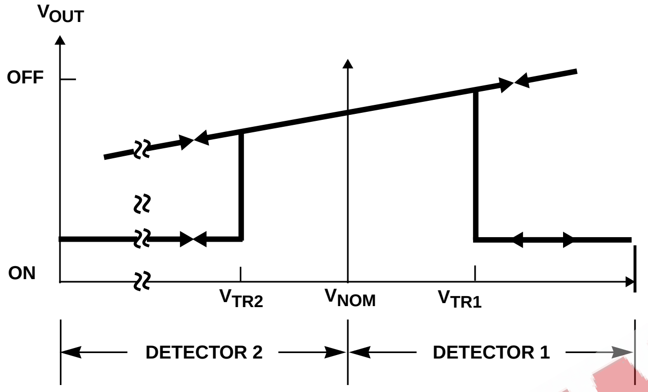


FIGURE 9B. TRANSFER CHARACTERISTICS

FIGURE 9. SIMPLE THRESHOLD DETECTOR

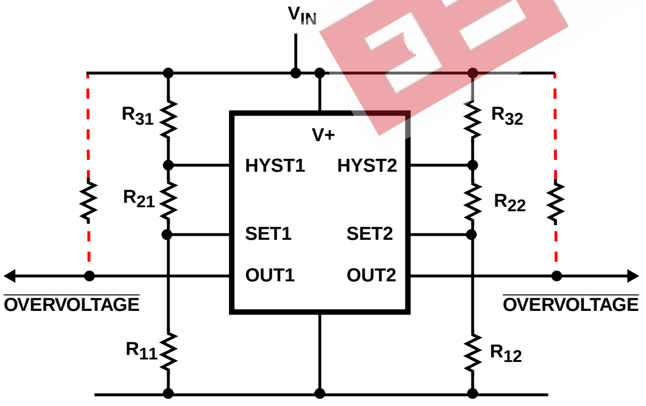


FIGURE 10A. CIRCUIT CONFIGURATION

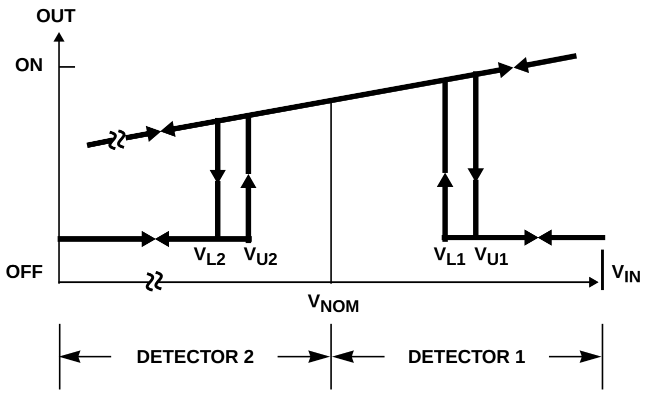


FIGURE 10B. TRANSFER CHARACTERISTICS

FIGURE 10. THRESHOLD DETECTOR WITH HYSTERESIS

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltage, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Threshold Detector with Hysteresis

Figure 10A shows how to set up such hysteresis, while Figure 10B shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicated direction of change. The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1N}, R_{2N}, and R_{3N}, until the trip point is reached. As this value is passed, the detector changes state, R_{3N} is shorted out, and the trip point becomes controlled by only R_{1N} and R_{2N}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 11. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.

$$V_{TR2} = V_{SET2}\frac{(R_{12} + R_{22})}{R_{12}} = 1.3\frac{(R_{12} + R_{22})}{R_{12}} \quad \text{for detector 2}$$

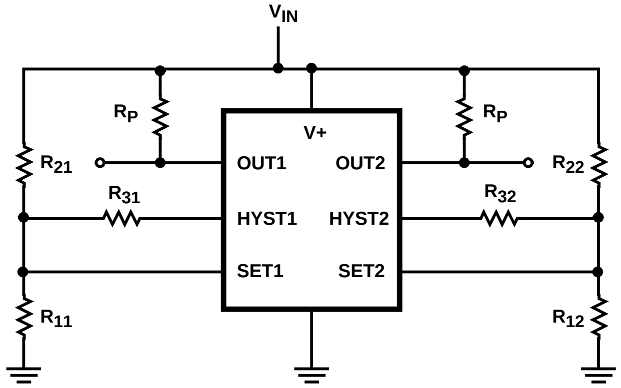


FIGURE 11. AN ALTERNATIVE HYSTERESIS CIRCUIT

TABLE 1. SET-POINT EQUATIONS

NO HYSTERESIS
Over-Voltage $V_{TRIP} = \dfrac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage $V_{TRIP} = \dfrac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 10A
$V_{U1} = \dfrac{R_{11} + R_{21} + R31}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \dfrac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
$V_{U2} = \dfrac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$
Under-Voltage V_{TRIP}
$V_{L2} = \dfrac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 11
$V_{U1} = \dfrac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \dfrac{R_{11} + \dfrac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$
$V_{U2} = \dfrac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
Over-Voltage V_{TRIP}
$V_{L2} = \dfrac{R_{12} + \dfrac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$

Applications

Single Supply Fault Monitor

Figure 12 shows an over/under voltage fault monitor for a single supply. The over voltage trip point is centered around 5.5V and the under voltage trip point is centered around 4.5V. Both have some hysteresis to prevent erratic output ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

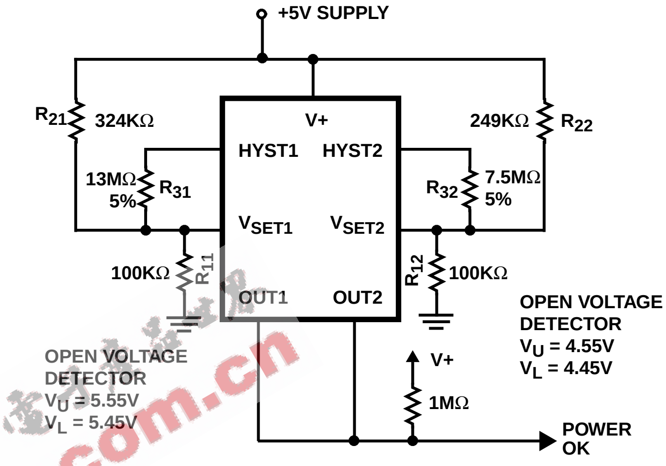


FIGURE 12. FAULT MONITOR FOR A SINGLE SUPPLY

Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 13. The resistors are chosen such that the sum of the currents through R_{21A}, R_{21B}, and R_{31} is equal to the current through R_{11} when the two input voltage are at the desired low voltage detection point. The current through R_{11} at this point is equal to $1.3V/R_{11}$. The voltage at the V_{SET} input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different that the trip voltage when both supplies are below their nominal voltages.

The other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.

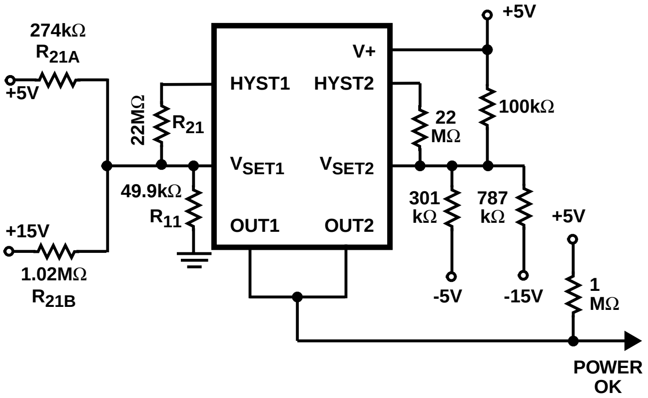


FIGURE 13. MULTIPLE SUPPLY FAULT MONITOR

Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 14 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as V_{SET1} is greater than 1.3V, OUT1 is low, but when V_{SET1} drops below 1.3V, OUT1 goes high shutting off the ICL7663S. OUT2 is used for low battery warning. When V_{SET2} is greater than 1.3V, OUT2 is high and the low battery warning is on. When V_{SET2} drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

Power Fail Warning and Powerup/Powerdown Reset

Figure 15 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

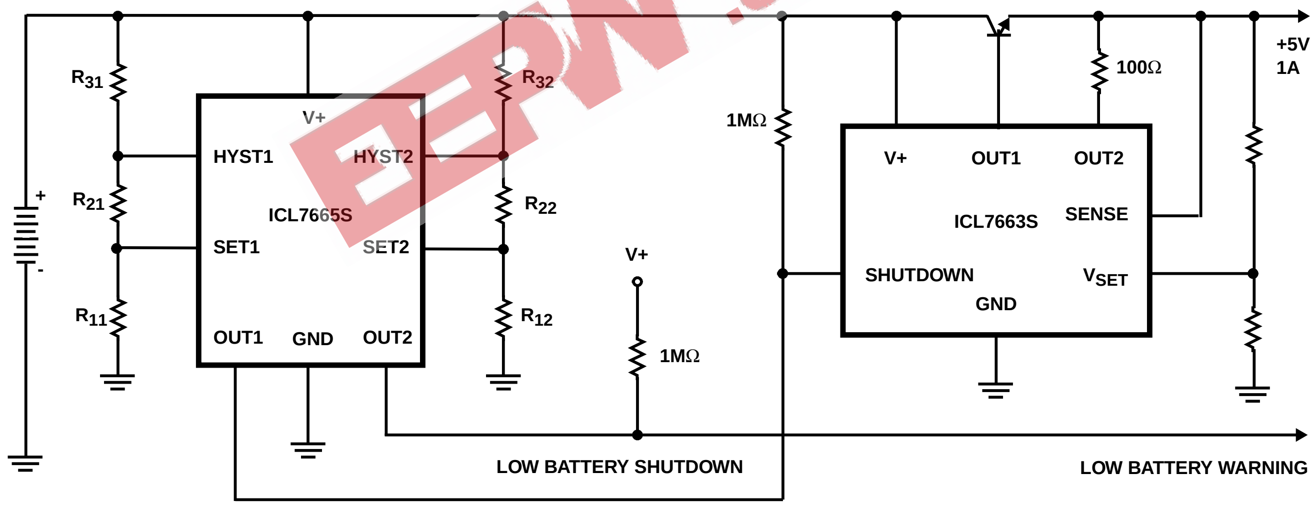


FIGURE 14. LOW BATTERY WARNING AND LOW BATTERY DISCONNECT

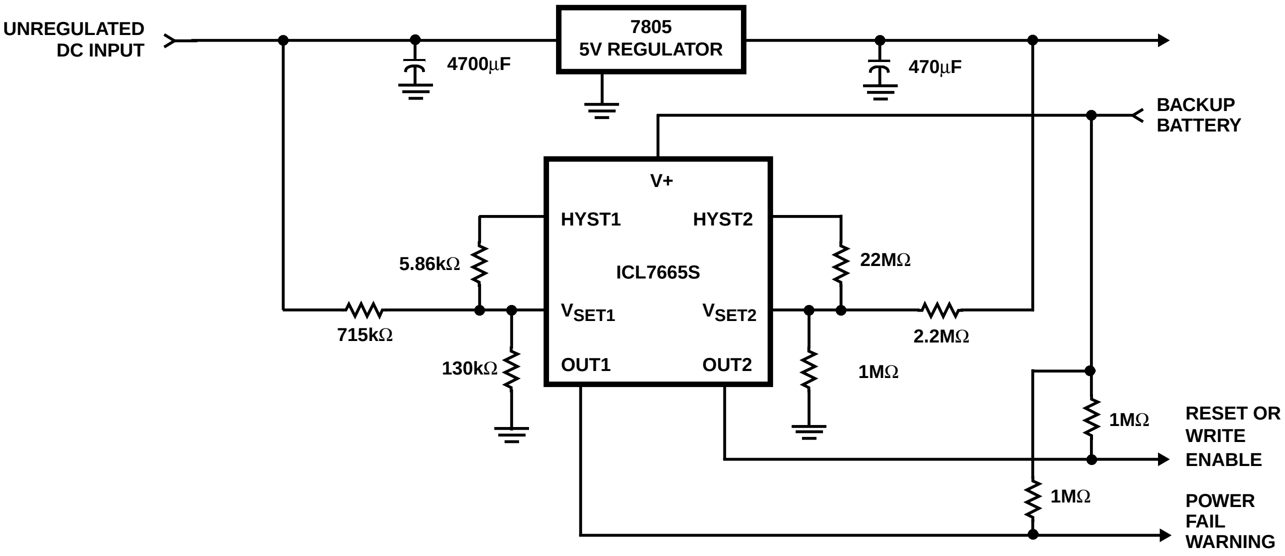


FIGURE 15. POWER FAIL WARNING AND POWERUP/POWERDOWN RESET

Simple High/Low Temperature Alarm

Figure 16 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of R_1 is determined by the V_{BE} of the transistor and the position of R_1's wiper arm. This voltage has a negative temperature coefficient. R_1 is adjusted so that V_{SET2} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2 goes low. R_2 is adjusted so that V_{SET1} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

AC Power Fail and Brownout Detector

Figure 17 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor, C_1, is charged through R_1 when OUT1 is OFF. With a normal 100 VAC input to the transformer, OUT1 will discharge C_1 once every cycle, approximately every 16.7ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that C_1 does not discharge. When the voltage on C_1 reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant, R_1C_1, is chosen such that it takes longer than 16.7ms to charge C_1 1.3V.

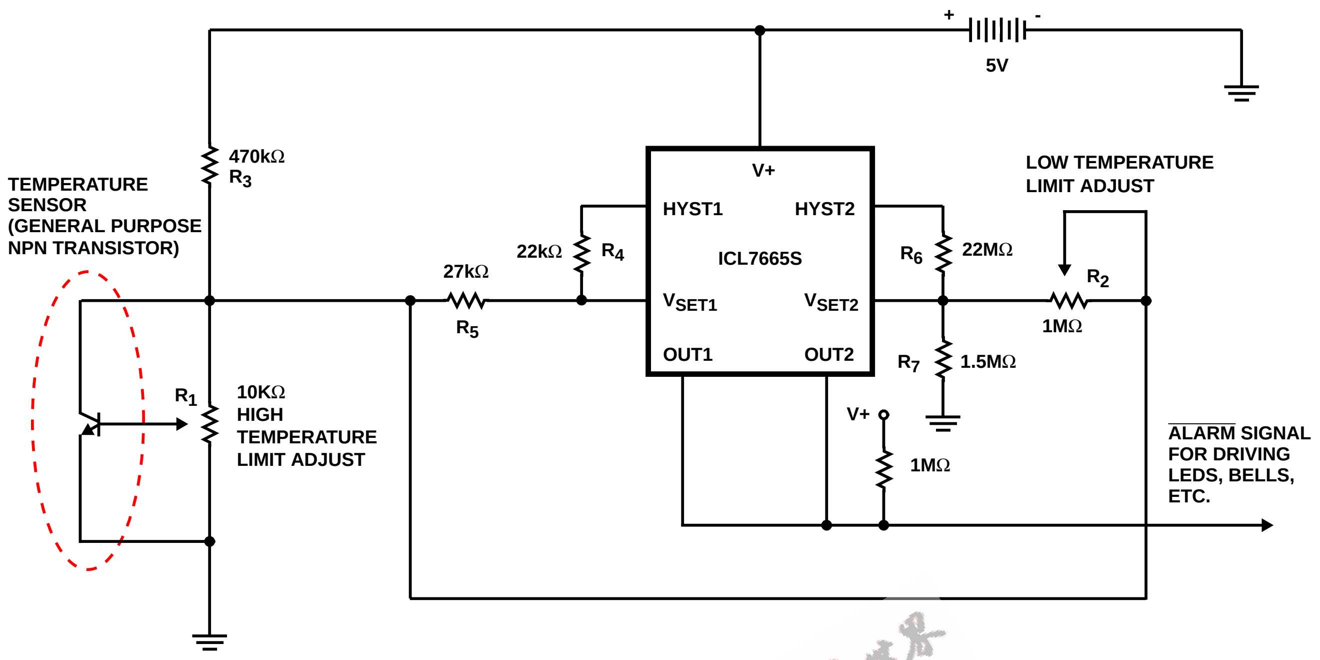


FIGURE 16. SIMPLE HIGH/LOW TEMPERATURE ALARM

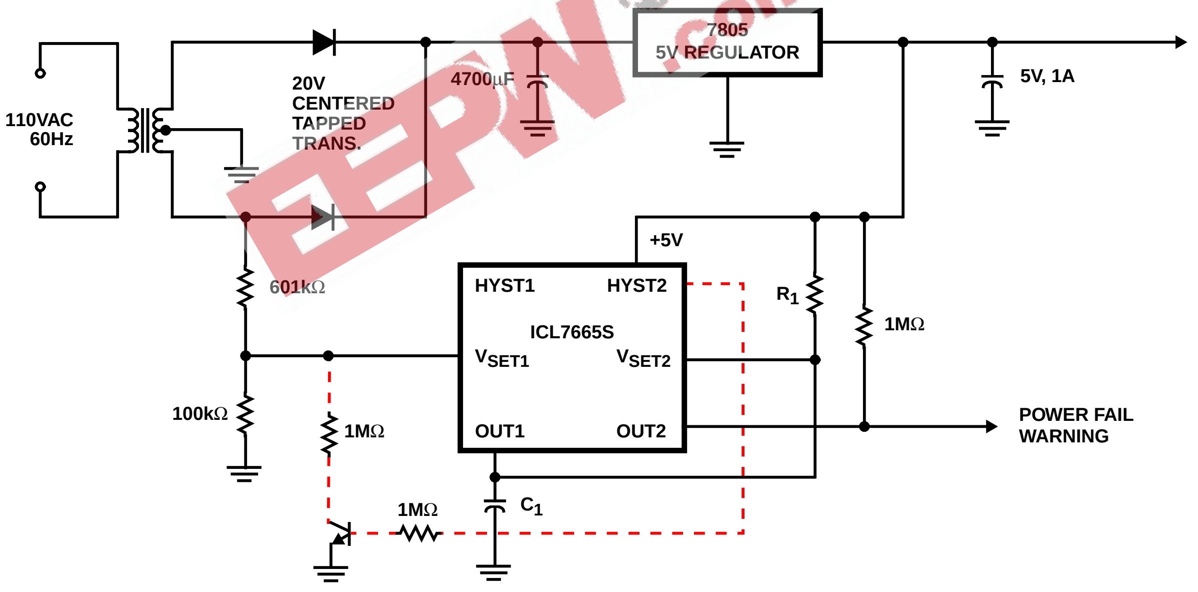


FIGURE 17. AC POWER FAIL AND BROWNOUT DETECTOR