

Long Range Fixed Timer

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

Ordering Information

| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---------------------------|--------------|------------------|--------------------------|-------------|
| ICM7242IPA | 7242 IPA | -25 to +85 | 8 Ld PDIP | E8.3 |
| ICM7242IPAZ (See Note) | 7242 IPAZ | -25 to +85 | 8 Ld PDIP** (Pb-free) | E8.3 |
| ICM7242CBAZ* | 7242 CBAZ | 0 to +70 | 8 Ld SOIC (Pb-free) | M8.15 |
| ICM7242IBAZ* | 7242 IBAZ | -25 to +85 | 8 Ld SOIC (Pb-free) | M8.15 |

*Add "-T" suffix for tape and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

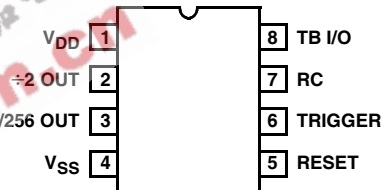
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Features

- Replaces the 2242 in Most Applications
- Timing From Microseconds to Days
- Cascadable
- Monostable or Astable Operation
- Wide Supply Voltage Range 2V to 16V
- Low Supply Current 115µA at 5V
- Pb-Free Plus Anneal Available (RoHS Compliant)

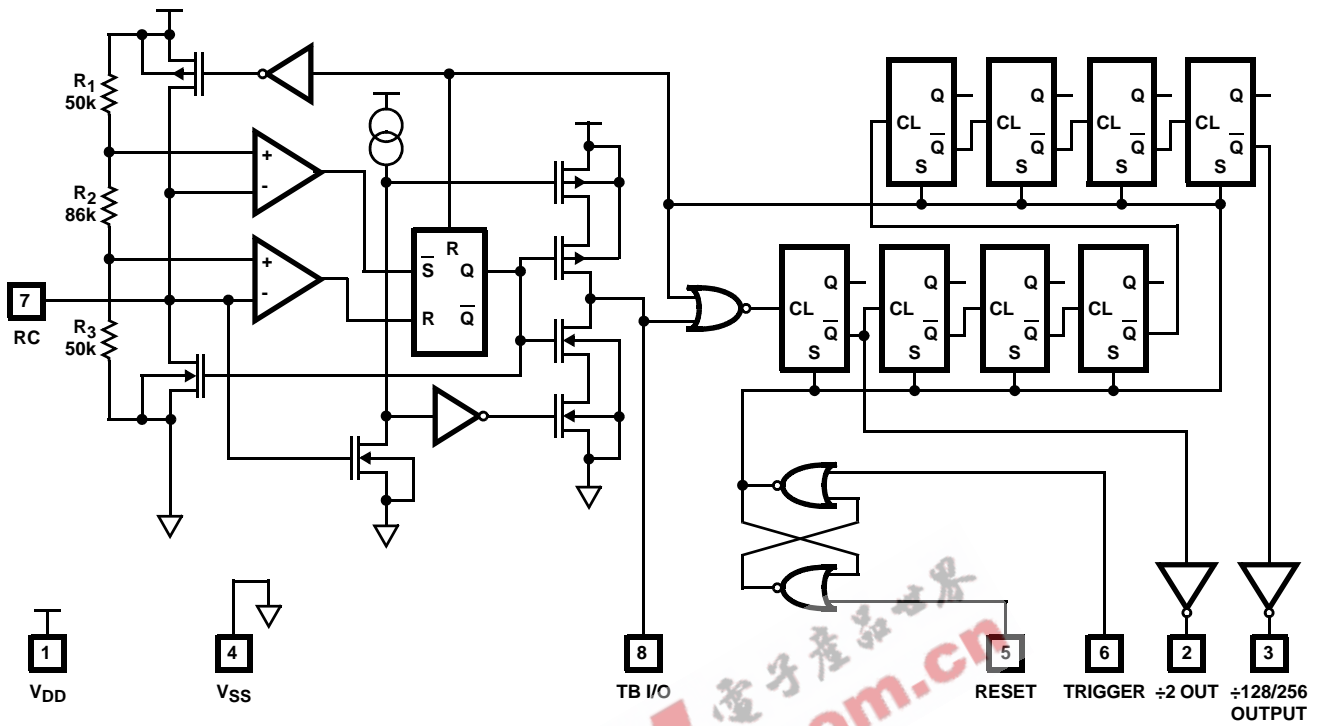
Pinout

**ICM7242
(8 LD PDIP, SOIC)
TOP VIEW**



ICM7242

Functional Block Diagram



ICM7242

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}) 18V
 Input Voltage (Note 1)
 Terminals (Pins 5, 6, 7, 8) ($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
 Continuous Output Current (Each Output) 50mA

Operating Conditions

Temperature Range
 ICM7242I -25°C to +85°C
 ICM7242C 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note2) θ_{JA} (°C/W)
 PDIP Package* 100
 SOIC Package 160
 Maximum Storage Temperature Range -65°C to +150°C
 Maximum Junction Temperature (Plastic Package) +150°C
 Pb-free reflow profile see link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

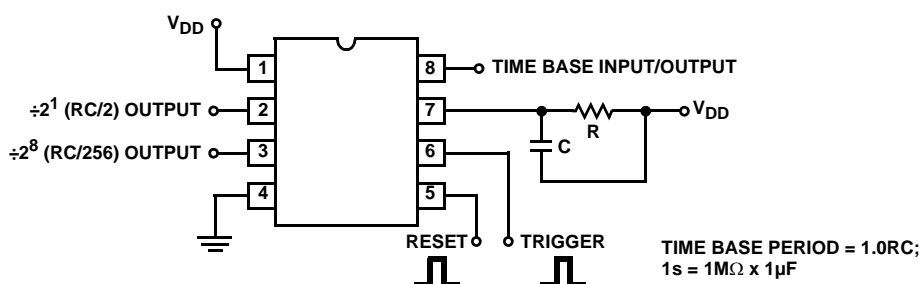
Electrical Specifications $V_{DD} = 5V$, $T_A = +25^\circ C$, $R = 10k\Omega$, $C = 0.1\mu F$, $V_{SS} = 0V$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|----------------------|--|------------------------|------|-----|----------|-----|
| Guaranteed Supply Voltage | V_{DD} | | 2 | - | 16 | V | |
| Supply Current | I_{DD} | Reset | - | 125 | - | μA | |
| | | Operating, $R = 10k\Omega$, $C = 0.1\mu F$ | - | 340 | 800 | μA | |
| | | Operating, $R = 1M\Omega$, $C = 0.1\mu F$ | - | 220 | 600 | μA | |
| | | TB Inhibited, RC Connected to V_{SS} | - | 225 | - | μA | |
| Timing Accuracy | | | - | 5 | - | % | |
| RC Oscillator Frequency Temperature Drift | $\Delta f/\Delta t$ | Independent of RC Components | - | 250 | - | ppm/°C | |
| Time Base Output Voltage | V_{OTB} | $I_{SOURCE} = 100\mu A$ | - | 3.5 | - | V | |
| | | $I_{SINK} = 1.0mA$ | - | 0.40 | - | V | |
| Time Base Output Leakage Current | I_{TBLK} | RC = Ground | - | - | 25 | μA | |
| Trigger Input Voltage | V_{TRIG} | $V_{DD} = 5V$ | - | 1.6 | 2.0 | V | |
| | | $V_{DD} = 15V$ | - | 3.5 | 4.5 | V | |
| Reset Input Voltage | V_{RST} | $V_{DD} = 5V$ | - | 1.3 | 2.0 | V | |
| | | $V_{DD} = 15V$ | - | 2.7 | 4.0 | V | |
| Trigger/Reset Input Current | I_{TRIG} I_{RST} | | - | 10 | - | μA | |
| Max Count Toggle Rate | f_T | $V_{DD} = 2V$ | } Counter/Divider Mode | - | 1 | - | MHz |
| | | $V_{DD} = 5V$ | | 2 | 6 | - | MHz |
| | | $V_{DD} = 15V$ | | - | 13 | - | MHz |
| | | 50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS} | | | | | |
| Output Saturation Voltage | V_{SAT} | All Outputs Except TB Output $V_{DD} = 5V$, $I_{OUT} = 3.2mA$ | - | 0.22 | 0.4 | V | |
| Output Sourcing Current | I_{SOURCE} | $V_{DD} = 5V$ Terminals 2 and 3, $V_{OUT} = 1V$ | - | 300 | - | μA | |
| MIN Timing Capacitor (Note 3) | C_T | | 10 | - | - | pF | |
| Timing Resistor Range (Note 3) | R_T | $V_{DD} = 2 - 16V$ | 1k | - | 22M | Ω | |

NOTE:

- For design only, not tested.

Test Circuit



NOTE:
4. $\pm 2^1$ and $\pm 2^8$ outputs are inverters and have active pullups.

Application Information

Operating Considerations

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in Figure 8. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200kHz.

The timing capacitor should be connected between the RC pin and the positive supply rail, V_{DD} , as shown in Figure 1. When system power is turned off, any charge remaining on the capacitor will be discharged to ground through a large internal diode between the RC node and V_{SS} . Do NOT reference the timing capacitor to ground, since there is no high current path in this direction to safely discharge the capacitor when power is turned off. The discharge current from such a configuration could potentially damage the device.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to the supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be ANDed, output inverters are used instead of open drain N-Channel transistors, and the

external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 1. Assuming that the device is in the RESET mode, which occurs on power up or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\pm 2^8$ output returns to the high state.

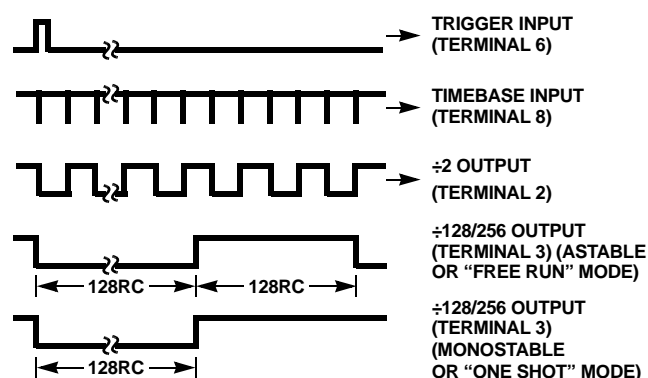


FIGURE 1. TIMING DIAGRAMS OF OUTPUT WAVEFORMS FOR THE ICM7242 (COMPARE WITH FIGURE 5)

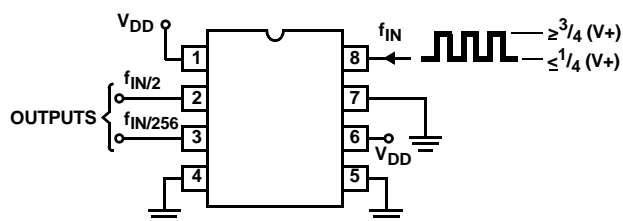


FIGURE 2. USING THE ICM7242 AS A RIPPLE COUNTER (DIVIDER)

ICM7242

To use the 8-bit counter without the timebase, Terminal 7 (RC) should be connected to ground and the outputs taken from Terminals 2 and 3.

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 3).

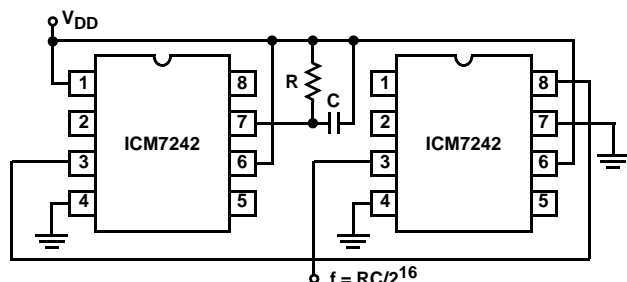


FIGURE 3. LOW FREQUENCY REFERENCE (OSCILLATOR)

For monostable operation the $\pm 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

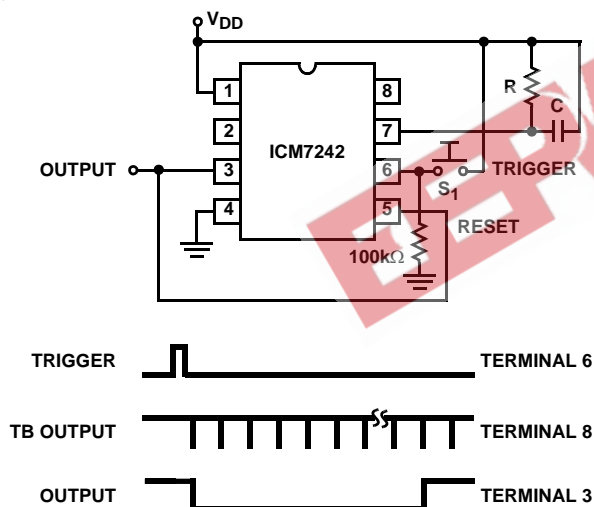


FIGURE 4. MONOSTABLE OPERATION

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p-resistors have been used on the ICM7242 to provide the comparator timing points.

TABLE 1. COMPARING THE ICM7242 WITH THE 2242

| CHARACTERISTICS | ICM7242 | 2242 |
|--|---------------|-------------|
| Operating Voltage | 2V to 16V | 4V to 15V |
| Operating Temperature Range | -25°C to 85°C | 0°C to 70°C |
| Supply Current, $V_{DD} = 5V$ | 0.7mA (Max) | 7mA (Max) |
| Pullup Resistors | | |
| TB Output | No | Yes |
| ± 2 Output | No | Yes |
| ± 256 Output | No | Yes |
| Toggle Rate | 3.0MHz | 0.5MHz |
| Resistor to Inhibit Oscillator | No | Yes |
| Resistor in Series with Reset for Monostable Operation | No | Yes |
| Capacitor TB Terminal for HF Operation | No | Sometimes |

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as shown in Figure 5.

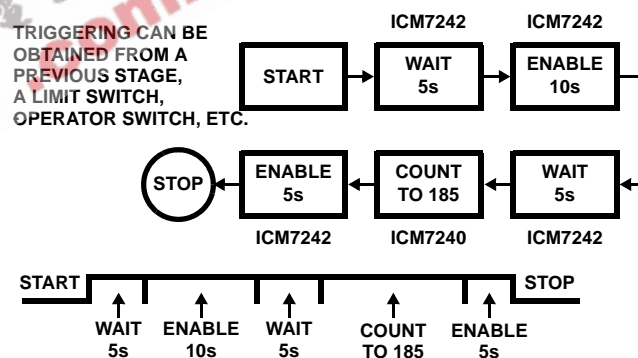


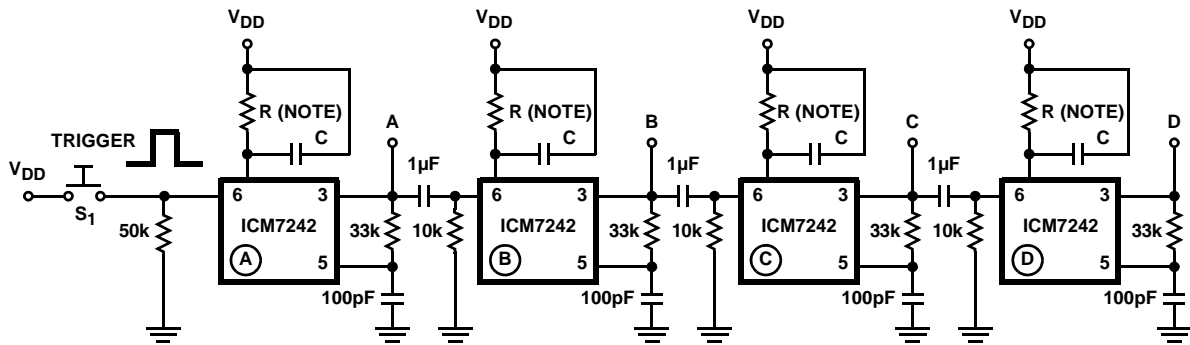
FIGURE 5. FLOW CHART FOR MACHINE TOOL CONTROLLER

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

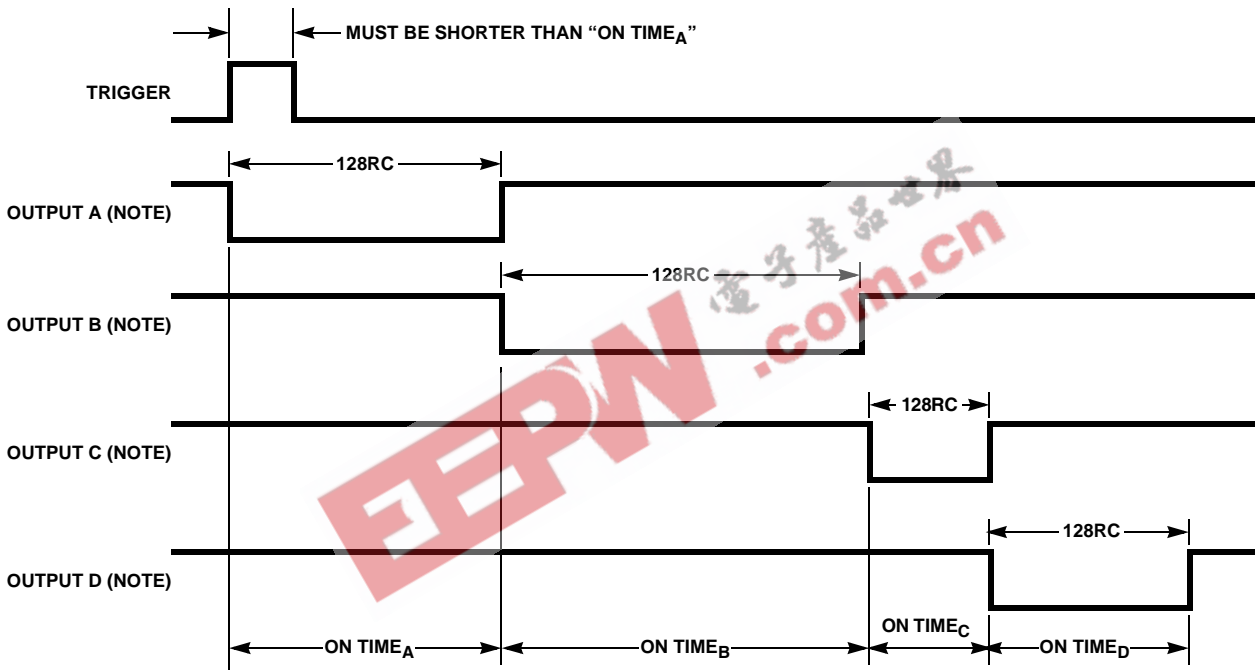
Sequence Timing

- Process Control
- Machine Automation
- Electro-Pneumatic Drivers
- Multi Operation (Serial or Parallel Controlling)

ICM7242



PUSH S_1 TO START SEQUENCE:



NOTE: Select RC values for desired "ON TIME" for each ICM7242.

FIGURE 6. SEQUENCE TIMER

Typical Performance Curves

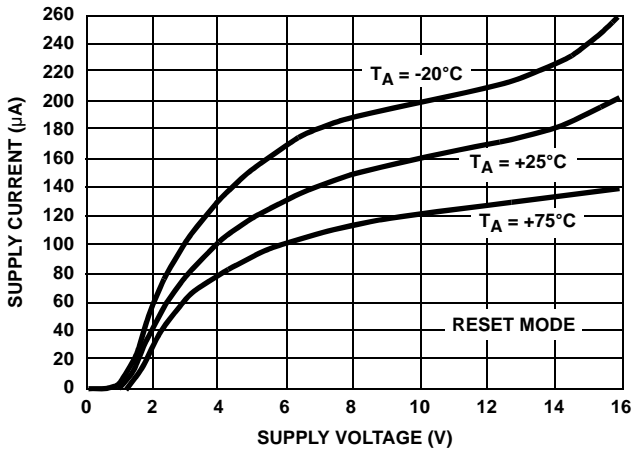


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

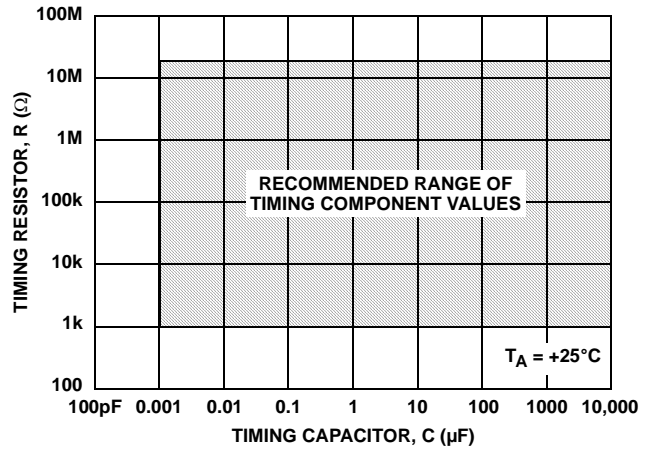


FIGURE 8. RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING

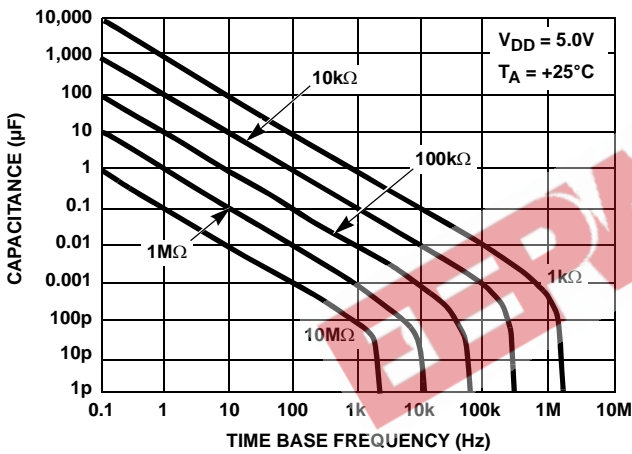


FIGURE 9. TIMEBASE FREE RUNNING FREQUENCY vs R AND C

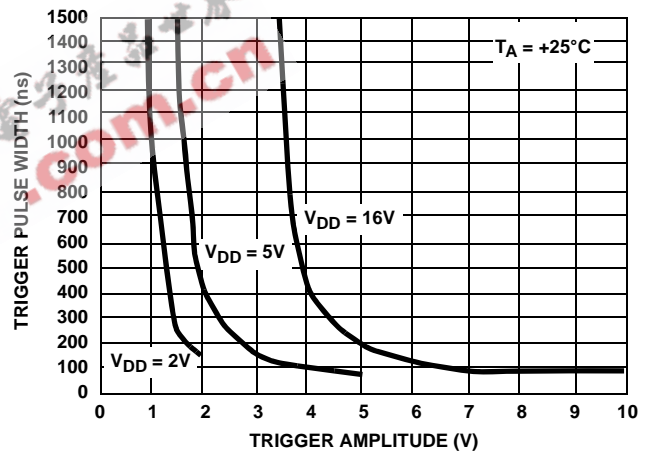


FIGURE 10. MINIMUM TRIGGER PULSE WIDTH vs TRIGGER AMPLITUDE

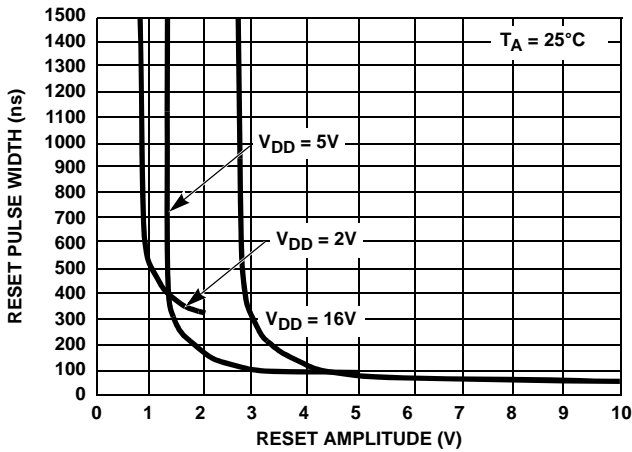


FIGURE 11. MINIMUM RESET PULSE WIDTH vs RESET AMPLITUDE

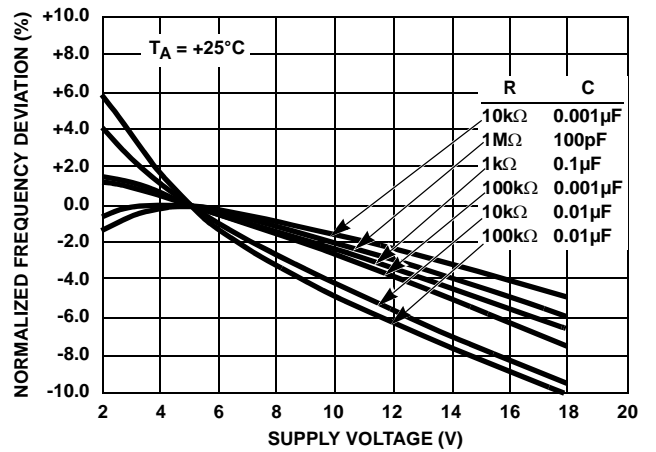


FIGURE 12. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

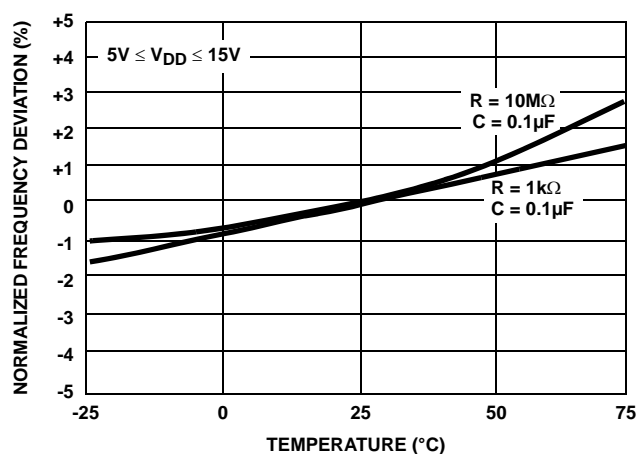


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

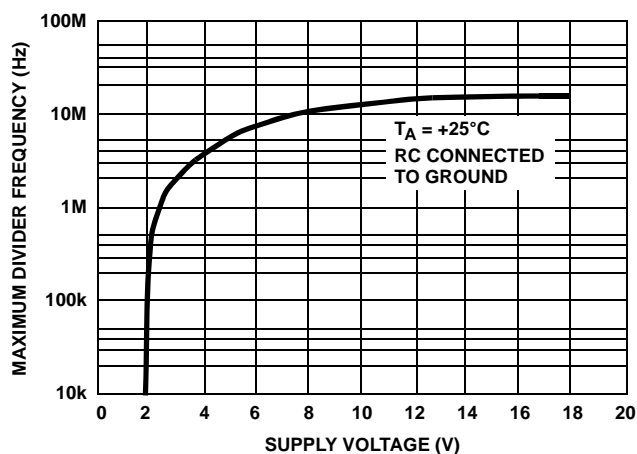


FIGURE 14. MAXIMUM DIVIDER FREQUENCY vs SUPPLY VOLTAGE

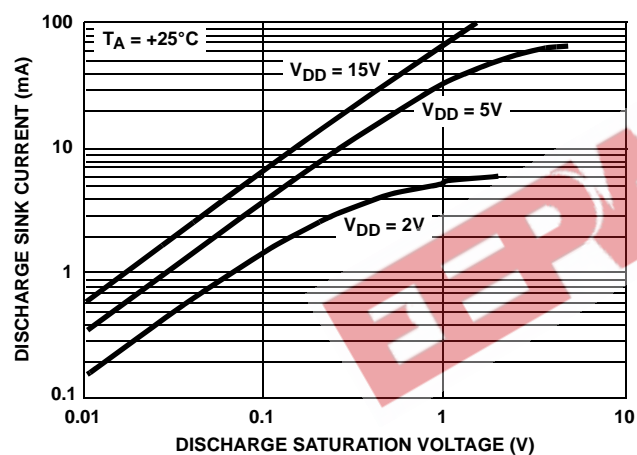


FIGURE 15. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

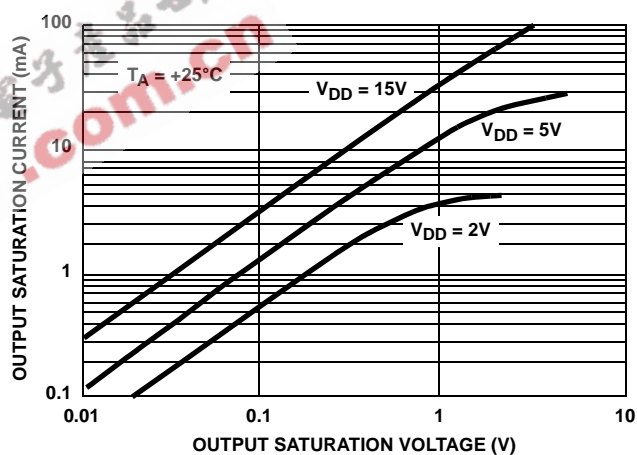
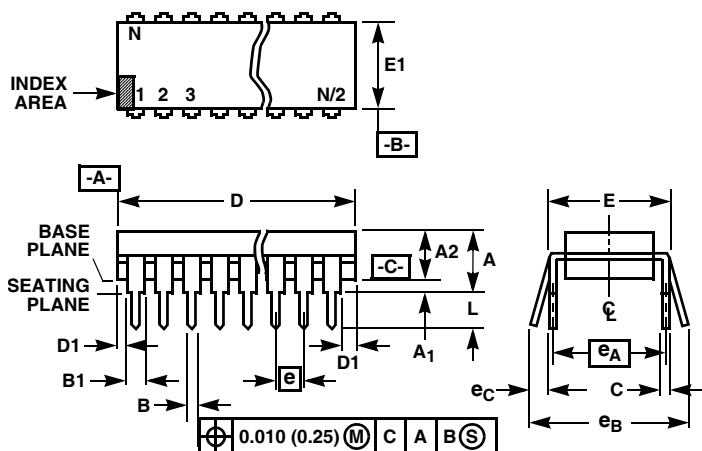


FIGURE 16. OUTPUT SATURATION CURRENT vs OUTPUT SATURATION VOLTAGE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

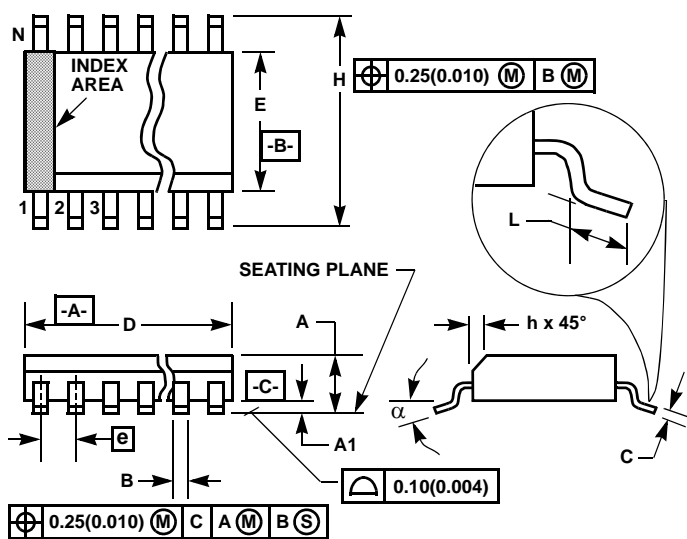
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|-------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| e_A | 0.300 BSC | | 7.62 BSC | | 6 |
| e_B | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

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Small Outline Plastic Packages (SOIC)

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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