PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840002-32

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840002-32 is a 2 output LVCMOS/LVTTL Synthesizer optimized to generate Fibre Channel or Serial ATA reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using an 18pF parallel resonant crystal, the following frequencies can be generated based on 1 frequency select pin (SEL): 106.25MHz and 75MHz, or 212.5MHz. The ICS840002-32 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Fibre Channel and Serial ATA jitter requirements. The ICS840002-32 is packaged in a small 8-pin TSSOP package.

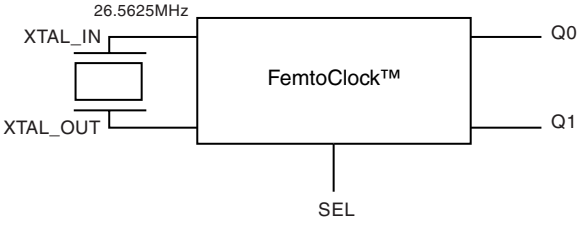
FEATURES

- Two LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Crystal oscillator interface
- Output frequency range: 75MHz and 106.25MHz, or 212.5MHz
- RMS phase jitter at 106.25MHZ (637kHz - 5MHz): 0.86ps (typical)
- Full 3.3V or 3.3V core/2.5V output supply mode
- 0°C to 70°C ambient operating temperature

SELECT FUNCTION TABLE

Input	Output Frequency Range (MHz)	
SEL	Q0	Q1
0	75	106.25
1	75	212.5

BLOCK DIAGRAM



PIN ASSIGNMENT

ICS840002-32

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Core supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface.
4	GND	Power		Power supply ground.
5, 7	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedence.
1	V_{DDO}	Power		Output supply pin.
8	SEL	Input	Pulldown	Select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDO} = 3.465V		TBD		pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V		TBD		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDO}	Output Supply Current			TBD		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	SEL		-0.3		0.8	V
I_{IH}	Input High Current	SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V ± 5\%$	2.6			V
			$V_{DDO} = 2.5V ± 5\%$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V$ or $2.5V ± 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range			212.5		MHz
				106.25		
				75		
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz @ Integration Range: 2.55MHz - 20MHz		0.50		ps
		106.25MHz @ Integration Range: 637kHz - 5MHz		0.86		ps
		75MHz @ Integration Range: 12kHz - 20MHz		TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

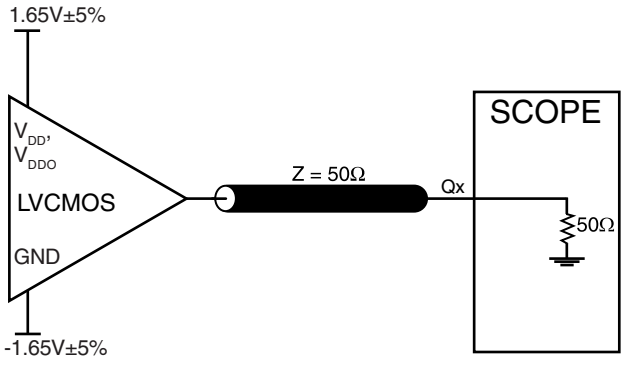
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, $T_A = 0°C$ TO $70°C$

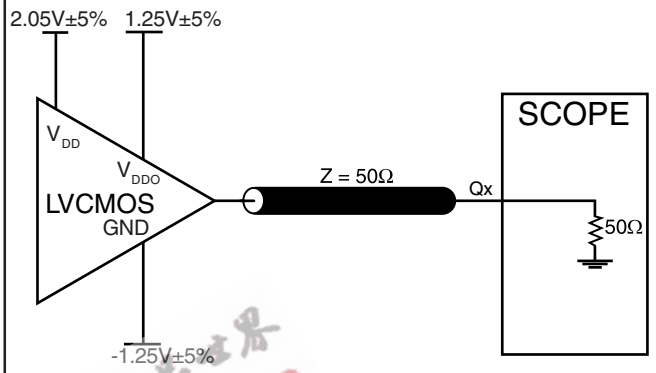
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range			212.5		MHz
				106.25		
				75		
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz @ Integration Range: 2.55MHz - 20MHz		0.57		ps
		106.25MHz @ Integration Range: 637kHz - 5MHz		1.1		ps
		75MHz @ Integration Range: 12kHz - 20MHz		TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		450		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

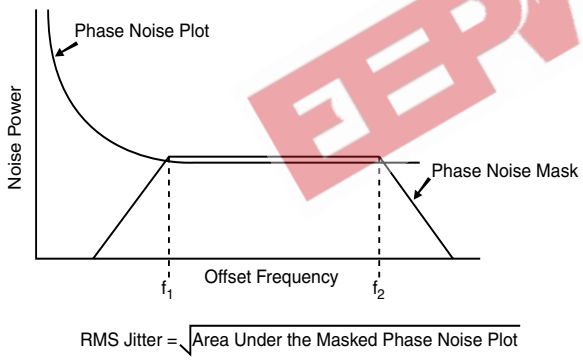
PARAMETER MEASUREMENT INFORMATION



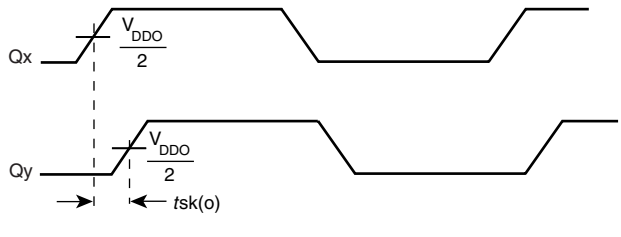
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



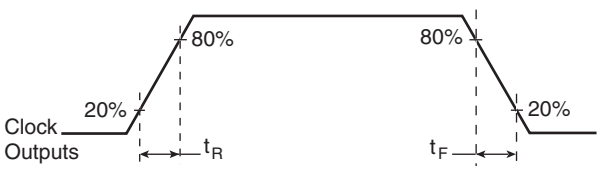
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



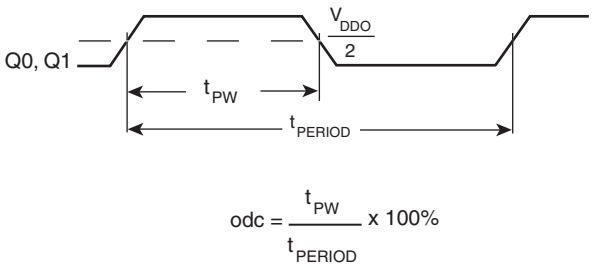
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The ICS840002-32 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

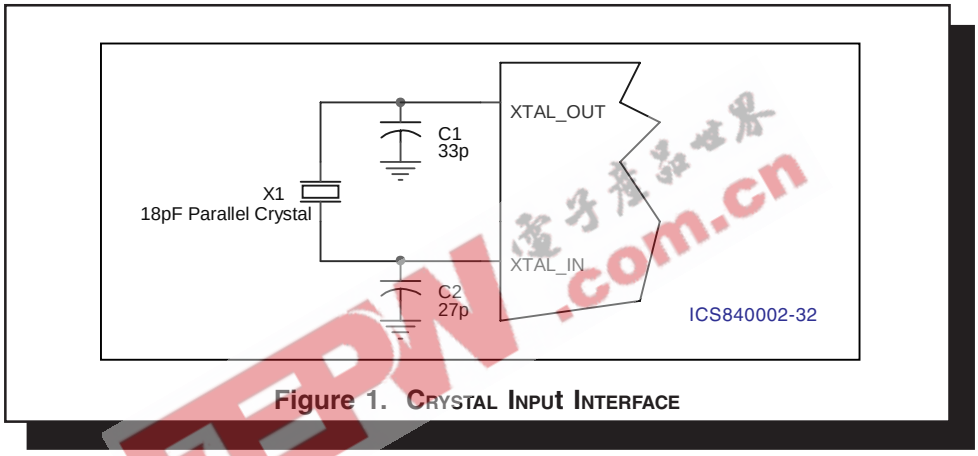


Figure 1. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters Per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS840002-32 is: 2322

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

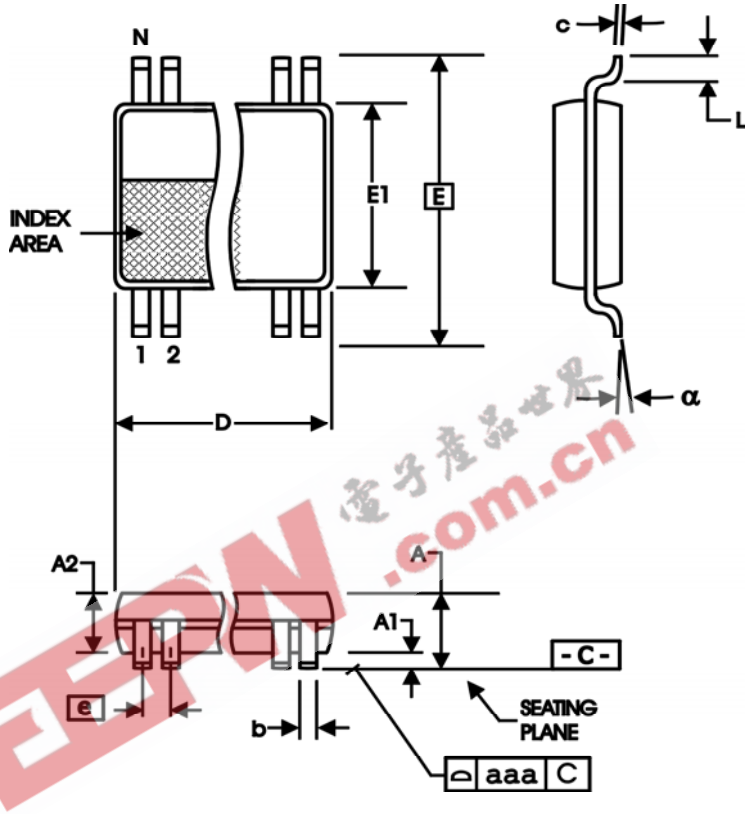


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840002BG-32	02B32	8 lead TSSOP	tube	0°C to 70°C
ICS840002BG-32T	02B32	8 lead TSSOP	2500 tape & reel	0°C to 70°C