PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844031I-01

FEMTOCLOCKS™ CRYSTAL-TO- LVDS CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS844031I-01 is an Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS844031I-01 uses an 18pF parallel resonant crystal over the range of 19.6MHz - 27.2MHz. For Ethernet applications, a 25MHz crystal is used to generate 312.5MHz. The ICS844031I-01 has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The ICS844031I-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

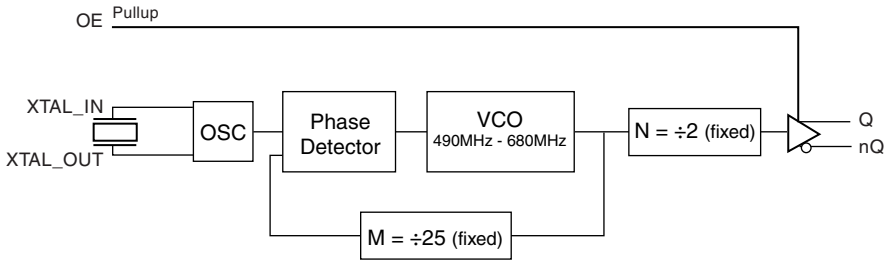
FEATURES

- (1) Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (19.6MHz - 27.2MHz)
- Output frequency range: 245MHz - 340MHz
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.49ps (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature

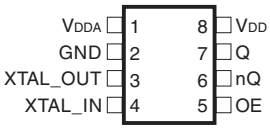
COMMON CONFIGURATION TABLE

Inputs				Output Frequency (MHz)
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	
25	25	2	12.5	312.5

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS844031I-01

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q0/nQ0 output is active. When LOW, the Q0/nQ0 output is in a high impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			40		mV
V_{OS}	Offset Voltage			1.25		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.2		V
ΔV_{OS}	V_{OS} Magnitude Change			40		mV

NOTE: Please refer to Parameter Measurement Information for output information.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.6		27.2	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.49		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		ps
odc	Output Duty Cycle			50		%

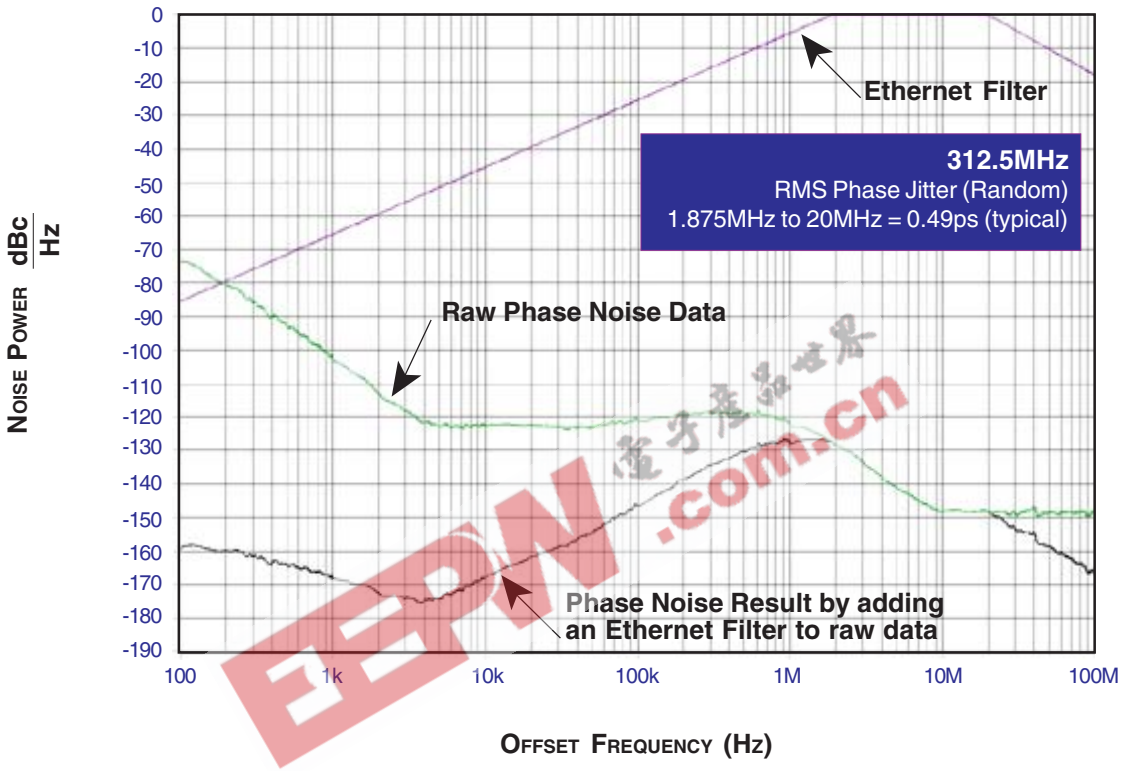
NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 2.5V±5%, T_A = -40°C TO 85°C

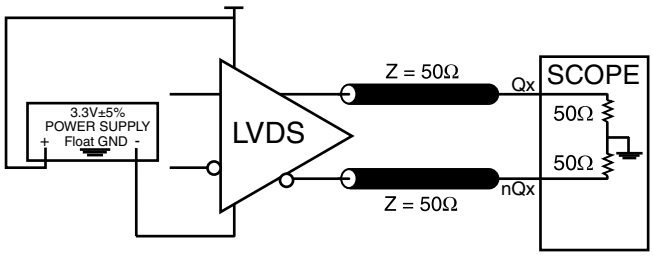
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.70		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

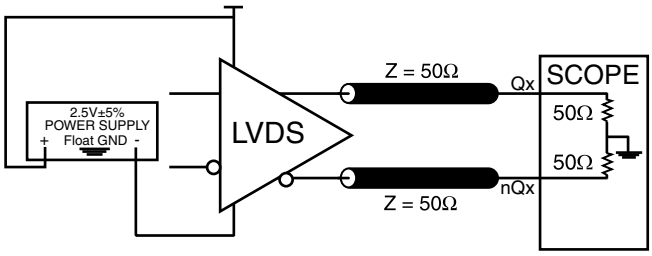
TYPICAL PHASE NOISE AT 312.5MHZ



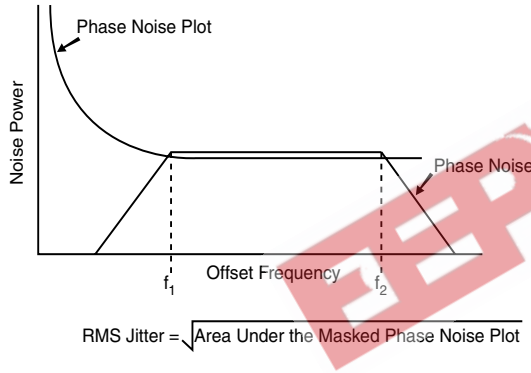
PARAMETER MEASUREMENT INFORMATION



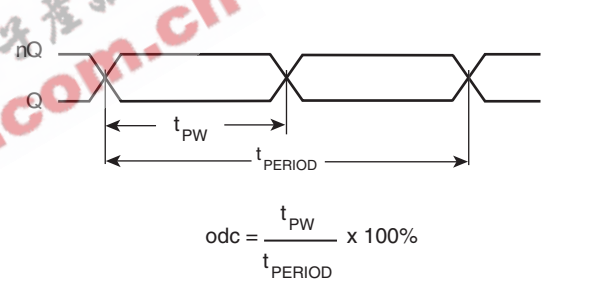
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



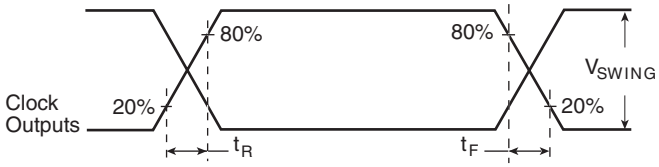
LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT



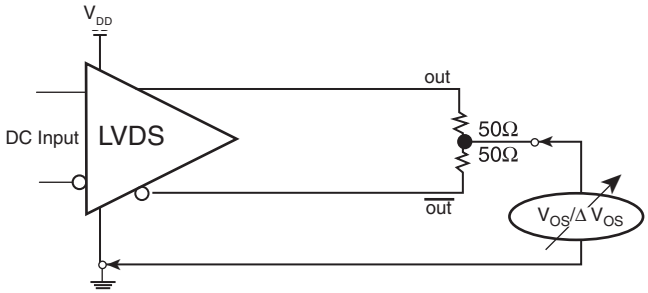
RMS PHASE JITTER



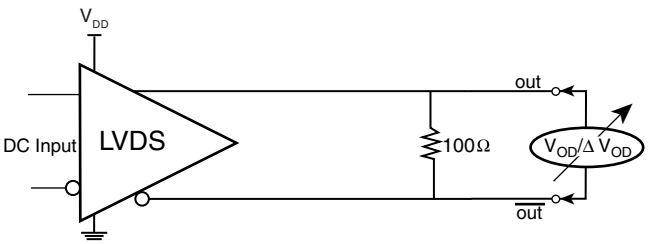
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844031I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

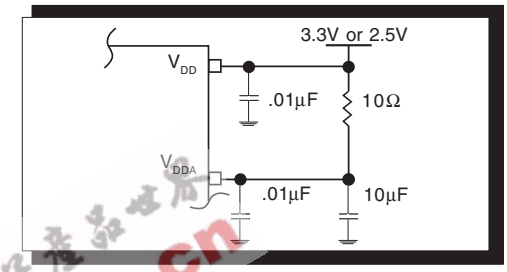


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844031I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

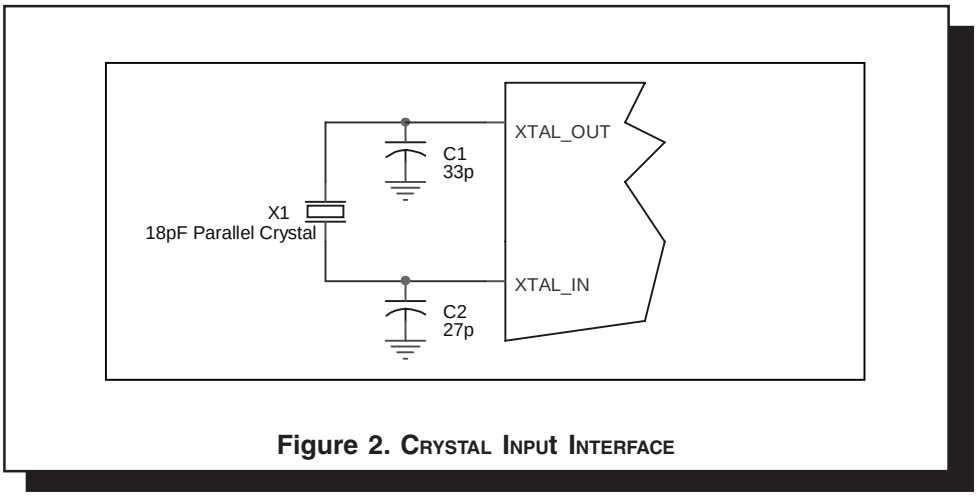


Figure 2. CRYSTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

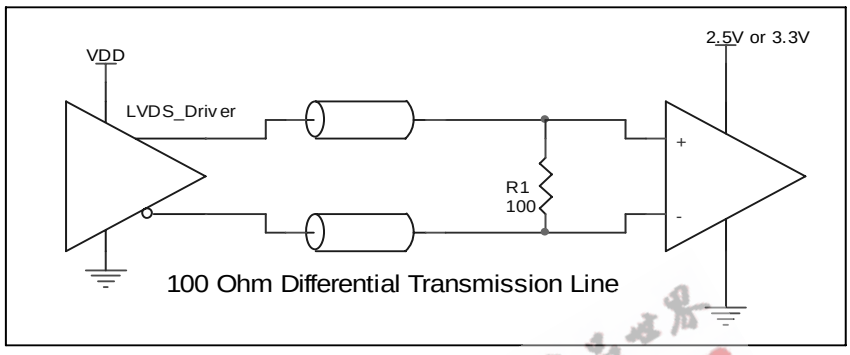


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

APPLICATION SCHEMATIC

Figure 4A provides a schematic example of ICS844031I. In this example, an 18 pF parallel resonant crystal is used. The C1=22pF and C2=22pF are recommended for frequency. The C1 and C2 values may be slightly adjusted for optimizing frequency accuracy. At least one decoupling capacitor near the power pin is required. Suggested value range is from 0.01uF to 0.1uF. Other filter type can be added depending on the system power supply noise type.

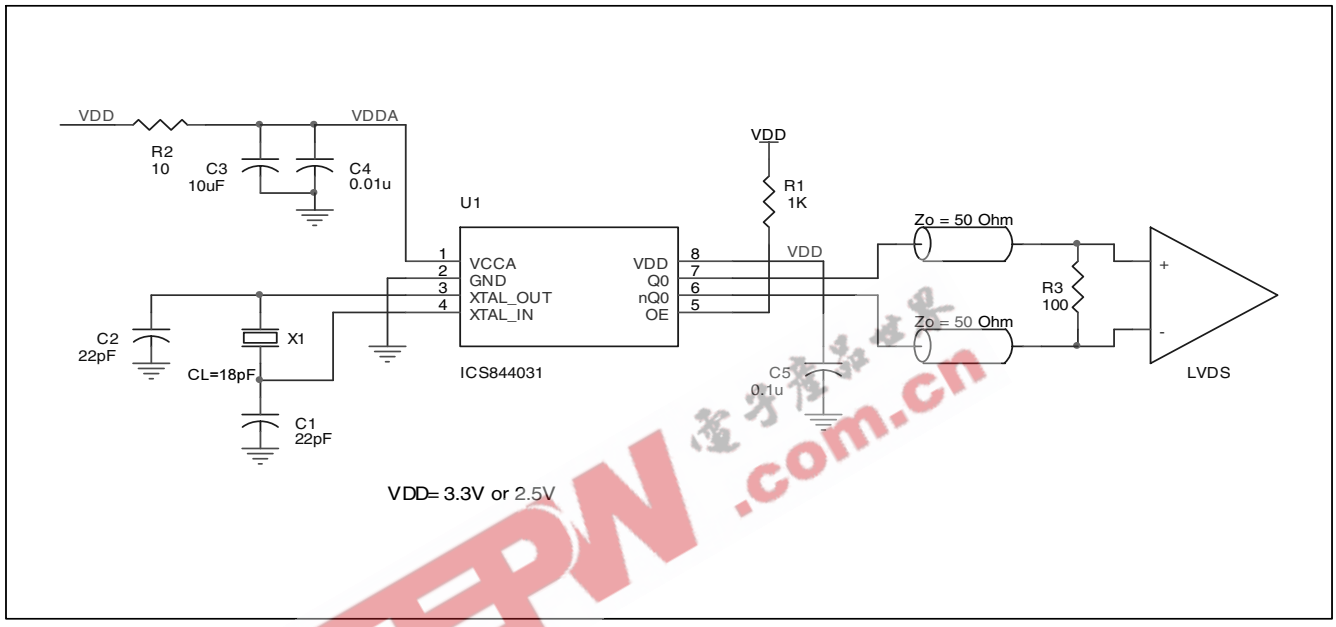


FIGURE 4A. APPLICATION SCHEMATIC EXAMPLE

PC BOARD LAYOUT EXAMPLE

Figure 4B shows an example of ICS844031I P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

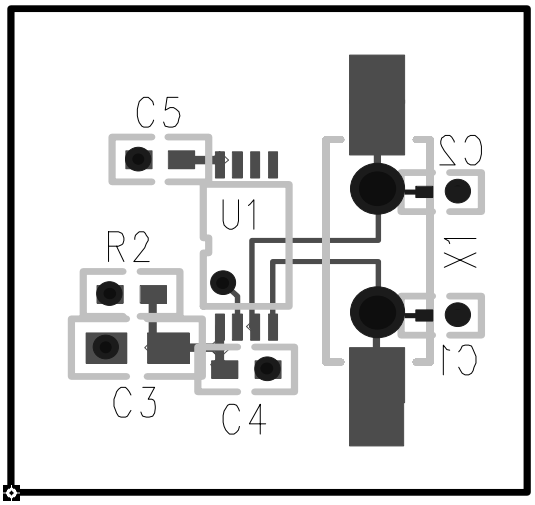


FIGURE 4B. ICS843001 PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

NOTE: Table 6, lists component sizes shown in this layout example.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS844031I-01 is: 2519

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

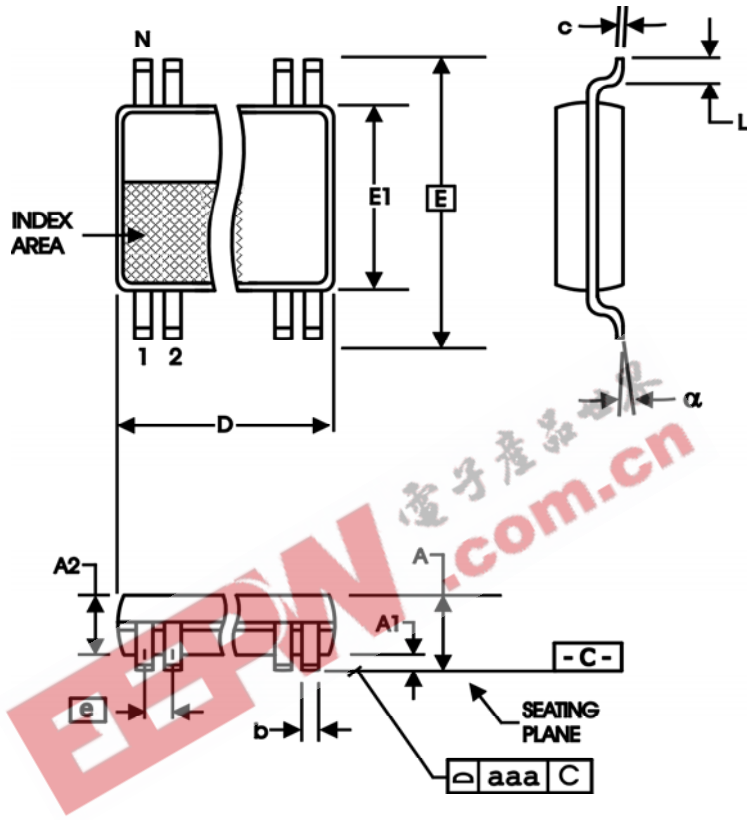


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844031AGI-01	TBD	8 lead TSSOP	tube	-40°C to 85°C
ICS844031AGI-01T	TBD	8 lead TSSOP	2500 tape & reel	-40°C to 85°C