FEATURES

- 12/10/8-Bit Monotonic Quad DACs in 16 lead QSOP Package
- Wide Output Voltage Swing
- 150 µA per DAC at 5V Supply
- 100 µA per DAC at 3V Supply
- On Board Reference
- Three-wire SPI Interface
- Serial Data Out for Daisy-Chaining
- 8µs Full-Scale Settling Time

APPLICATIONS

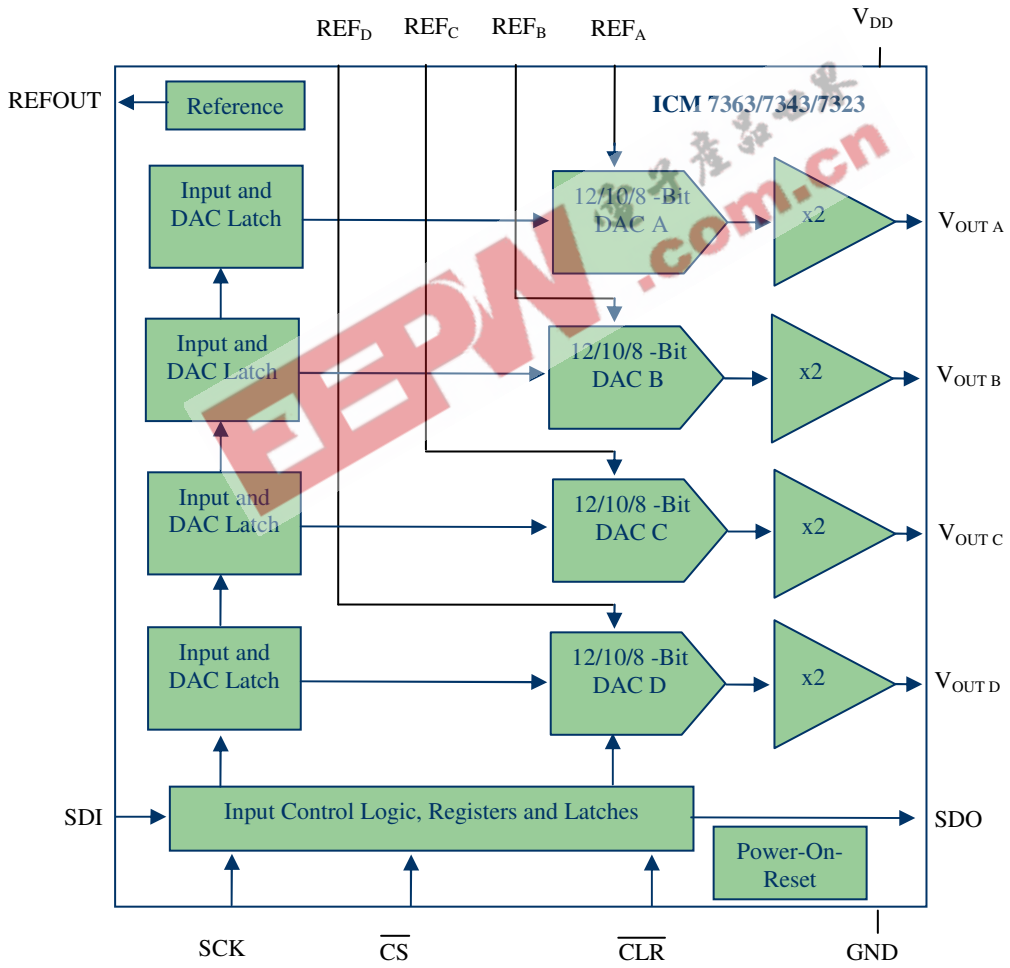
Battery-Powered Applications
Industrial Process Control
Digital Gain and Offset Adjustment

OVERVIEW

The ICM7363, ICM7343 and ICM7323 are Quad 12-Bit, 10-Bit and 8-Bit wide output voltage swing DACs respectively, with guaranteed monotonic behavior. They include a 1.25V reference for ease of use and flexibility. The reference output is available on a separate pin and can be used to drive the reference input of each DAC. Alternately, each DAC can be driven by an external reference. There is a wide operating supply range of 2.7V to 5.5V.

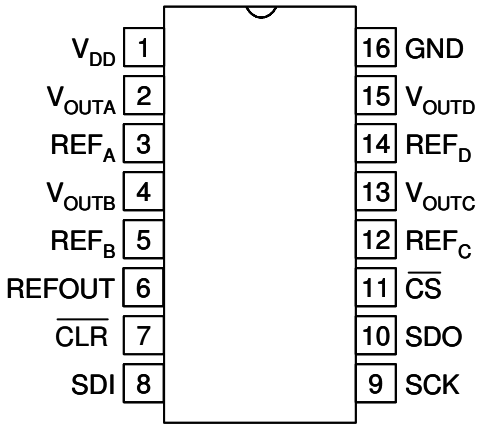
The input interface is an easy to use three-wire SPI/QSPI compatible interface. Each DAC can be individually controlled and has a double buffered digital input. There is a serial data output to allow for daisy-chaining applications.

BLOCK DIAGRAM



PACKAGE

16-Pin QSOP



PIN DESCRIPTION

Pin No	Symbol	Description
1	V_{DD}	**Supply Voltage**
2	$V_{OUT\ A}$	**DAC A Output**
3	REF_{A}	**DAC A Reference Input**
4	$V_{OUT\ B}$	**DAC B Output**
5	REF_{B}	**DAC B Reference Input**
6	REFOUT	**Reference Output (1.25V)**
7	$\overline{CLR}$	**Clear Input (TTL or CMOS)**
8	SDI	**Serial Data Input (TTL or CMOS)**
9	SCK	**Serial Clock Input (TTL or CMOS)**
10	SDO	**Serial Data Output**
11	$\overline{CS}$	**Chip Select (TTL or CMOS)**
12	REF_{C}	**DAC C Reference Input**
13	$V_{OUT\ C}$	**DAC C Output**
14	REF_{D}	**DAC D Reference Input**
15	$V_{OUT\ D}$	**DAC D Output**
16	GND	**Ground**

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (SCK, SDI, $\overline{CS}$, $\overline{CLR}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C

T_{SOL}	Soldering Temperature	300	°C

Note: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Temperature Range	Package
ICM7363	-40 °C to 85 °C	16-Pin QSOP
ICM7343	-40 °C to 85 °C	16-Pin QSOP
ICM7323	-40 °C to 85 °C	16-Pin QSOP

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, $V_{REF\ IN}$ = 1.25V ; V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
ICM7363						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7343						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7323						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
GE	Gain Error				±0.5	% of FS
OE	Offset Error				±25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	(Note 4)		1.2	2.5	mA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
	Output Voltage Range	(Note 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
R_{OUT}	Amp Output Impedance	At Mid-scale At Zero-scale		1.0 100	5.0 200	Ω Ω
	Output Line Regulation	Vdd=2.7 to 5.5 V		0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	2.4			V
V_{IL}	Digital Input Low	(Note 2)			0.8	V
	Digital Input Leakage				5	μA
REFERENCE						
R_{IN}	Reference Input Resistance		25	41	65	kΩ
	Reference Input Range	(Note 2)	0.5		V_{DD} -1.5	V
V_{REFOUT}	Reference Output		1.2	1.25	1.3	V
	Reference Output Line Regulation	Vdd=2.7 to 5.5 V		0.8	4.0	mV/V

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, $V_{REF\ IN}$ = 1.25V ; V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			2		V/µs
	Settling Time	Full-scale settling		8		µs
	Mid-scale Transition Glitch Energy			40		nV-S

Note 1: Linearity is defined from code 64 to 4095 (ICM7363)
Linearity is defined from code 16 to 1023 (ICM7343)
Linearity is defined from code 4 to 255 (ICM7323)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information
Note 4: All digital inputs are either at GND or Vdd

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t1	SCK Cycle Time	(Note 2)	30			ns
t2	Data Setup Time	(Note 2)	10			ns
t3	Data Hold Time	(Note 2)	10			ns
t4	SCK Falling edge to $\overline{CS}$ Rising Edge	(Note 2)	0			ns
t5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	15			ns
t6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns
t7	$\overline{CLR}$ Pulse Width	(Note 2)	20			ns
t8	SDO Delay	(Note 2)			100	ns

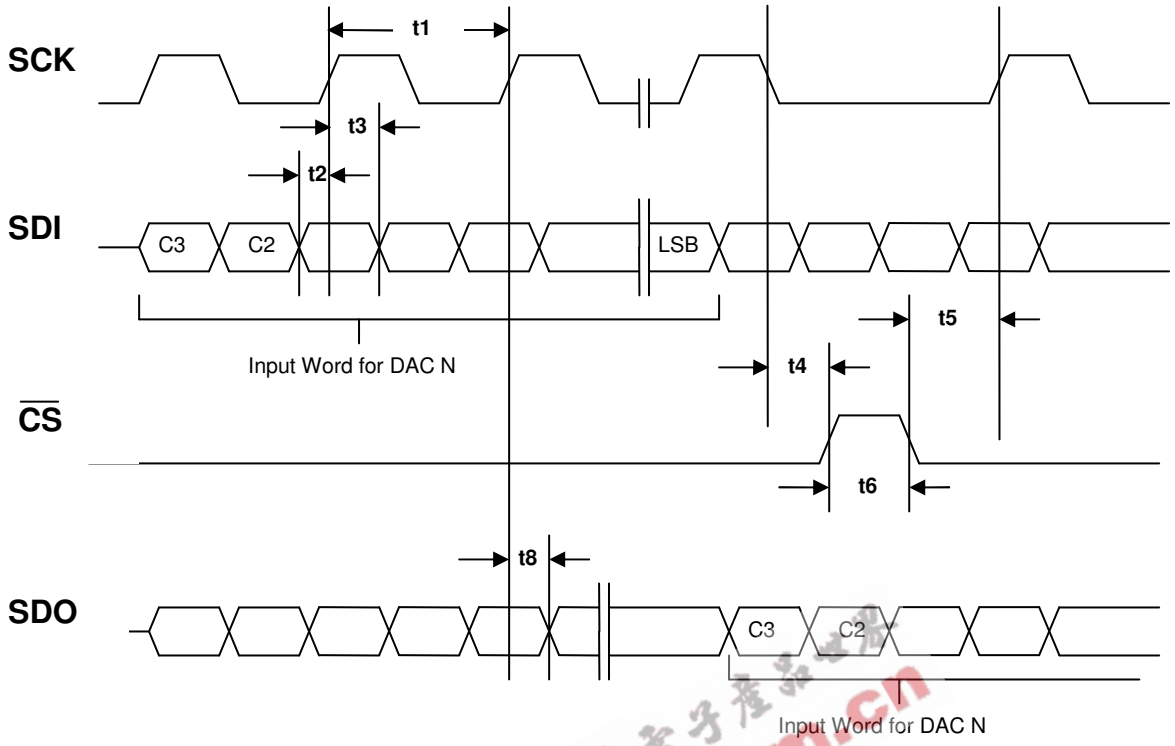


Figure 1: Serial Interface Timing Diagram

CONTENTS OF INPUT SHIFT REGISTER

ICM7363 (12-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2: Contents of ICM7363 Input Shift Register

ICM7343 (10-Bit DAC)

MSB														LSB	
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

Figure 3: Contents of ICM7343 Input Shift Register

ICM7323 (8-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

Figure 4: Contents of ICM7323 Input Shift Register

C3	C2	C1	C0	DATA	DAC	FUNCTION
0	0	0	0	Data	A	Load Input Latch
0	0	0	1	Data	A	Update DAC
0	0	1	0	Data	A	Load Input Latch and Update DAC
0	0	1	1	Data	B	Load Input Latch
0	1	0	0	Data	B	Update DAC
0	1	0	1	Data	B	Load Input Latch and Update DAC
0	1	1	0	Data	C	Load Input Latch
0	1	1	1	Data	C	Update DAC
1	0	0	0	Data	C	Load Input Latch and Update DAC
1	0	0	1	Data	D	Load Input Latch
1	0	1	0	Data	D	Update DAC
1	0	1	1	Data	D	Load Input Latch and Update DAC
1	1	0	0	Data	A-D	Load Input Latch
1	1	0	1	Data	A-D	Update DAC
1	1	1	0	Data	A-D	Load Input Latch and Update DAC
1	1	1	1	X	X	No Operation

Table 1: Serial Interface Control Command

DETAILED DESCRIPTION

The ICM7363 is a 12-bit quad voltage output DAC. The ICM7343 is the 10-bit version of this family and the ICM7323 is the 8-bit version.

This family of DACs employs a resistor string architecture guaranteeing monotonic behavior. There is a 1.25V onboard reference and a wide operating supply range of 2.7V to 5.5V.

Reference Input and Output

Each DAC has its own reference input pin which can be driven from ground to V_{DD} -1.5V. The input resistance on each of these pins is typically 41 kΩ. There is a gain of two in the output amplifiers which means they swing from ground at code 0 to 2 x $V_{REF\ IN}$ at full-scale :

$$Vout = 2 \times (V_{REF\ IN} \times D)/2^n$$

Where D=digital input (decimal) and n= number of bits, i.e. 12 for ICM7363, 10 for ICM7343 and 8 for ICM7323.

There is also an onboard band-gap reference on all these parts. This reference output is nominally 1.25V and is brought out to a separate pin, REFOUT and can be used to drive the reference input of the DACs. The outputs will nominally swing from 0 to 2.5V when using this reference.

Output Amplifier

Each DAC has its own output amplifier with a wide output voltage swing. The actual swing of the output amplifier will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The amplifiers are configured in a gain of 2 with internal gain resistors of about 50 kΩ. The output swing will be from 0V to 2 x $V_{REF\ IN}$ at full-scale.

The output amplifier can drive a load of 2.0 kΩ to V_{DD} or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 8 µs and it dissipates about 150 µA with a 5V supply voltage.

Serial Interface and Input Logic

This quad DAC family uses a standard 3-wire connection compatible with SPI/QSPI interfaces. There is also a serial data output pin that allows daisy-chaining. Data is loaded in 16-bit words which consist of 4 address and control bits (MSBs) followed by 12 bits of data (see table 1). The ICM7343 has the last two LSBs as don't cares and the ICM7323 has the last 4 LSBs as don't cares. Each DAC is double buffered with an input latch and a DAC latch.

All the digital inputs are CMOS/TTL compatible. The current dissipation of the device however, will be higher when the inputs are driven at TTL levels.

The output of the 16-bit input shift register is available at the SDO pin. Data is clocked in on the rising edge of SCK which has a Schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The $\overline{CS}$ pin must be low when data is being clocked into the part. After the 16th clock pulse the $\overline{CS}$ pin must be pulled high (level-triggered) for the data to be transferred to an input bank of latches. The $\overline{CS}$ pin also disables the SCK pin internally when pulled high and the SCK pin must be low before the $\overline{CS}$ pin is pulled back low. As the $\overline{CS}$ pin is pulled high the shift register contents are transferred to a bank of 16 latches. The 4 bit control word (C3~C0) is then decoded and the appropriate DAC is updated or loaded depending on the control word (see Table 1).

Each DAC has a double-buffered input with an input latch and a DAC latch. The DAC output will swing to its new value when data is loaded into the DAC latch. For each DAC, the user has three options: loading only the input latch, updating the DAC with data previously loaded into the input latch or loading the input latch and updating the DAC at the same time with a new code. The user also has the ability to perform this operation simultaneously for all DACs as shown in Table 1.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage outputs will go to ground. The $\overline{CLR}$ pin will also perform this same operation asynchronously when it is pulled low.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD} however, offset and gain error limit this ability. Figure 5 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a deadband area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 6 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a deadband of codes close to full-scale. This can be avoided by using a reference voltage slightly less then 0.5 x V_{DD} ensuring that the full-scale of the DAC is always less than V_{DD}.

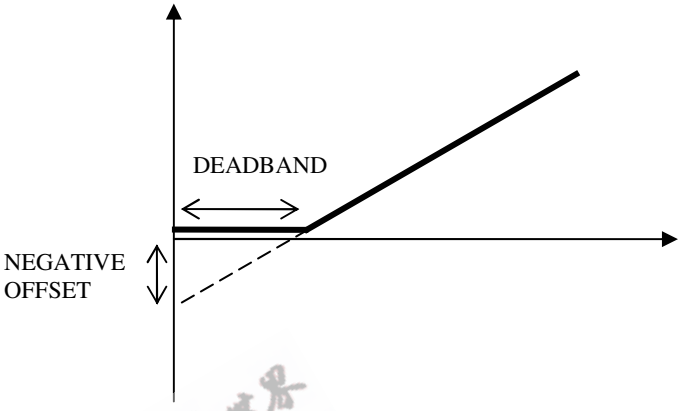


Figure 5: Effect of Negative Offset

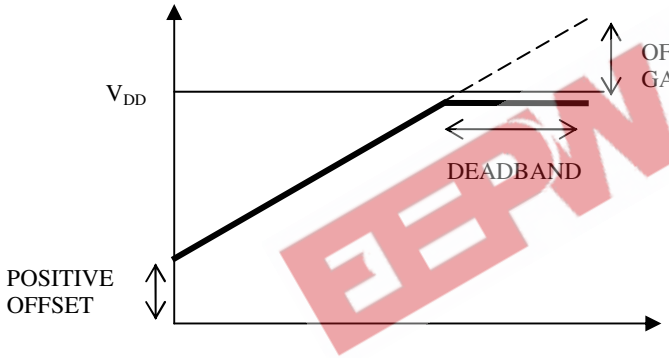
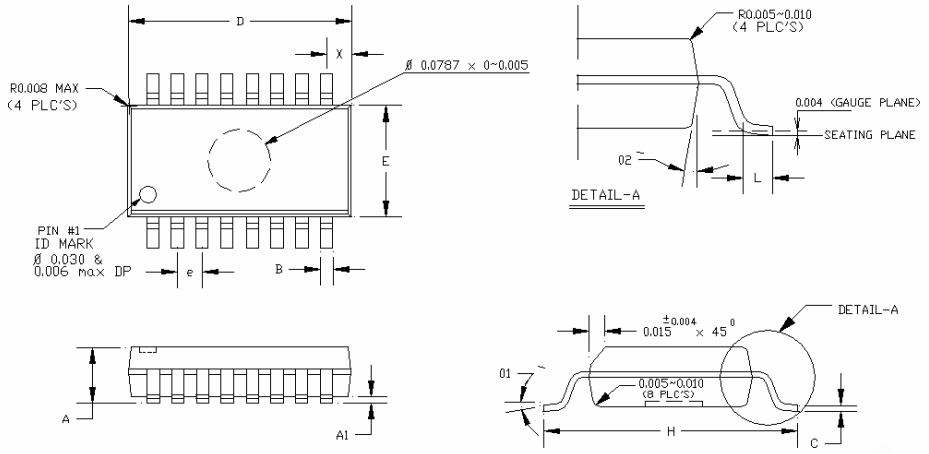


Figure 6: Effect of Gain Error and Positive Offset

PACKAGE INFORMATION



SYMBOL	16 QSOP	
	MIN	MAX
A	0.053	0.068
A1	0.004	0.010
B	0.008	0.012
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.025 BSC	
C	0.007	0.009
L	0.016	0.034
X	0.009 REF	
θ1	0^0	8^0
θ2	7^0 BSC	

NOTE:

1. LEAD COPLANARITY SHOULD BE 0 TO 0.004" MAX.
2. PACKAGE SURFACE FINISHING:
   (2.1) TOP: MATTE (CHARMILLES # 24~27)
   (2.2) ALL SIDE: MATTE (CHARMILLES # 24~27)
   (2.3) BOTTOM: MATTE (CHARMILLES # 24~27)
3. ALL DIMENSION EXCLUDING MOLD FLASHES.
4. MAX DEVIATION OF CENTRE OF PACKAGE AND CENTRE OF LEADFRAME TO BE 0.004".
5. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTRE OF PACKAGE TO BE 0.004".
6. THE LEAD WIDTH, B TO BE DETERMINED AT 0.0075" FROM THE LEAD TIP.

ORDERING INFORMATION