ICM7372/7352/7332

DUAL 12/10/8-BIT VOLTAGE-OUTPUT DACS with Serial Interface and Adjustable Output Offset

FEATURES

- 12/10/8-Bit Monotonic Dual DAC in 16 Lead QSOP Package
- Adjustable Output Offset
- Wide Output Voltage Swing
- 100 µA per DAC at 3V Supply
- On Board Reference
- Three-wire SPI/QSP and Microwire Interface Compatible
- Serial Data Out for Daisy-Chaining
- 8 µS Full scale Settling Time

APPLICATIONS

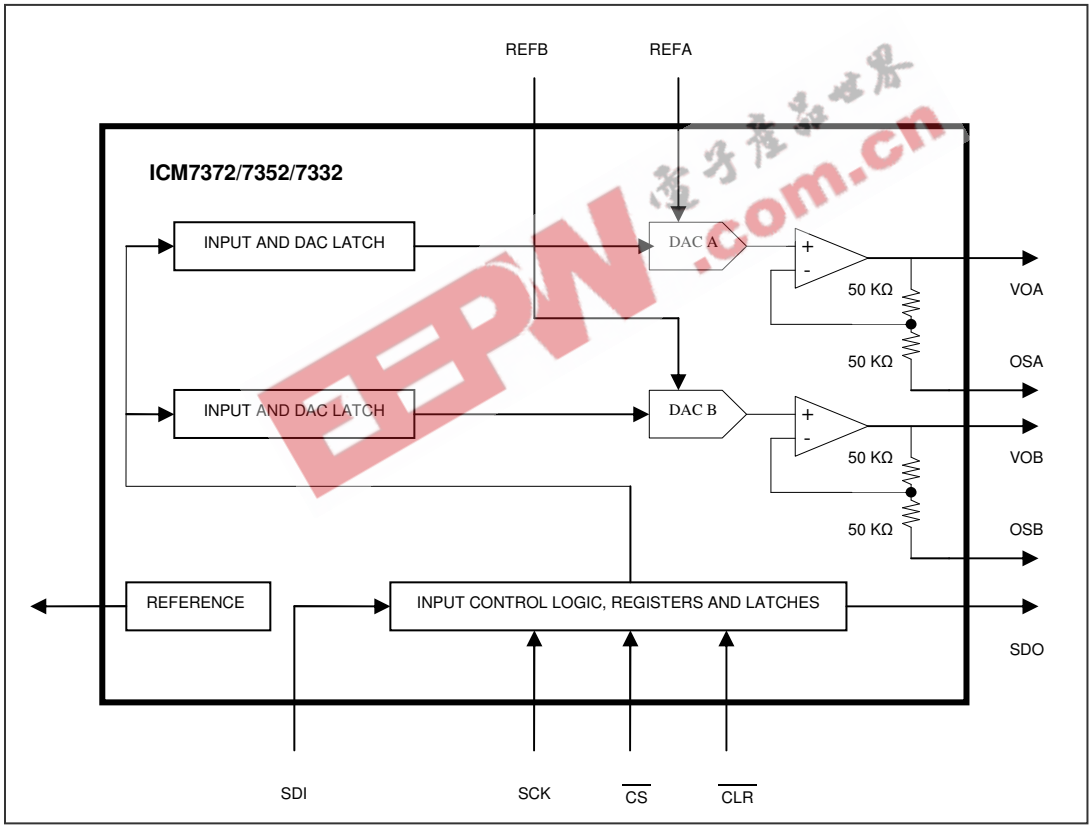
Battery-Powered Applications
Industrial Process Control
Digital Gain and Offset Adjustment

OVERVIEW

The ICM7372, ICM7352 and ICM7332 are 12-Bit, 10-Bit and 8-Bit voltage output DACs respectively, with guaranteed monotonic behavior. These DACs are available in 16-pin QSOP package. They include adjustable output offset for ease of use and flexibility. The reference output is available on a separate pin and can be used to drive external loads. The operating supply range is 2.7V to 5.5V.

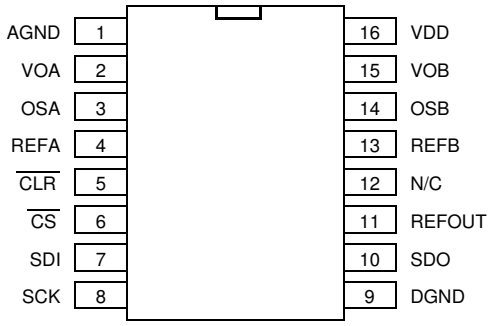
The input interface is an easy to use three-wire SPI/QSPI and Microwire compatible interface. The DAC has a double buffered digital input for added flexibility.

BLOCK DIAGRAM



PACKAGE

16 Lead QSOP



TOP VIEW

PIN DESCRIPTION (16 Lead QSOP)

Pin	Name	I/O	Description
1	AGND	I	Analog Ground
2	VOA	O	DAC A Output Voltage
3	OSA	I	DAC A Offset Adjustment
4	REFA	I	Reference Voltage Input to DAC A
5	$\overline{CLR}$	I	Active Low Clear Input (CMOS). Resets All Registers to Zero. DAC outputs go to 0 V
6	$\overline{CS}$	I	Active Low Chip Select (CMOS)
7	SDI	I	Serial Data Input (CMOS)
8	SCK	I	Serial Clock Input (CMOS)
9	DGND	I	Digital Ground
10	SDO	O	Serial data Output
11	REFOUT	O	Reference Output
12	N/C	-	No Connection
13	REFB	I	Reference Voltage Input to DAC B
14	OSB	I	DAC B Offset Adjustment
15	VOB	O	DAC B Output Voltage
16	VDD	I	Supply Voltage

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (SCK, SDI, $\overline{CLR}$, $\overline{CS}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SOL}	Soldering Temperature	300	°C

Note: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Operating Temperature Range	Package
ICM7372	-40 °C to 85 °C	16-Pin QSOP
ICM7352	-40 °C to 85 °C	16-Pin QSOP
ICM7332	-40 °C to 85 °C	16-Pin QSOP

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
DC PERFORMANCE						
ICM7372						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7352						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7332						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
GE	Gain Error				±0.5	% of FS
OE	Offset Error				±25	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7		5.5	V
I_{DD}	Supply Current	(Note 4)		0.6	1.5	mA

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
OUTPUT CHARACTERISTICS						
	Output Voltage Range	(Note 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
R_{OUT}	Amp Output Impedance	At Mid-scale (Note 2) At 0-scale (Note 2)		1.0 100	5.0 200	Ω Ω
	Output Line Regulation	V_{DD}=2.7 to 5.5 V		0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	2.4			V
V_{IL}	Digital Input Low	(Note 2)			0.8	V
	Digital Input Leakage				5	μA
REFERENCE						
V_{REFOUT}	Reference Output		1.2	1.25	1.3	V
	Reference Output Line Regulation			0.8	4.0	mV/V

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
SR	Slew Rate			2		V/μs
	Settling Time	Full-scale settling		8		μs
	Mid-scale Transition Glitch Energy			40		nV-S

Note 1: Linearity is defined from code 64 to 4095 (ICM7372)
Linearity is defined from code 16 to 1023 (ICM7352)
Linearity is defined from code 4 to 255 (ICM7332)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information
Note 4: All digital Inputs at GND or V_{DD}

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	SCK Cycle Time	(Note 2)	30			ns
t_2	Data Setup Time	(Note 2)	10			ns
t_3	Data Hold Time	(Note 2)	10			ns
t_4	SCK Falling edge to $\overline{CS}$ Rising Edge	(Note 2)	0			ns
t_5	$\overline{CS}$ Falling Edge to SCK Rising Edge	(Note 2)	15			ns
t_6	$\overline{CS}$ Pulse Width	(Note 2)	20			ns
t_7	SDO Delay	(Note 2)			100	ns

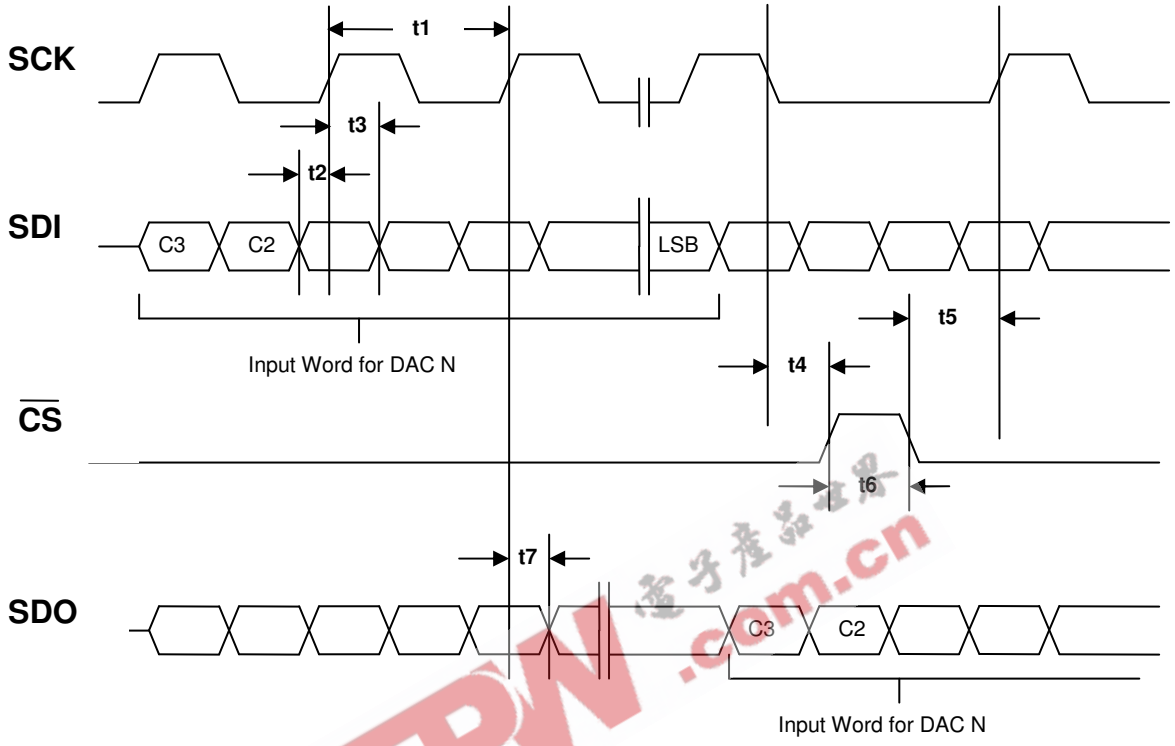


Figure 1. Serial Interface Timing Diagram

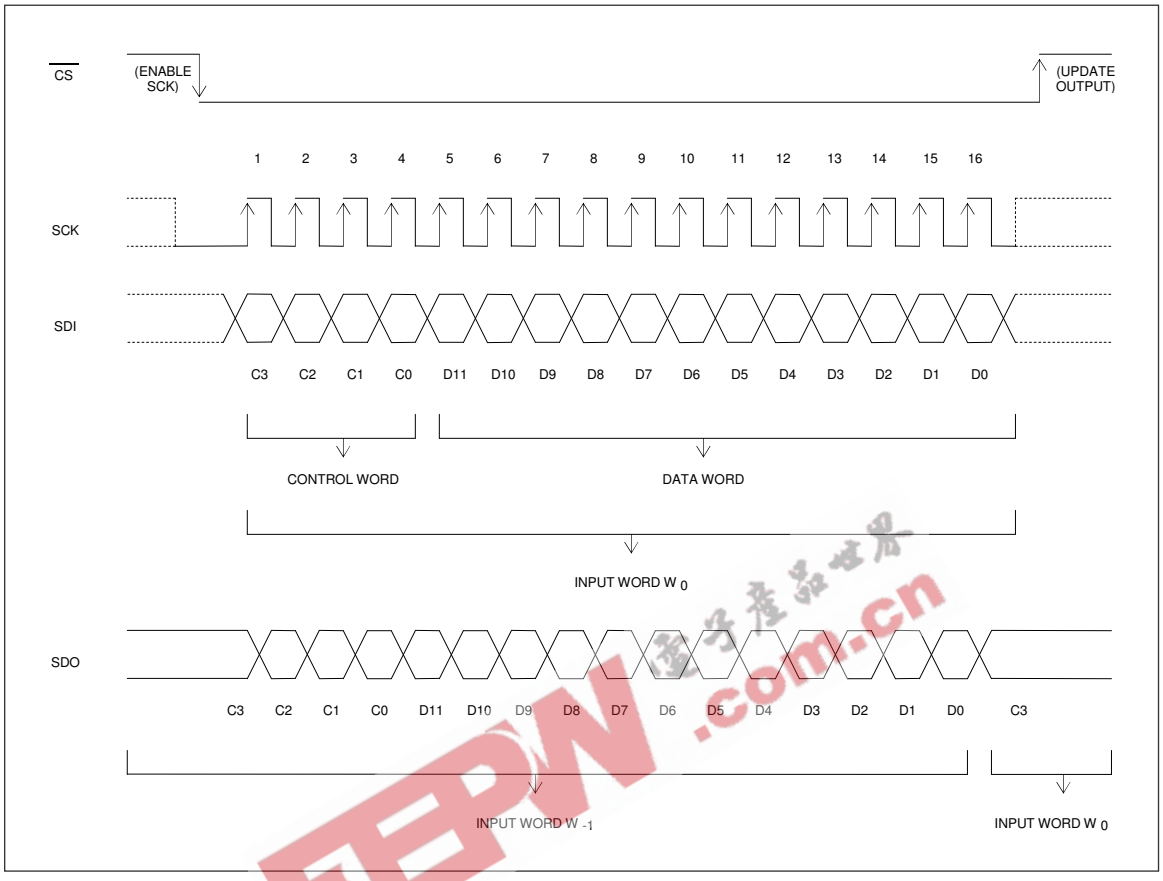


Figure 2. Serial Interface Operation Diagram

CONTENTS OF INPUT SHIFT REGISTER

ICM7372 (12-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL WORD				DATA WORD											

Figure 3. Contents of ICM7372 Input Shift Register

ICM7352 (10-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
CONTROL WORD				DATA WORD										X	X

Figure 4. Contents of ICM7352 Input Shift Register

ICM7332 (8-Bit DAC)

MSB															LSB
C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
CONTROL WORD				DATA WORD								X	X	X	X

Figure 5. Contents of ICM7332 Input Shift Register

C3	C2	C1	C0	DATA (D11 – D0)	FUNCTION
0	0	0	0	Data	Load Input Latch DAC A
0	0	0	1	Data	Update DAC A
0	0	1	0	Data	Load Input Latch and Update DAC A
0	0	1	1	Data	Load Input Latch DAC B
0	1	0	0	Data	Update DAC B
0	1	0	1	Data	Load Input Latch and Update DAC B
0	1	1	0	X	No Operation
0	1	1	1	X	No Operation
1	0	0	0	X	No Operation
1	0	0	1	X	No Operation
1	0	1	0	X	No Operation
1	0	1	1	X	No Operation
1	1	0	0	Data	Load Input Latch All DACs
1	1	0	1	Data	Update DAC All DACs
1	1	1	0	Data	Load Input Latch and Update All DACs
1	1	1	1	X	No Operation

Table 1. Serial Interface Input Word

DETAILED DESCRIPTION

The ICM7372 is a 12-bit voltage output dual DAC. The ICM7352 is the 10-bit version of this family and the ICM7332 is the 8-bit version. These devices have a 16-bit data-in/data-out shift register and double buffered input. The amplifier's offset adjustment pins allow for a DC shift in the DAC's output.

This family of DACs employs a resistor string architecture guaranteeing monotonic behavior. There is a 1.25V onboard reference and an operating supply range of 2.7V to 5.5V.

Reference Input

Each DAC has its own reference input pin which can be driven from ground to V_{DD} -1.5V. Determine the output voltage using the following equation when output adjustment pin, OSA or OSB is connected to ground 0V.

$$V_{OUT} = 2 \times (V_{REF} \times (D / (2^n)))$$

Where D is the numeric value of DAC's decimal input code, V_{REF} is the reference voltage and n is number of bits, i.e. 12 for ICM7372, 10 for ICM7352 and 8 for ICM7332.

Reference Output

The reference output is nominally 1.25V and is brought out to a separate pin and can be used to drive external loads. The outputs will nominally swing from 0 to 2.5V when using this reference.

Output Amplifier

The Dual DAC has 2 output amplifiers with a wide output voltage swing. The actual swing of the output amplifiers will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The offset adjustment pins, either OSA or OSB can be used to produce an adjustable offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to the offset adjustment pin to produce an output range from 1V to (1V + VREF x 2). Note that the DAC's output range is still limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The output amplifier can drive a load of 2.0 kΩ to V_{DD} or GND in parallel with a 500 pF load capacitance.

The output amplifier has a full-scale typical settling time of 8 µs and it dissipates about 100 µA with a 3V supply voltage.

Serial Interface and Input Logic

This dual DAC family uses a standard 3-wire connection compatible with SPI/QSPI and Microwire interfaces. Data is loaded in 16-bit words which consist of 4 address and control bits (MSBs) followed by 12 bits of data (see table 1). The ICM7352 has the last 2 LSBs as don't care and the ICM7332 has the last 4 LSBs as don't care. The DAC is double buffered with an input latch and a DAC latch.

Serial Data Input

SDI (Serial Data Input) pin is the data input pin for all DACs. Data is clocked in on the rising edge of SCK which has a Schmitt trigger internally to allow for noise immunity on the SCK pin. This specially eases the use for opto-coupled interfaces.

The Chip Select pin which is the 6th pin of 16 QSOP package is active low. This pin must be low when data is being clocked into the part. After the 16th clock pulse the Chip Select pin must be pulled high (level-triggered) for the data to be transferred to an input bank of latches. This pin also disables the SCK pin internally when pulled high and the SCK pin must be low before this pin is pulled back low. As the Chip Select pin is pulled high the shift register contents are transferred to a bank of 16 latches (see Figure 2.). The 4 bit control word (C3~C0) is then decoded and the DAC is updated or loaded depending on the control word (see Table 1).

The DAC has a double-buffered input with an input latch and a DAC latch. The DAC output will swing to its new value when data is loaded into the DAC latch. The user has three options: loading only the input latch, updating the DAC with data previously loaded into the input latch or loading the input latch and updating the DAC at the same time with a new code.

Serial Data Output

SDO (Serial Data Output) is the internal shift register's output. This pin can be used as the data output pin for Daisy-Chaining and data readback. It is compatible with SPI/QSPI and Microwire interfaces.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage output will go to ground.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD}. However, offset and gain error limit this ability. Figure 6 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 7 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

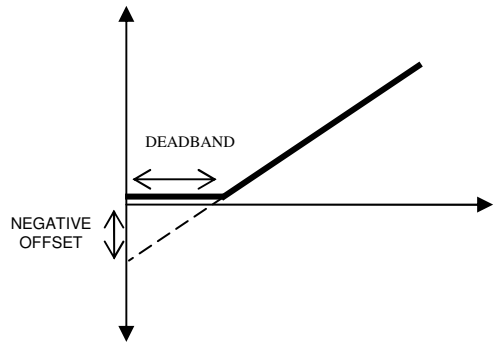


Figure 6. Effect of Negative Offset

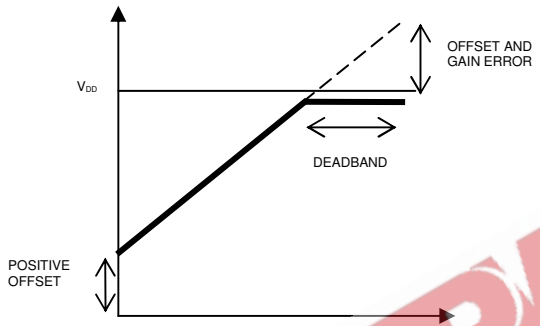
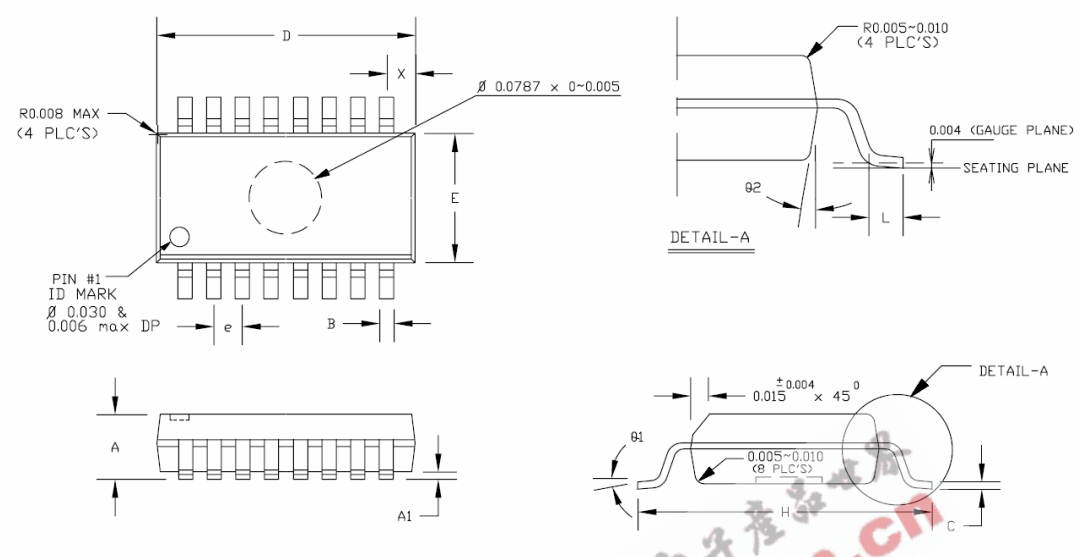


Figure 7. Effect of Gain Error and Positive Offset

PACKAGE INFORMATION



SYMBOL	16 QSOP	
	MIN	MAX
A	0.053	0.068
A1	0.004	0.010
B	0.008	0.012
D	0.189	0.196
E	0.150	0.157
H	0.229	0.244
e	0.025 BSC	
C	0.007	0.009
L	0.016	0.034
X	0.009 REF	
θ1	0^0	8^0
θ2	7^0 BSC	

NOTE:

1. LEAD COPLANARITY SHOULD BE 0 TO 0.004" MAX.
2. PACKAGE SURFACE FINISHING:
   (2.1) TOP: MATTE (CHARMILLES # 24~27)
   (2.2) ALL SIDE: MATTE (CHARMILLES # 24~27)
   (2.3) BOTTOM: MATTE (CHARMILLES # 24~27)
3. ALL DIMENSION EXCLUDING MOLD FLASHES.
4. MAX DEVIATION OF CENTRE OF PACKAGE AND CENTRE OF LEADFRAME TO BE 0.004".
5. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTRE OF PACKAGE TO BE 0.004".
6. THE LEAD WIDTH, B TO BE DETERMINED AT 0.0075" FROM THE LEAD TIP.

ORDERING INFORMATION