Impala Linear Corporation

ILC7281 *Advance*

Micropower Dual 150mA CMOS RF LDO™ Regulators
with Power Supply Reset Monitor

POWER POWERED BY IMPALA ON THE GO

General Description

The ILC7281 provides two independant 150mA low dropout (LDO) voltage regulators and power supply reset monitor in an 8-pin MSOP package. Each regulator output is independantly short circuit protected and has independant shutdown. The device offers a unique combination of low dropout voltage and low quiescent current of CMOS and low noise and high ripple rejection characteristics of bipolar LDO regulators. Moreover, only one input capacitor is required. The power supply reset monitor is available in a ±1% accurate trip voltage to fit most microprocessor applications. Even though its output can sink 2mA, the monitor draws only 1µA in normal operation. Additionally, a built-in hysteresis of 5% of detect voltage simplifies system design.

Dropout Voltage: Typically 150mV at 150mA load, and 1mV at 1mA load.

Ground pin current: Typically 20µA at 1mA load, and 30µA at 150mA load.

Ripple rejection: 75dB at 1kHz and 60dB at 100kHz.

Shutdown mode: Less than 0.5µA quiescent current in shutdown mode.

Small package: 8-pin MSOP.

Small capacitor: Requires only a 0.47µF external cpacitor on the regulator output.

Precision output: Output voltage trimmed to 1% accuracy.

Features

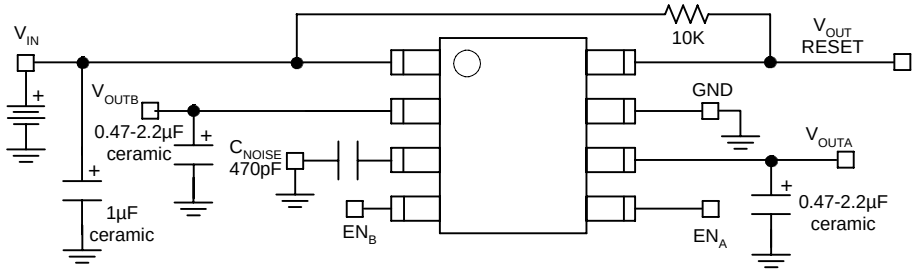
- Guaranteed 150mA output per regulator
- Ultra low 150mV dropout at 150mA
- 1% output voltage accuracy
- Built-in hysteresis of 5% of detection voltage
- Requires only 0.47µF output capacitor
- Only 30µA ground current at 150mA load
- 75dB ripple rejection at 1kHz (C_{OUT} = 0.47µF)
- 80µV_{RMS} noise at BW = 300Hz to 50kHz
- Excellent line and load transient rsponse
- Over current / over temperature protection
- 8-pin MSOP package
- -80dB cross talk

Applications

- Cellular Phones, pagers and wireless headsets
- Microprocessor reset circuits
- Palmtops, oragnizers, PDA's and portable electronics
- Microprocessor reset circuits
- Battery powered portable appliances
- Memory battery back-up circuitry

Ordering Information* (T_A = -40°C to +85°C)	
ILC7281CS-2530	150mA 2.5V and 3.0V LDO regulators with 2.7V detect fail voltage (V_{DF}) Monitor

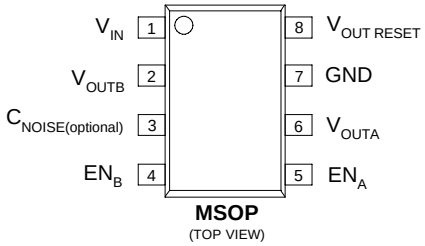
Figure 1



Note: Enable may be connected to V_{IN}, C_{NOISE} connects to both LDO's

Pin-Package Configurations

Figure 2



ILC7281CS-XXXX

Pin Functions ILC7281

Pin Number	Pin Name	Pin Description
1	V_{IN}	Supply Input
2	V_{OUTB}	Regulator Output B
3	$C_{NOISE(optional)}$	Voltage Reference Bypass: Connect external 470pF capacitor to GND to reduce output noise in regulator “A” or “B.” May be left open.
4	EN_B	Enable/Shutdown B (Input): CMOS compatible input. Logic high = enable, logic low or open = shutdown. Do not leave floating.
5	EN_A	Enable/Shutdown A (Input): CMOS compatible input. Logic high = enable, logic low or open = shutdown. Do not leave floating.
6	V_{OUTA}	Regulator Output A
7	GND	Ground
8	$V_{OUT\ RESET}$	Power supply reset monitor output. N-CH open drain output, must connect through a resistor to supply voltage.

Absolute Maximum Ratings for Regulators (Note 1)

Parameter	Symbol	Ratings	Units
Input Voltage	V_{IN}	-0.3 to +12	V
S/D Input Voltage	$V_{S/D}$	-0.3 to V_{IN}	
Output Current	I_{OUT}	Short circuit protected	mA
Output Voltage	V_{OUT}	-0.3 to 10	V
Power Dissipation	P_d	Internally Limited	mW
Maximum Junction Temp Range	$T_{J(max)}$	-40~+125	°C
Storage Temperature	T_{stg}	-40~+125	°C
ESD Rating		2	kV
Operating Input Voltage	V_{IN}	2.1 to 10	V
Operating Ambient Temperature	T_A	-40 to +85	°C
Package Thermal Resistance	θ_{JA}	200	°C/W

Electrical Characteristics ILC7281CS

Unless otherwise specified, all limits are at T_A = 25°C; V_{IN} = $V_{O(NOM)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 0.47µF, $V_{S/D}$ = 2V.
Boldface limits apply over the operating temperature range. **(Note 2)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT}	I_{OUT} = 1mA	-1	V_{OUT} (Nom.)	+1	%V (Nom.)
Output Voltage	V_{OUT}	1mA < I_{OUT} < 100mA 1mA < I_{OUT} < 100mA	-1.5 **-2.5**	V_{OUT} (Nom.)	+1.5 **+2.5**	%V (Nom.)
Output Voltage	V_{OUT}	1mA < I_{OUT} < 150mA 1mA < I_{OUT} < 150mA	-2.5 **-3.5**	V_{OUT} (Nom.)	2.5 **+3.5**	%V (Nom.)
Line Regulation	$\Delta V_O/\Delta V_{IN}$	$V_{O(NOM)}$ + 1V ≤ V_{IN} ≤ 10V		0.007	0.014 **0.032**	%/V
Dropout Voltage **(Note 3)**	V_{IN} - V_{OUT}	I_{OUT} = 0mA		0.1	1 **2**	mV
Dropout Voltage **(Note 3)**	V_{IN} - V_{OUT}	I_{OUT} = 10mA		10	15 **20**	mV
Dropout Voltage **(Note 3)**	V_{IN} - V_{OUT}	I_{OUT} =150mA		150	175 **200**	mV
Ground Pin Current	I_{GND}	I_{OUT} = 0mA		20	60 **80**	µA
Ground Pin Current	I_{GND}	I_{OUT} = 10mA		25	70 **90**	µA
Ground Pin Current	I_{GND}	I_{OUT} = 150mA		30	80 **120**	µA
Shutdown Current	$I_{S/D}$			0.1	**1**	µA

Electrical Characteristics ILC7281CS

Unless otherwise specified, all limits are at T_A = 25°C; V_{IN} = $V_{O(NOM)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 0.47µF, $V_{S/D}$ = 2V.
Boldface limits apply over the operating temperature range. **(Note 2)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Shutdown Input Voltage	$V_{S/D}$	High = Regulator On Low = Regulator Off	**2.0**		**10** **0.6**	V
Peak Output Current **(Note 4)**	$I_{O(peak)}$	$V_{OUT} \geq 0.95V_{O(NOM)}$	300	500		mA
Output Noise Voltage (RMS)	e_N	BW = 300Hz to 50kHz, C_{NOISE} = 0pF		80		μV_{RMS}
Ripple Rejection	$\Delta V_O/\Delta V_{IN}$	freq = 1kHz freq = 10kHz		75 70		dB
Dynamic Line Regulation	$\Delta V_{O(line)}$	freq = 100kHz V_{IN}: $V_{O(NOM)}$ + 1V to $V_{O(NOM)}$ + 2V; $dV_{IN/dt}$ = 1V/$_{\mu S;Io}$ = 150mA		60 10		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	I_{OUT}: 0 to 150mA; $d(I_{OUT})/dt$ = 50A/µs, with C_{OUT} = 2.2µF		40 20		mV
Short Circuit Current	I_{SC}	V_{OUT} = 0V		300		mA
Cross Talk				-60		dB

Note1: Absolute maximum ratings indicate limits which when exceeded may result in damage to the component. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: Specified Min/Max limits are production tested or guaranteed through correlation based on statistical control methods. Measurements are taken at constant junction temperature as close to ambient as possible using low duty pulse testing.

Note 3: Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the nominal value measured with a 1V differential.

Note 4: Guaranteed by design

Absolute Maximum Ratings Supply Reset Monitor (T_A = 25°C)

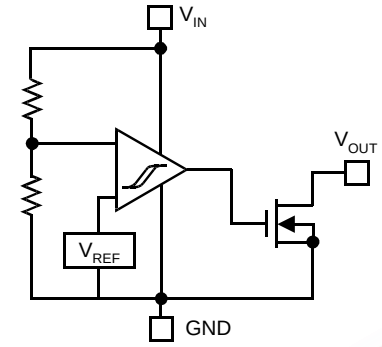
Parameter	Symbol	Ratings	Units
Input Voltage	V_{IN}	12	V
Output Current	I_{OUT}	50	mA
Output Voltage	V_{OUT}	V_{SS}-0.3~V_{IN}+0.3	V
Continuous Total Power Dissipation (SOT-23)	P_d	150	mW
Operating Ambient Temperature	T_{opr}	-30~+80	°C
Storage Temperature	T_{stg}	-40~+125	°C

Electrical Characteristics Power Supply Reset Monitor (T_A = 25°C)

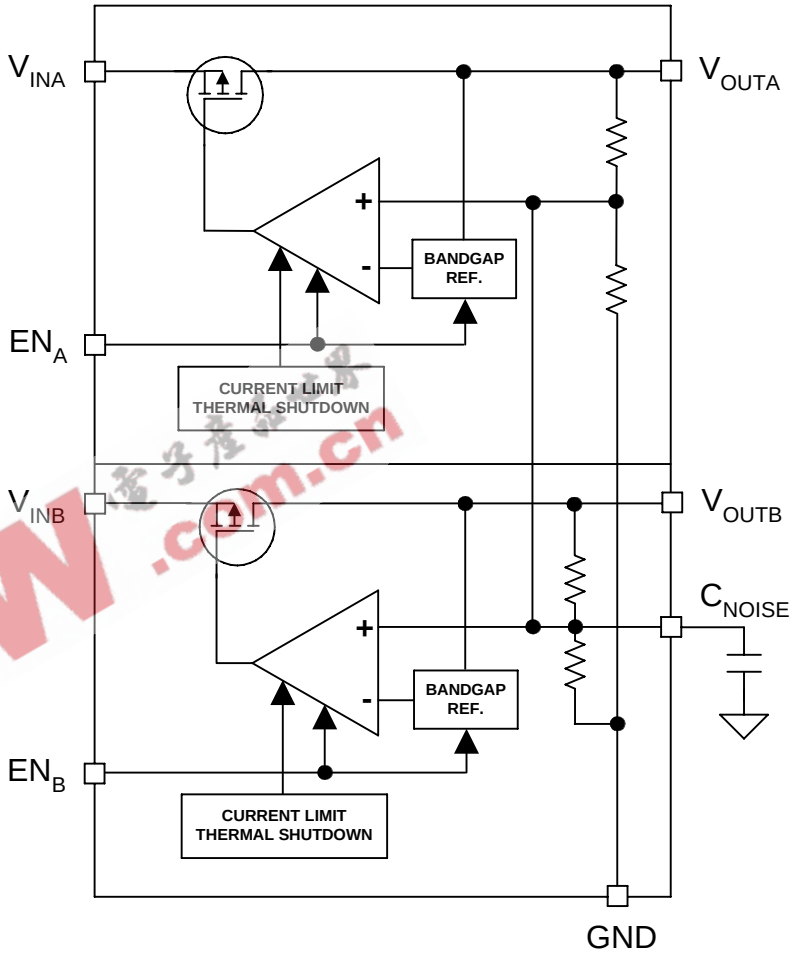
Paramter	Symbol	Conditions	Min	Typ	Max	Units
Detect Fail Voltage	V_{DF}	A grade	V_{DF} X 0.99	V_{DF}	V_{DF} X 1.01	V
Hysteresis Range	V_{HYS}		V_{DF} X 0.02	V_{DF} X 0.05	V_{DF} X 0.08	V
Supply Current	I_{SS}	V_{IN} = 1.5V V_{IN} = 2.0V V_{IN} = 3.0V V_{IN} = 4.0V V_{IN} = 5.0V	1.5	0.9 1.0 1.3 1.6 2.0	2.6 3.0 3.4 3.8 4.2	µA
Operating Voltage	V_{IN}	V_{DF} = 2.1~6.0V			10.0	V
Output Current	I_{OUT}	N-ch V_{DS} = 0.5V V_{IN} = 1.0V V_{IN} = 2.0V V_{IN} = 3.0V V_{IN} = 4.0V V_{IN} = 5.0V		 2.2 7.7 10.1 11.5 13.0		mA
Temperature Characteristics	$\Delta V_{DF}/(\Delta T_{opr} \bullet V_{DF})$	-30°C ≤ T_{opr} ≤ 80°C		±100		ppm/°C
Delay Time (Release Voltage Output Inversion)	t_{DLY} (V_{DR} V_{OUT} Inversion)				0.2	ms

Note:

1. An additional resistor between the V_{IN} pin and supply voltage may cause deterioration of the characteristics due to increasing of V_{DR}.



N - Channel Open Drain Output



APPLICATIONS INFORMATION - Regulators

Enable/Shutdown

Forcing $EN_{A/B}$ (enable/shutdown) high (>2V) enables the regulator. $EN_{A/B}$ is compatible with CMOS logic gates. If the enable/shutdown feature is not required, connect $EN_{A/B}$ to $V_{INA/B}$ (supply input).

Input Capacitor

A 1µF capacitor should be placed from $V_{INA/B}$ to GND if there is more than 10 inches of wire between the input and the ac filter capacitor or if a battery is used as the input.

Reference Bypass Capacitor

C_{NOISE} (reference bypass) is connected to the internal voltage reference of regulator A and B. A 470pF capacitor connected from C_{NOISE} to GND decouples the reference, providing a significant reduction in output noise. C_{NOISE} reduces the regulator phase margin; when using C_{NOISE}, output capacitors of 2.2µF or greater are generally required to maintain stability. The start-up speed of the ILC7281 is inversely proportional to the size of the reference bypass capacitor. Applications requiring a slow ramp-up of output voltage should consider larger values of C_{NOISE}. Likewise, if rapid turn-on is necessary, consider omitting C_{NOISE}. If output noise is not a major concern, omit C_{NOISE} and leave the pin open.

Output Capacitor

An output capacitor is required between $V_{OUTA/B}$ and GND to prevent oscillation. The minimum size of the output capacitor is dependent upon whether a reference bypass capacitor is used. 1.0µF minimum is recommended when C_{NOISE} is not used (see figure 2). 2.2µF minimum is recommended when C_{NOISE} is 470pF (see figure 1). Larger values slow the regulator's transient response. The output capacitor value may be increased without limit. The output capacitor should have an ESR (effective series resistance) of about 5 or less and a resonant frequency above 1MHz. Ultra low ESR capacitors may be used and will not cause a low-amplitude oscillation and/or underdamped transient response which shows up in some LDO regulators. Most ceramic capacitors are adequate so there is no need for more expensive tantalum capacitors.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.47µF for current below 10mA or 0.33µF for currents below 1mA

No-Load Stability

The ILC7281 will remain stable and in regulation with no load unlike many other voltage regulators. This is expecially important in CMOS RAM KeepAlive applications.

Dual-Supply Operation

When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

Thermal Considerations

Multilayer boards having a ground plane, wide traces near the pads, and large supply bus lines provide better thermal conductivity. The 8-lead MSOP has a thermal resistance of 200°C/W when mounted on an FR4 board with minimum trace widths and no ground plane.

Thermal Evaluation Examples

For example, at 50°C ambient temperature, the maximum package power dissipation is:

P D(max) = (125°C - 50°C)/200°C/W
P D(max) = 375mW

If the intent is to operate the part from a 4V supply at the full 150mA load for both outputs in a 50°C maximum ambient temperature, make the following calculations:

P D(each regulator) = $(V_{IN} - V_{OUT}) * I_{OUT} + (V_{IN} * I_{GND})$
P D(each regulator) = (4V - 3V) * 150mA + (4V * 0.12mA)
P D(each regulator) = 150mW
P D(both regulators) = 2 regulators * 150mW
P D(both regulators) = 300mW

The actual total power dissipation of 300mW is below the 375mW package maximum; therefore the regulator can be used. Note that both regulators cannot always be used at their maximum current rating. For example, in a 5V input to 3.0V output application at 50°C, if one regulator supplies 150mA, the other regulator is limited to a much lower current. The first regulator dissipates:

P D = (5V - 3.0V) 150 + 0.12mA (5V)
P D = 267.5mW

Then, the load that the remaining regulator can dissipate must not exceed: 375mW - 267.5mW = 107.5mW. This means, using the same 5V input and 3.3V output voltage, the second regulator is limited to about 60mA

Taking advantage of the extremely low dropout voltage characteristics of the ILC7281, power dissipation can be reduced by using the lowest possible input voltage to minimize the input to output voltage drop.

Functional Descriptin - Power Supply Reset Monitor

The following designators 1~6 refer to the timing diagram below.

1. While the input voltage (V_{IN}) is higher than the detect fail voltage (V_{DF}); the V_{OUT} output pin is at high impedence state.

2. When the input V_{IN} voltage falls lower than V_{DF}, V_{OUT} drops near to ground voltage.

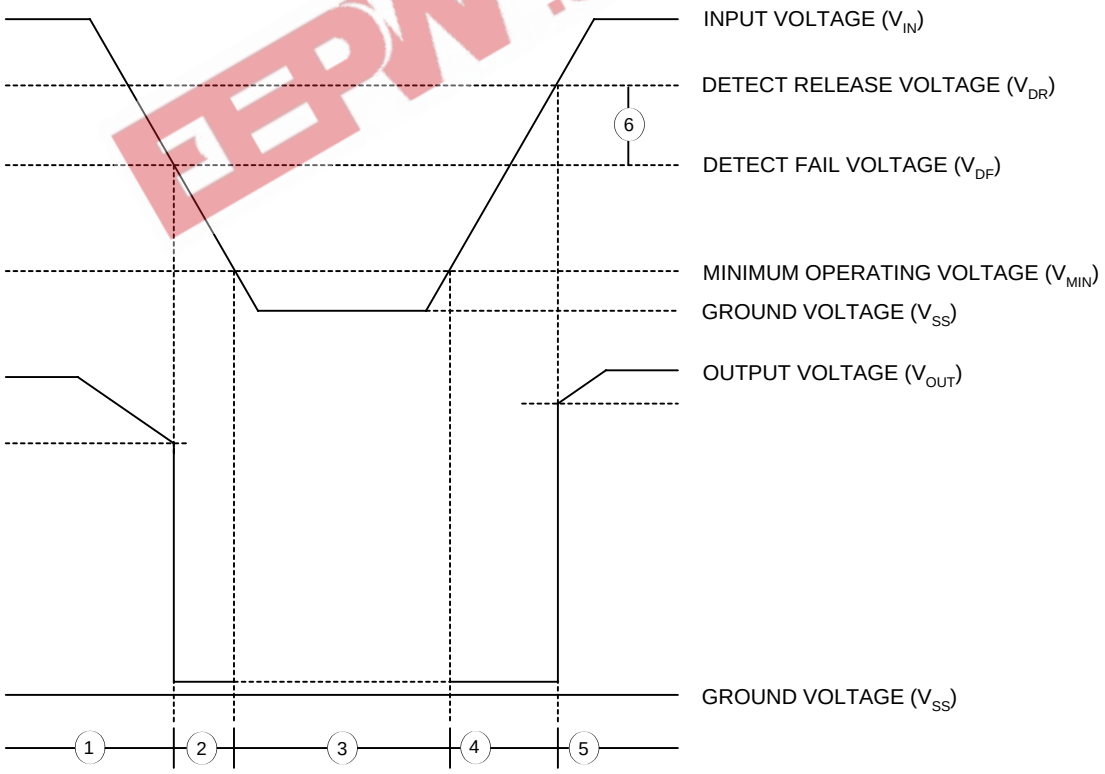
3. If the input voltage decreases below the minimum operating voltage (V_{MIN}), the V_{OUT} output becomes unstable. In this condition, if the V_{OUT} pin is pulled up, V_{OUT} indicates the V_{IN} voltage.

4. During an increase of the input voltage from V_{SS} voltage, V_{OUT} is not stable in the voltage below the V_{MIN}. Exceeding that level, the output stays at the ground level (V_{SS}) between the minimum operating voltage (V_{MIN}) and detect release voltage (V_{DR}).

5. If the input voltage increases more than V_{DR}, the V_{OUT} output pin is at high impedence state.

6. The difference between V_{DR} and V_{DF} is the hysteresis in the system.

Timing Diagram



Package Dimensions

MSOP-8