Impala Linear Corporation

ILC705/706/707/708

mP Supervisory Circuit

POWER POWERED BY IMPALA ON THE GO

General Description

The ILC705/ILC706/ILC707/ILC708 are low cost microprocessor supervisory circuits that monitor power supplies in microprocessor based systems. Circuit functions include a watchdog timer, microprocessor reset, power failure warning and a debounced manual reset input.

The ILC705 and ILC706 offer a watchdog timer function while the ILC707 and ILC708 have an active high reset output in addition to the active low reset output.

Supply voltage monitor levels of 4.65V and 4.4V are available. The ILC705/ILC707 have a nominal reset threshold level of 4.65V while the ILC706 and ILC708 have a 4.4V nominal reset threshold level. When the supply voltage drops below the respective reset threshold level, RESET is asserted.

Features

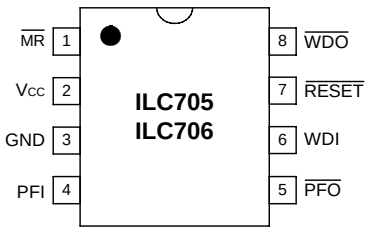
- 4.4V or 4.65V Precision Voltage Monitor
- 200ms Reset Pulse Width
- Debounced TTL/CMOS Compatible Manual Reset Input
- Watchdog Timer with 1.6 sec Timeout (ILC705/ILC706)
- Voltage Monitor for Early Power Fail Warning or Low Battery Detect
- 8-Pin SOIC or DIP Package

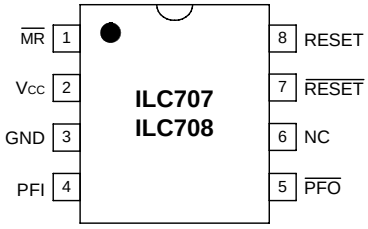
Applications

- Computers
- Controllers
- Critical Microprocessor Power Monitoring
- Intelligent Instruments
- Portable Equipment
- Controllers

Pin Package Configuration

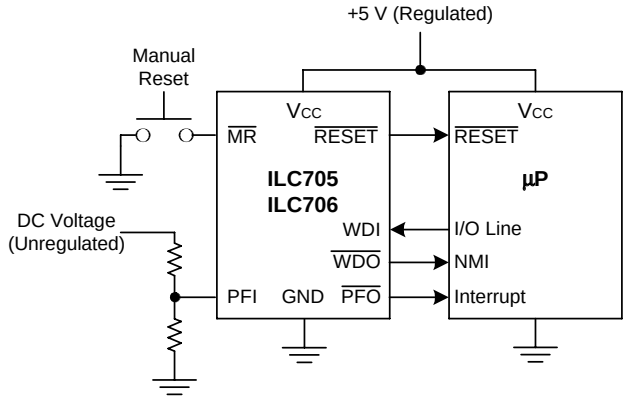
Top View





N Package - 8 Lead Plastic DIP Package
M Package - 8 Lead Plastic SOIC Package

Typical Circuit



Ordering Information

Part	Package	Temp. Range
ILC70_N	8-Lead PDIP	-40°C to +85°C
ILC70_M	8-Lead SOIC	-40°C to +85°C

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Terminal Voltage	V_{CC}	-0.3 to 6.0	V
	All other inputs	-0.3 to (V_{CC} + 0.3)	V
Input Current	V_{CC}, GND	25	mA
Output Current	All outputs	20	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Power Dissipation	PDIP	475	mW
	SOIC	400	mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

Electrical Characterisitcs

V_{CC} = 4.75 V to 5.5 V for ILC705/ILC707, V_{CC} = 4.5 V to 5.5 V for ILC706/ILC708, T_A = Operating Temperature Range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage Range, V_{CC}	ILC70__	1.4		5.5	V
Supply Current, I_{CC}	ILC70__			60	µA
Reset Voltage Threshold	ILC705, ILC707 ILC706, ILC708	4.5 4.25	4.65 4.4	4.75 4.5	V
Reset Threshold Hysteresis			40		mV
Reset Pulse Width, t_{RS}		140	200	280	ms
$\overline{RESET}$ Output Voltage	I_{SOURCE} = 800 µA I_{SINK} = 3.2 mA I_{SINK} = 50 µA, V_{CC} = 1.4V	V_{CC} – 1.5V		 0.4 0.3	V
RESET Output Voltage	I_{SOURCE} = 800 µA I_{SINK} = 1.2 mA	V_{CC} – 1.5V		 0.4	V
Watchdog Timeout Period, t_{WD}		1.0	1.6	2.25	sec
WDI Minimum Input Pulse, t_{WP}	V_{IL} = 0.4V, V_{IH} = 80% of V_{CC}	50			ns
WDI Threshold Voltage	V_{IH}, V_{CC} = 5V V_{IL}, V_{CC} = 5V	3.5		 0.8	V
WDI Input Current	WDI = 0V WDI = V_{CC}	-150	-50 50	 150	µA
WDO Output Voltage	I_{SOURCE} 800 µA I_{SINK} = 1.2 mA	V_{CC} – 1.5V		 0.4	V
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V	100	250	600	µA
$\overline{MR}$ Pulse Width, t_{MR}		150			ns
$\overline{MR}$ Input Threshold	V_{IL} V_{IH}	 2.0		0.8	V
$\overline{MR}$ to Reset Output Delay, t_{MD}				250	ns
PFI Input Threshold	V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current		-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA V_{CC} = 5V, I_{SOURCE} = 800 µA	 V_{CC} - 1.5V		0.4	V

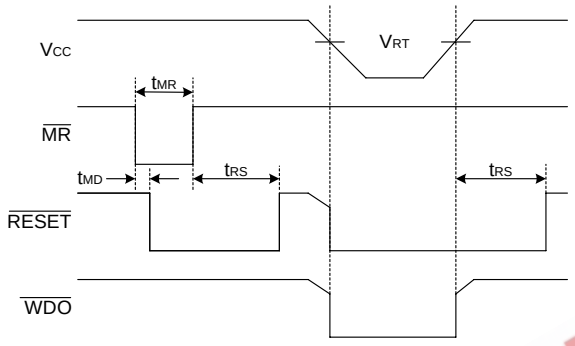
Pin Functions

Pin Name	Pin Number		Description
	ILC705 ILC706	ILC707 ILC708	
$\overline{MR}$	1	1	Manual reset input. $\overline{MR}$ forces $\overline{RESET}$ to assert when pulled below 0.8V. An internal pull-up current of 250 mA on this input forces it high when left floating. This input can also be driven from TTL or CMOS logic.
Vcc	2	2	Power supply input, 5V.
GND	3	3	Ground pin, 0 V reference.
PFI	4	4	Power fail input. Internally connected to the power fail comparator, which is referenced to 1.25V. The power fail output ($\overline{PFO}$) remains high if PFI is above 1.25V. PFI should be connected to GND or V_{OUT} if the power fail comparator is not used.
$\overline{PFO}$	5	5	Power fail output. The power fail comparator is independent of all other functions on this device.
WDI	6	N/A	Watchdog input. The WDI input monitors microprocessor activity, an internal watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, WDO is forced to active low. The watchdog function can be disabled by floating the WDI pin.
N/C	N/A	6	No Connect.
RESET	7	7	$\overline{RESET}$ output. $\overline{RESET}$ is asserted if either V_{CC} goes below the reset threshold or by a low signal on the manual reset input ($\overline{MR}$). $\overline{RESET}$ remains asserted for one reset timeout period (200ms) after V_{CC} exceeds the reset threshold or after the manual reset pin transitions from low to high. The watchdog timer will not assert $\overline{RESET}$ unless WDO is connected to $\overline{MR}$.
$\overline{WDO}$	8	N/A	Watchdog timer output. The watchdog timer resets itself with each transition on the watchdog input. If the WDI pin is held high or low for longer than the watchdog timeout period, $\overline{WDO}$ is forced low. $\overline{WDO}$ will also be forced low if V_{CC} is below the reset threshold and will remain low until V_{CC} returns to a valid level.
RESET	N/A	8	RESET output. RESET is the compliment of $\overline{RESET}$ and is asserted if either V_{CC} goes below the reset threshold or by a low signal on the manual reset input ($\overline{MR}$). RESET is suitable for microprocessors systems that use an active high reset.

Circuit Description

Microprocessor Reset

The RESET pin is asserted whenever V_{CC} falls below the reset threshold voltage or when MR goes low. The reset pin remains asserted for a period of 200ms after V_{CC} has risen above the reset threshold voltage and MR goes high. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. RESET will remain valid with V_{CC} as low as 1.4V



Watchdog Timer

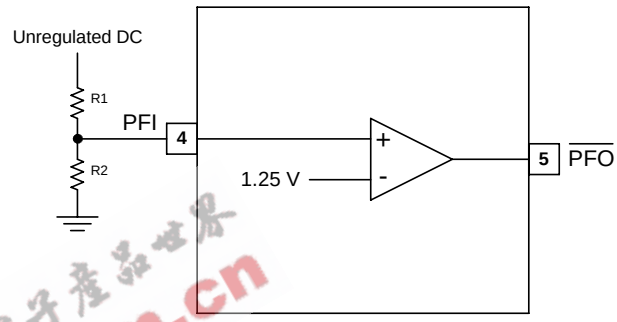
The microprocessor can be monitored by connecting the WDI pin (watchdog input) to a bus line or I/O line. If a transition does not occur on the WDI pin within the watchdog timeout period, then WDO will go low. A minimum pulse of 50ns or any transition low-to-high or high-to-low on the WDI pin will reset the watchdog timer. The output of the watchdog timer (WDO) will remain high if WDI sees a valid transition within the watchdog timeout period or if WDI is left floating. If V_{CC} falls below the reset threshold voltage then WDO goes low immediately regardless of WDI. If WDI is left floating, then WDO can be used as a low line indicator.

Manual Reset

The manual-reset input (MR) allows reset to be triggered by a pushbutton switch which is debounced by the 140ms minimum reset pulse width. MR can be driven by external TTL/CMOS compatible logic. By connecting WDO to MR a watchdog timeout will generate a reset pulse in the ILC705/ILC706.

Power Fail Warning

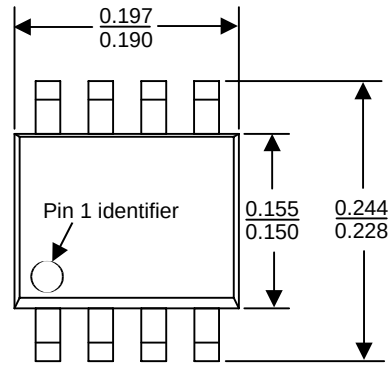
An additional comparator which is independent of other functions on the ILC705/706/707/708 is provided for early warning of power failure. An external voltage divider can be used to compare unregulated DC to an internal 1.25V reference. The voltage divider ratio on the input of the power fail comparator (PFI) can be chosen so as to trip the power fail comparator a few milliseconds before V_{CC} falls below the maximum reset threshold voltage. The output of the power fail comparator (PFO) can be used to interrupt the microprocessor when used in this mode and execute shutdown procedures prior to power loss



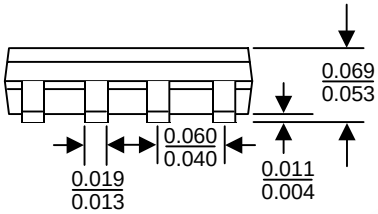
Alternate Reference Guide

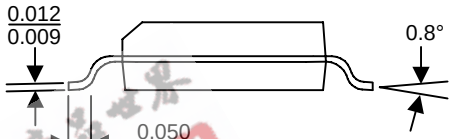
Industry P/N	ILC Direct Replacement
MAX705CPA	ILC705N
MAX705CSA	ILC705M
MAX705EPA	ILC705N
MAX705ESA	ILC705M
ADM705AN	ILC705N
DS1705	ILC705
MAX706CPA	ILC706N
MAX706CSA	ILC706M
MAX706EPA	ILC706N
MAX706C/D	ILC706D
ADM706AN	ILC706N
DS1706	ILC706
MAX707CPA	ILC707N
MAX707CSA	ILC707M
MAX707EPA	ILC707N
MAX707ESA	ILC707M
MAX707C/D	ILC707D
ADM707AN	ILC707N
DS1707	ILC707
MAX708CPA	ILC708N
MAX708CSA	ILC708M
MAX708EPA	ILC708N
MAX708ESA	ILC708M
MAX708C/D	ILC708D
ADM708AN	ILC708N
DS1708	ILC708

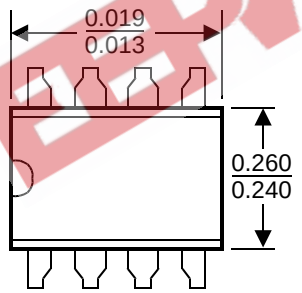
Packaging Information



M Package, 8-Pin Small Outline







N Package, 8-Pin Plastic Dual In-line