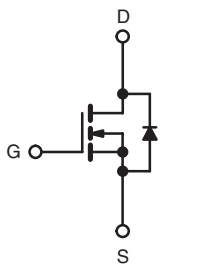


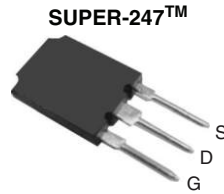


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	600	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.175
Q _g (Max.) (nC)	220	
Q _{gs} (nC)	67	
Q _{gd} (nC)	96	
Configuration	Single	



N-Channel MOSFET



FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhances dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offer Improved Noise Immunity
- Lead (Pb)-free Available



RoHS* COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	SUPER-247™
Lead (Pb)-free	IRFPS29N60LPbF SiHFPS29N60L-E3
SnPb	IRFPS29N60L SiHFPS29N60L

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	600	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	29	A
		T _C = 100 °C		18	
Pulsed Drain Current ^a			I _{DM}	110	
Linear Derating Factor				3.8	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	570	mJ
Repetitive Avalanche Current ^a			I _{AR}	29	A
Repetitive Avalanche Energy ^a			E _{AR}	48	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	480	W
Peak Diode Recovery dV/dt ^c			dV/dt	15	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 1.5 mH, R_G = 25 Ω, I_{AS} = 29 A (see fig.12a).
- I_{SD} ≤ 29 A, dI/dt ≤ 830 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

IRFPS29N60L, SiHFPS29N60L




Vishay Siliconix

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^a	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain) ^a	R_{thJC}	-	0.26	

Note

a. R_{th} is measured at T_J approximately 90 °C.

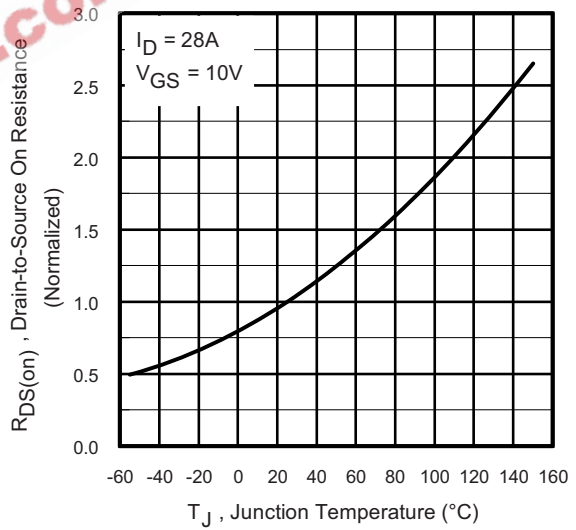
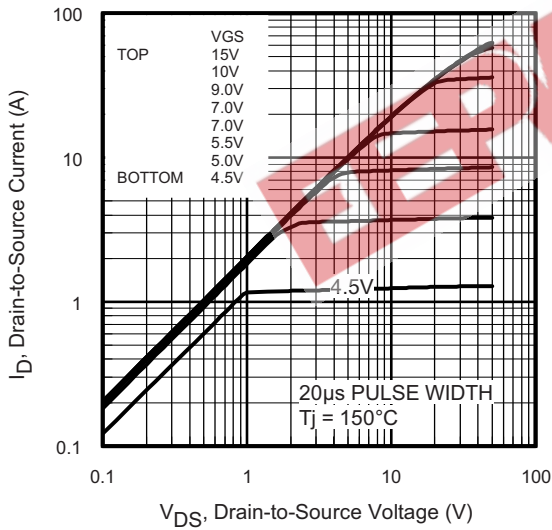
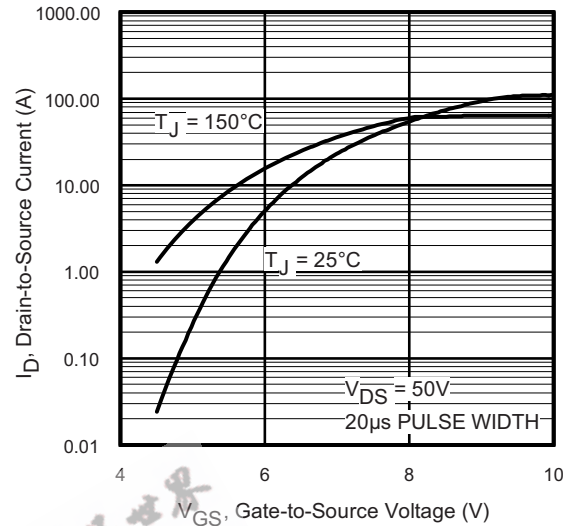
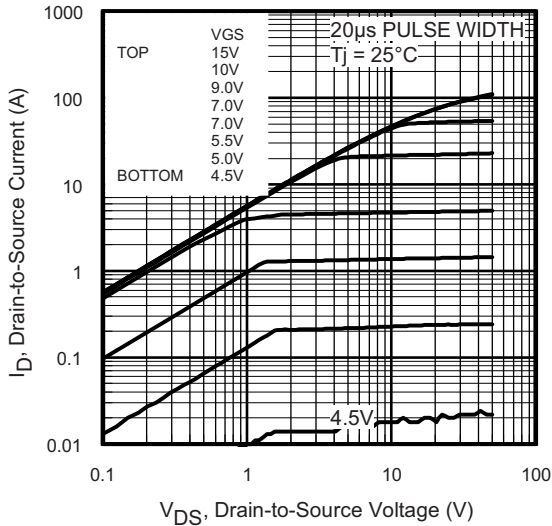
SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$	-	0.53	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$	-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}^b$	-	0.175	0.21	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 17\text{ A}^b$	15	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}^b$	-	6160	-	pF
Output Capacitance	C_{oss}		-	530	-	
Reverse Transfer Capacitance	C_{rss}		-	44	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		-	250	-	
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$		$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	190	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}, V_{DS} = 480\text{ V}, \text{ see fig. 7 and 15}^b$	-	-	220	nC
Gate-Source Charge	Q_{gs}		-	-	67	
Gate-Drain Charge	Q_{gd}		-	-	96	
Internal Gate Resistance	R_G	$f = 1\text{ MHz}, \text{ open drain}$	-	0.86	-	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 29\text{ A}, R_G = 4.3\text{ }\Omega, V_{GS} = 10\text{ V}, \text{ see fig. 11a and 11b}^b$	-	34	-	ns
Rise Time	t_r		-	100	-	
Turn-Off Delay Time	$t_{d(off)}$		-	66	-	
Fall Time	t_f		-	54	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	29	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	110	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 29\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}, I_F = 29\text{ A}, T_J = 125\text{ °C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	130	190	ns
			-	240	360	
Body Diode Reverse Recovery Charge	Q_{rr}		-	630	950	μC
			-	1820	2720	
Body Diode Recovery Current	I_{RRM}	$T_J = 25\text{ °C}$	-	9.4	14	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} . $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



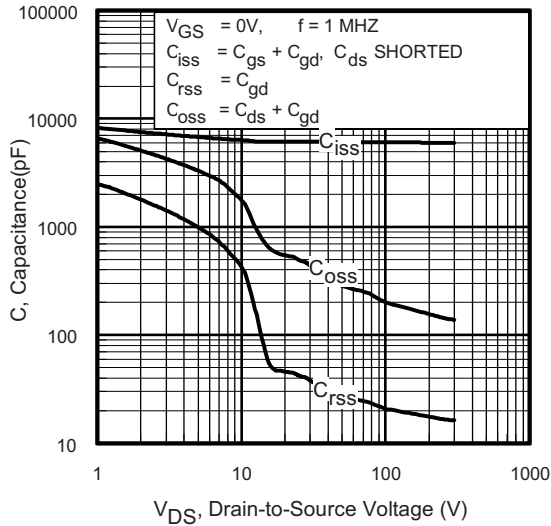


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

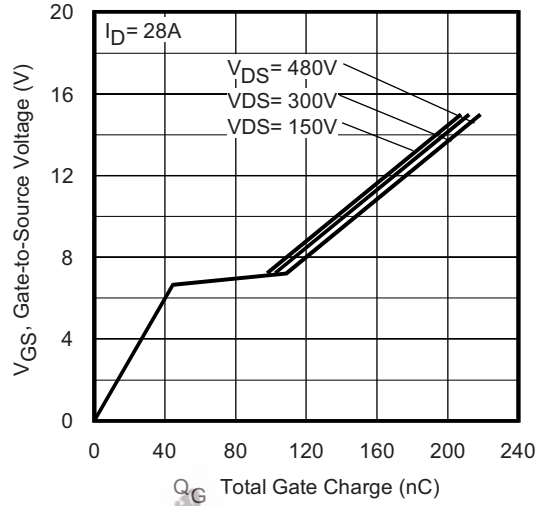


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

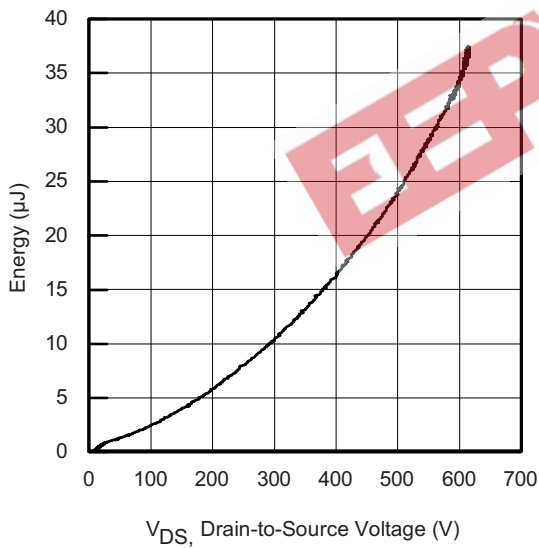


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

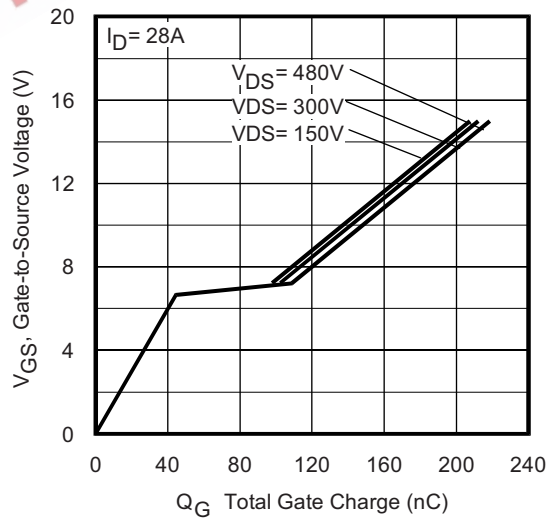


Fig. 8 - Typical Source-Drain Diode Forward Voltage

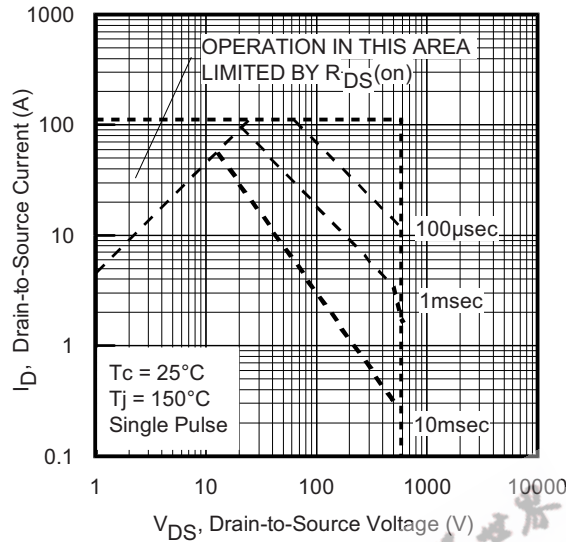


Fig. 9 - Maximum Safe Operating Area

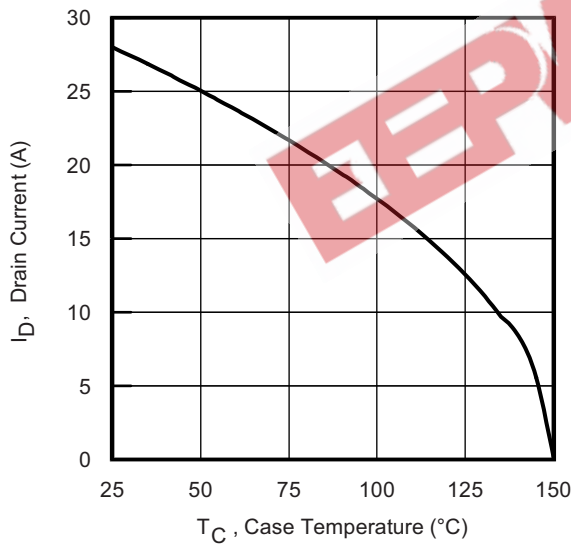


Fig. 10 - Maximum Drain Current vs. Case Temperature

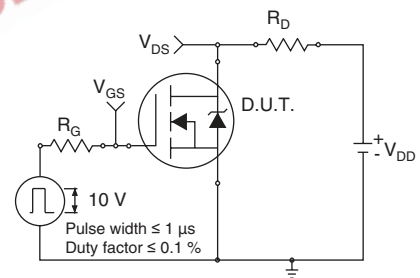


Fig. 11a - Switching Time Test Circuit

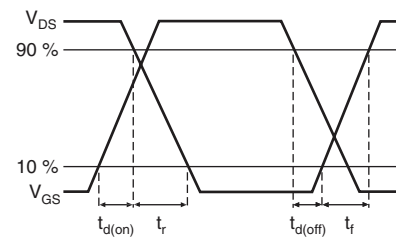


Fig. 11b - Switching Time Waveforms

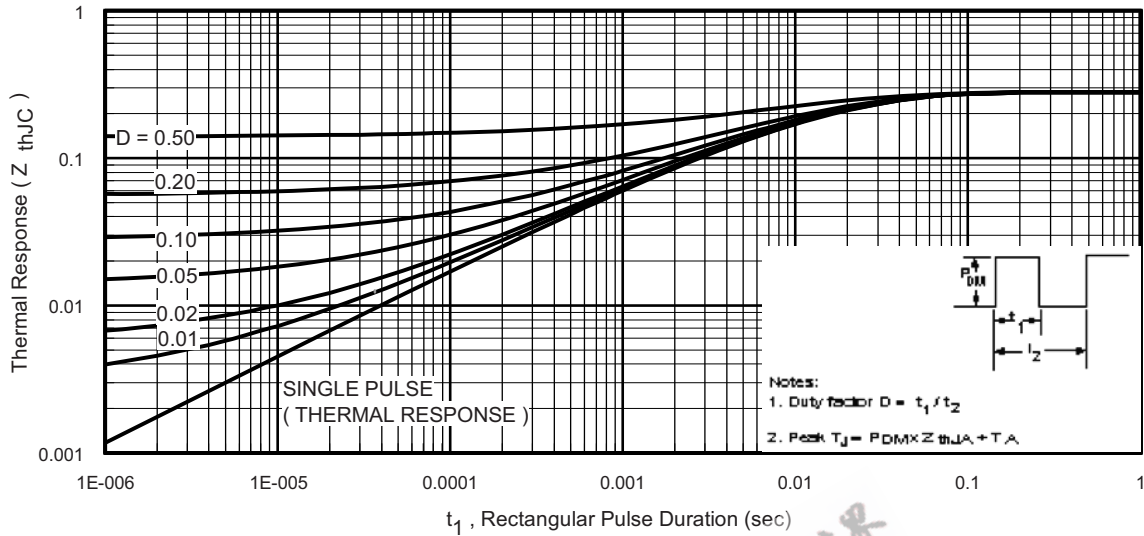


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

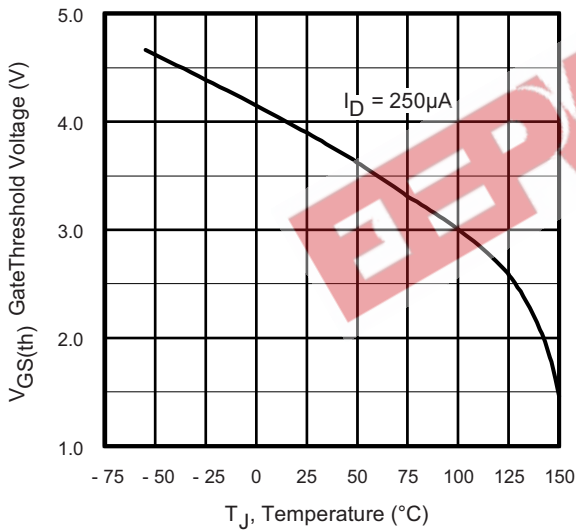


Fig. 13 - Threshold Voltage vs. Temperature

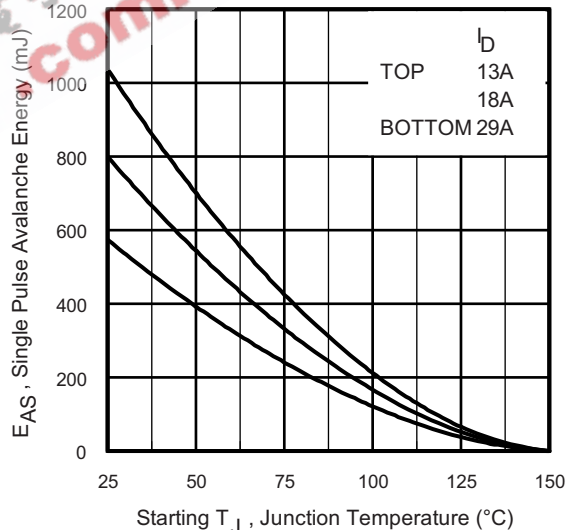


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

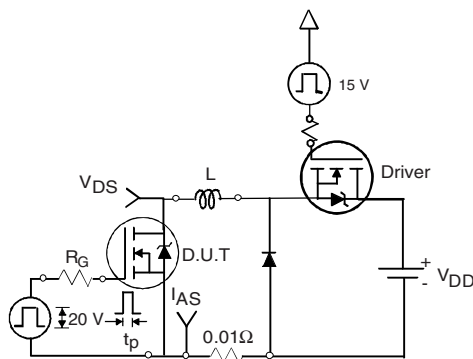


Fig. 14b - Unclamped Inductive Test Circuit

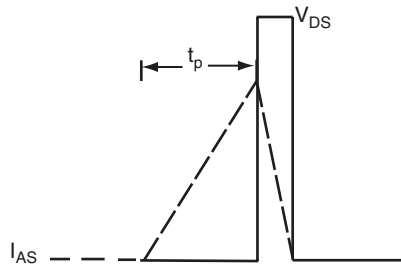


Fig. 14c - Unclamped Inductive Waveforms

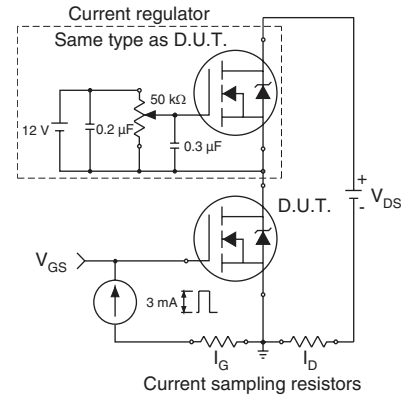


Fig. 15a - Gate Charge Test Circuit

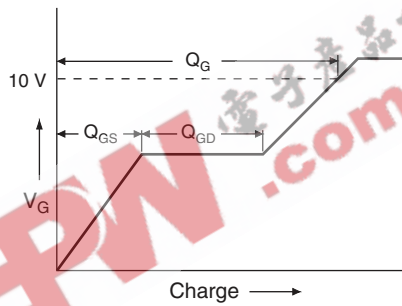
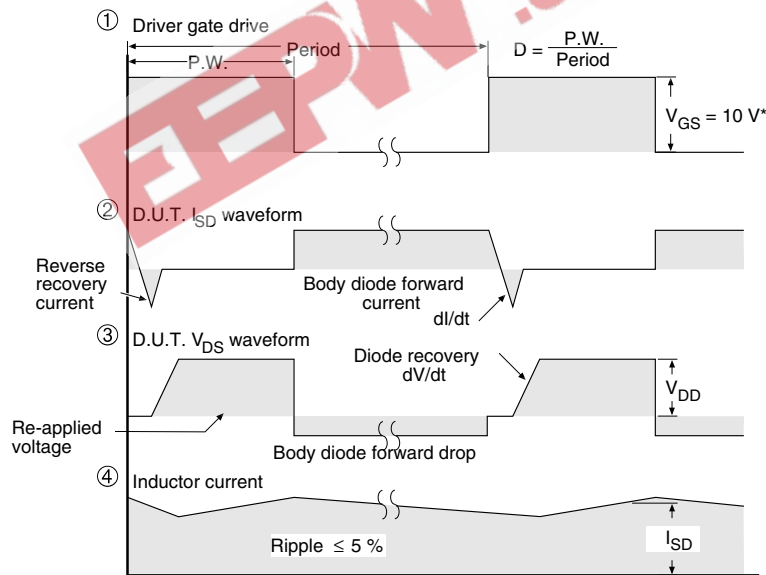
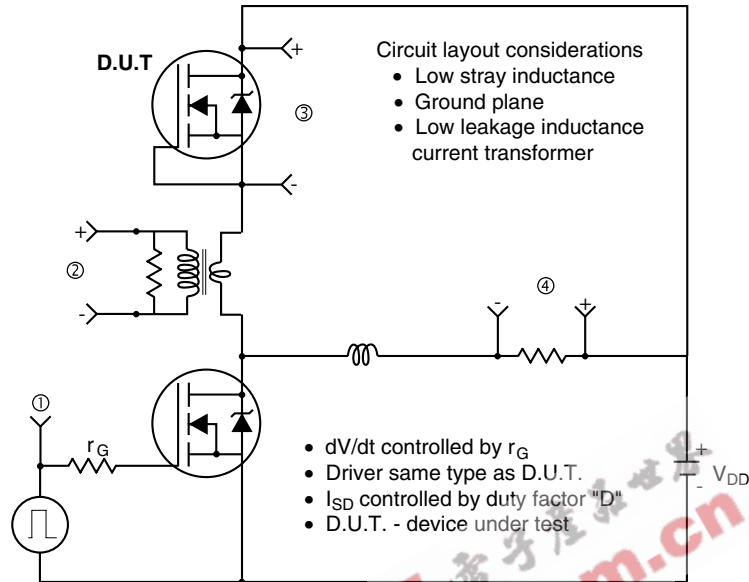


Fig. 15b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for logic level devices

Fig. 16 - For N-Channel

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