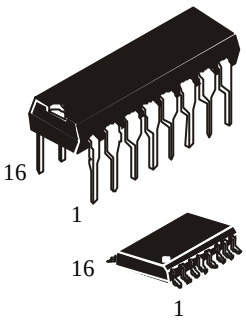
IW4040B

12-Stage Binary Ripple Counter
High-Voltage Silicon-Gate CMOS

The IW4040B is ripple-carry binary counter. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC DIP

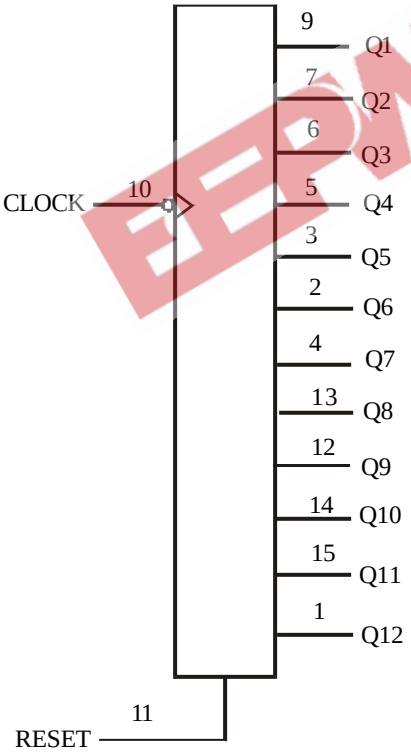
D SUFFIX
SOIC

ORDERING INFORMATION

IW4040BN	Plastic DIP
IW4040BD	SOIC
IZ4040B	chip

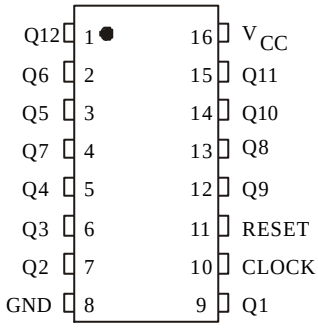
T_A = -55° to 125° C
for all packages

LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Clock	**Reset**	**Output state**
⌐	L	No change
¬	L	Advance to next state
X	H	All Outputs are low

H= high level
L = low level
X=don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500*[1]	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*[1] For T_A=-55 to 100°C (package plastic DIP), for T_A=-55 to 65°C (package SOIC)
+Derating - Plastic DIP: - 12 mW/°C from 100°Ñ to 125°C
SOIC Package: : - 7 mW/°C from 65°Ñ to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit -55°C	Guaranteed Limit 25°C	Guaranteed Limit 125° C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	3.5 7.0 11.0	3.5 7.0 11.0	3.5 7.0 11.0	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V V_{OUT}=1.0 V or V_{CC} - 1.0 V V_{OUT}=1.5 V or V_{CC} - 1.5 V	5.0 10 15	1.5 3.0 4.0	1.5 3.0 4.0	1.5 3.0 4.0	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}= GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	µA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, R_L=200 kΩ, t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit -55°C	25°C	125°C	Unit
f_{max}	Maximum Clock Frequency (Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	1.75 4.0 6.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q1 (Figure 1)	5.0 10 15	360 160 130	360 160 130	720 320 260	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Q_n to Q_{n+1} (Figure 2)	5.0 10 15	330 80 60	330 80 60	660 160 120	ns
t_{PHL}	Maximum Propagation Delay, Reset to Any Q (Figure 3)	5.0 10 15	280 120 100	280 120 100	560 240 200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS (C_L=50 pF, R_L=200 kΩ, t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit -55°C	25°C	125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	140 60 40	140 60 40	280 120 80	ns
t_w	Minimum Pulse Width, Reset (Figure 3)	5.0 10 15	200 80 60	200 80 60	400 160 120	ns
t_{rem}	Minimum Removal Time, Reset(Figure 3)	5.0 10 15	350 150 100	350 150 100	700 300 200	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0 10 15	Unlimited			ns

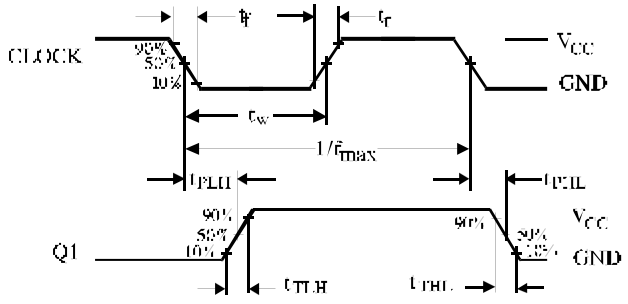


Figure 1. Switching Waveforms

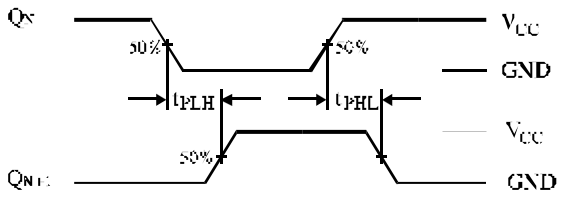


Figure 2. Switching Waveforms

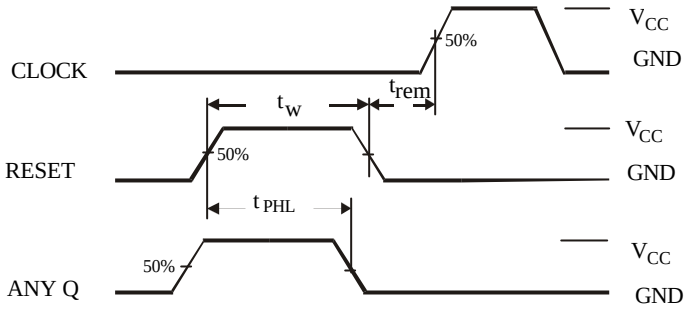
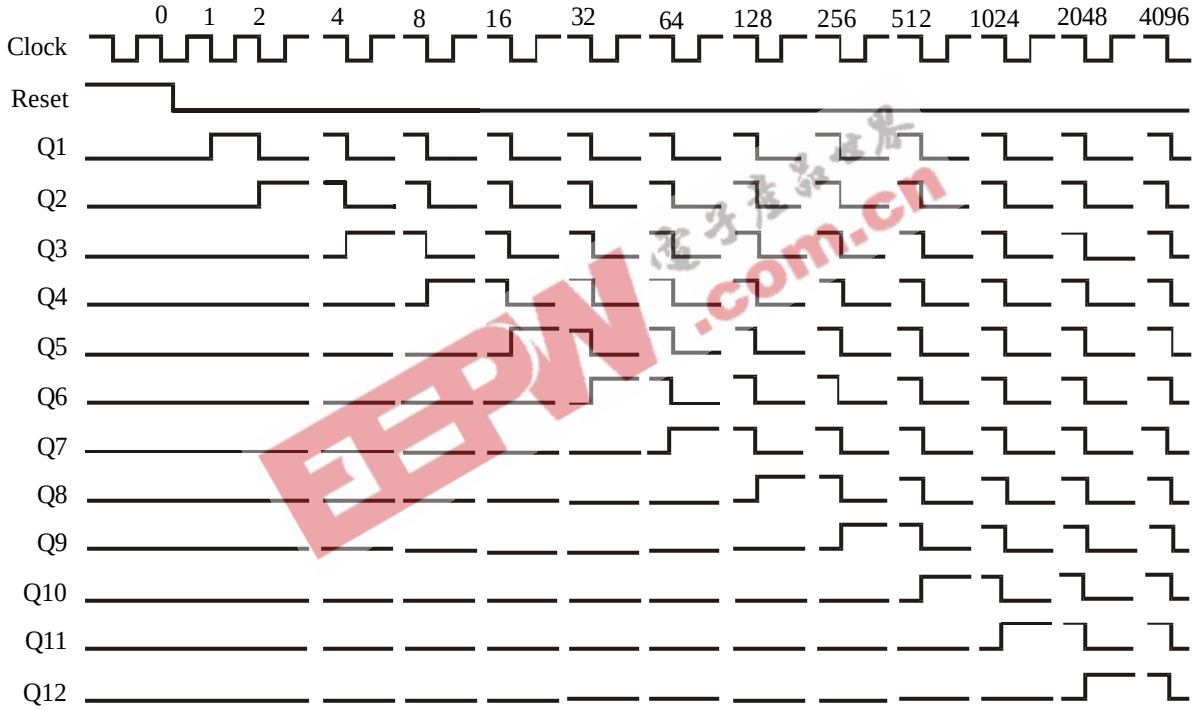
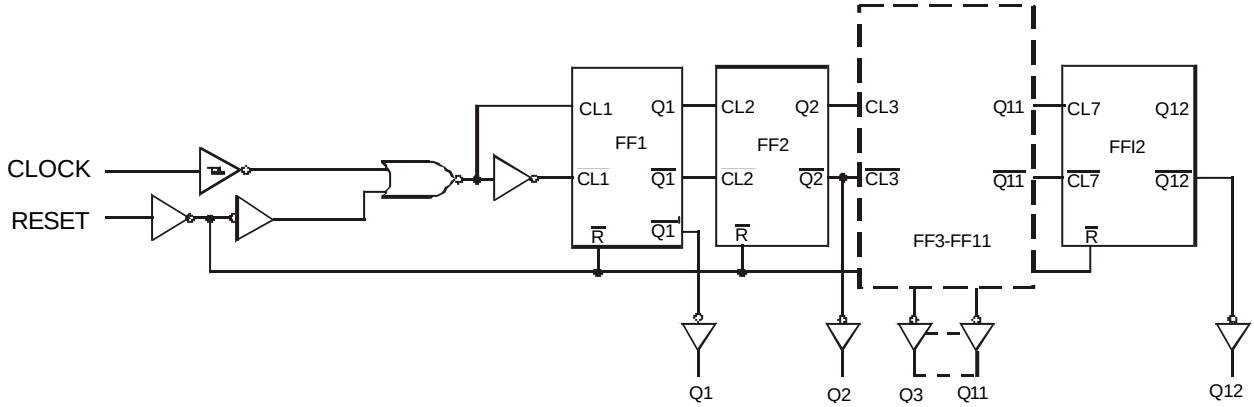


Figure 3. Switching Waveforms

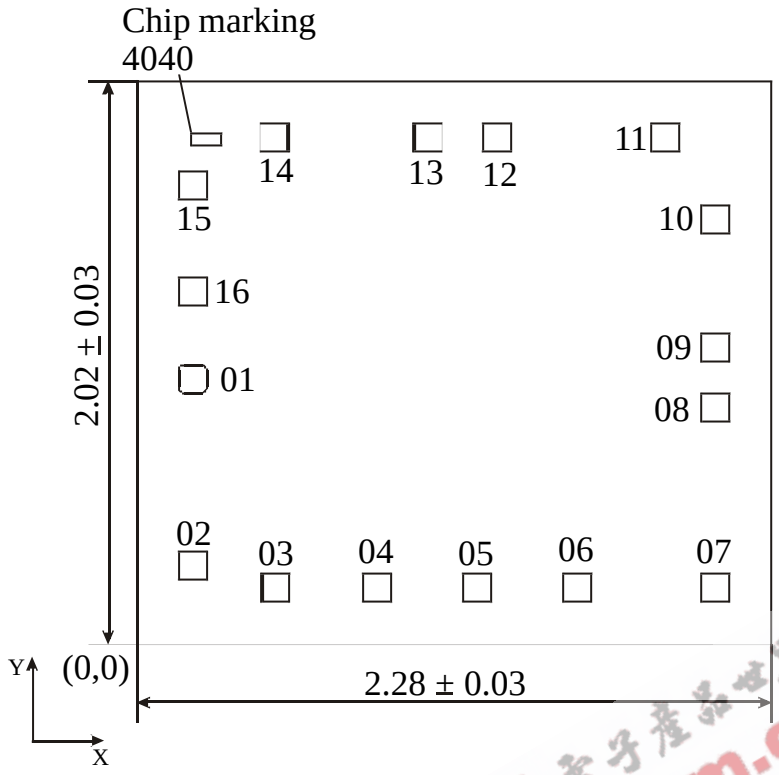
TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=0.199, y=1.792.

Chip thickness: 0.46 ± 0.02 (0.35 ± 0.02) mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Q12	0.1525	0.9025	0.100 x 0.100
02	Q6	0.1525	0.2315	0.100 x 0.100
03	Q5	0.4515	0.1525	0.100 x 0.100
04	Q7	0.8115	0.1525	0.100 x 0.100
05	Q4	1.1715	0.1525	0.100 x 0.100
06	Q3	1.5315	0.1525	0.100 x 0.100
07	Q2	2.0270	0.3365	0.100 x 0.100
08	GND	2.0270	0.7995	0.100 x 0.100
09	Q1	2.0270	1.0135	0.100 x 0.100
10	INPUT	2.0270	1.4760	0.100 x 0.100
11	RES	1.8470	1.7675	0.100 x 0.100
12	Q9	1.2430	1.7675	0.100 x 0.100
13	Q8	0.9965	1.7675	0.100 x 0.100
14	Q10	0.4445	1.7675	0.100 x 0.100
15	Q11	0.1525	1.5980	0.100 x 0.100
16	V_{CC}	0.1525	1.2140	0.100 x 0.100

Note: Pad location is given as per passivation layer