

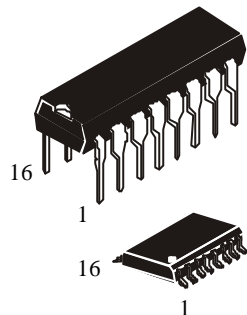
IW4040B

12-Stage Binary Ripple Counter

High-Voltage Silicon-Gate CMOS

The IW4040B is ripple-carry binary counter. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC DIP

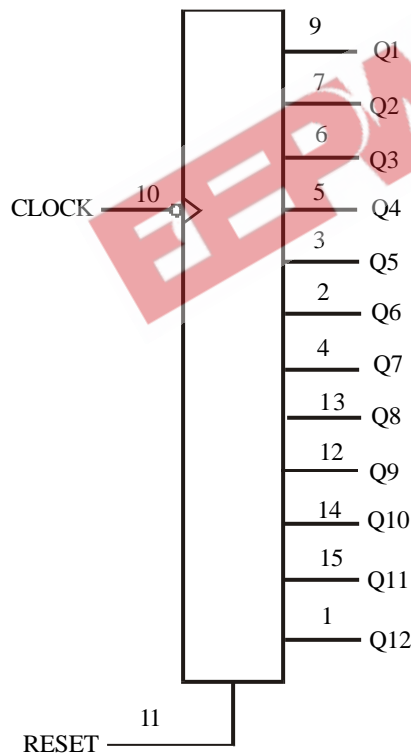
D SUFFIX
SOIC

ORDERING INFORMATION

IW4040BN Plastic DIP
IW4040BD SOIC
IZ4040B chip

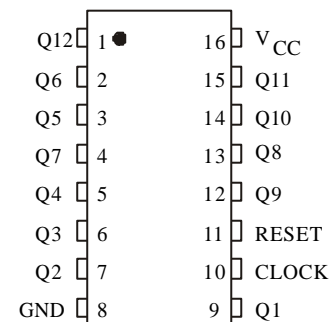
$T_A = -55^\circ$ to 125° C
for all packages

LOGIC DIAGRAM





PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
Clock	Reset	Output state
	L	No change
	L	Advance to next state
X	H	All Outputs are low

H= high level
L = low level
X=don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	500* ¹	mW
P _{Tot}	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

*¹ For T_A=-55 to 100°C (package plastic DIP), for T_A=-55 to 65°C (package SOIC)

+Derating - Plastic DIP: - 12 mW/°C from 100°C to 125°C
SOIC Package: - 7 mW/°C from 65°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55°C	25°C	125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V V _{OUT} =1.0 V or V _{CC} - 1.0 V V _{OUT} =1.5 V or V _{CC} - 1.5 V	5.0	3.5	3.5	3.5	V
			10	7.0	7.0	7.0	
			15	11.0	11.0	11.0	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V V _{OUT} =1.0 V or V _{CC} - 1.0 V V _{OUT} =1.5 V or V _{CC} - 1.5 V	5.0	1.5	1.5	1.5	V
			10	3.0	3.0	3.0	
			15	4.0	4.0	4.0	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	5	5	150	µA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{ pF}$, $R_L=200\text{ k}\Omega$, $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C	25°C	125°C	
f _{max}	Maximum Clock Frequency (Figure 1)	5.0	3.5	3.5	1.75	MHz
		10	8	8	4.0	
		15	12	12	6.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1 (Figure 1)	5.0	360	360	720	ns
		10	160	160	320	
		15	130	130	260	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Q _n to Q _{n+1} (Figure 2)	5.0	330	330	660	ns
		10	80	80	160	
		15	60	60	120	
t _{PHL}	Maximum Propagation Delay, Reset to Any Q (Figure 3)	5.0	280	280	560	ns
		10	120	120	240	
		15	100	100	200	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C _{IN}	Maximum Input Capacitance	-	-	7.5	-	pF

TIMING REQUIREMENTS ($C_L=50\text{ pF}$, $R_L=200\text{ k}\Omega$, $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C	25°C	125°C	
t _w	Minimum Pulse Width, Clock (Figure 1)	5.0	140	140	280	ns
		10	60	60	120	
		15	40	40	80	
t _w	Minimum Pulse Width, Reset (Figure 3)	5.0	200	200	400	ns
		10	80	80	160	
		15	60	60	120	
t _{rem}	Minimum Removal Time, Reset(Figure 3)	5.0	350	350	700	ns
		10	150	150	300	
		15	100	100	200	
t _r , t _f	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0	Unlimited			ns
		10				
		15				

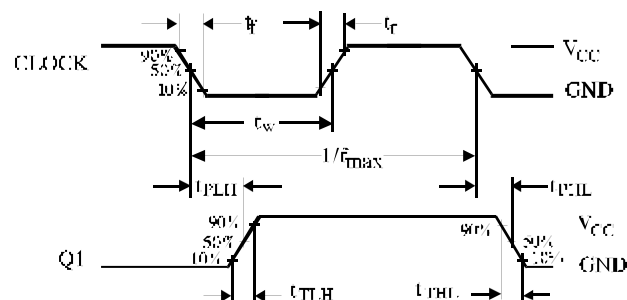


Figure 1. Switching Waveforms

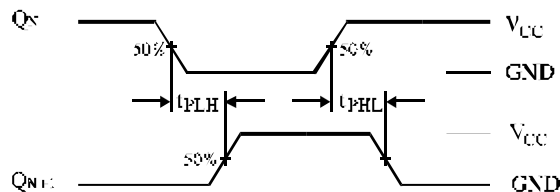


Figure 2. Switching Waveforms

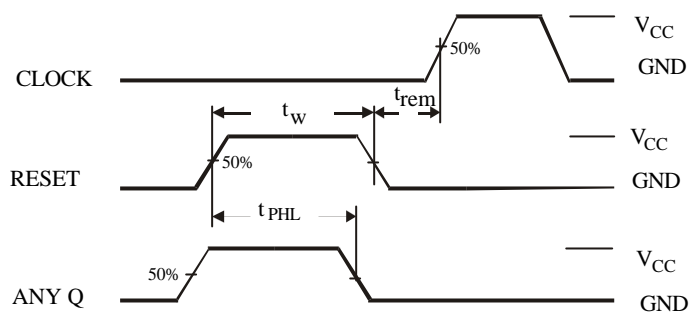
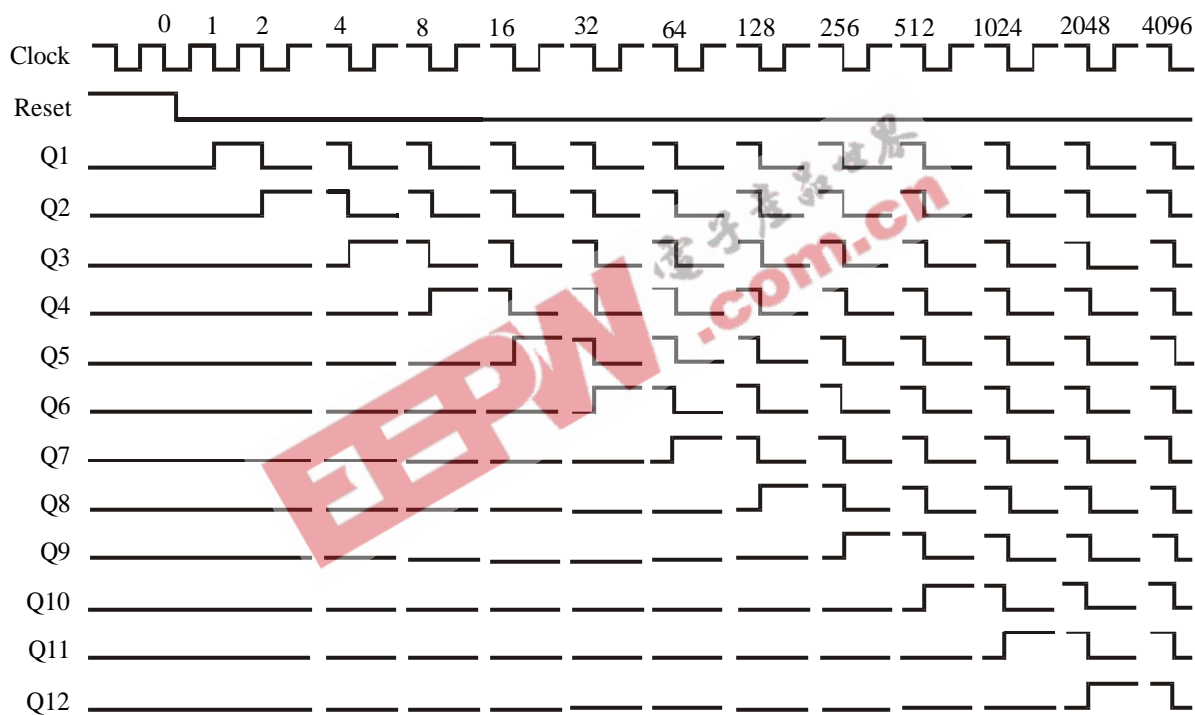
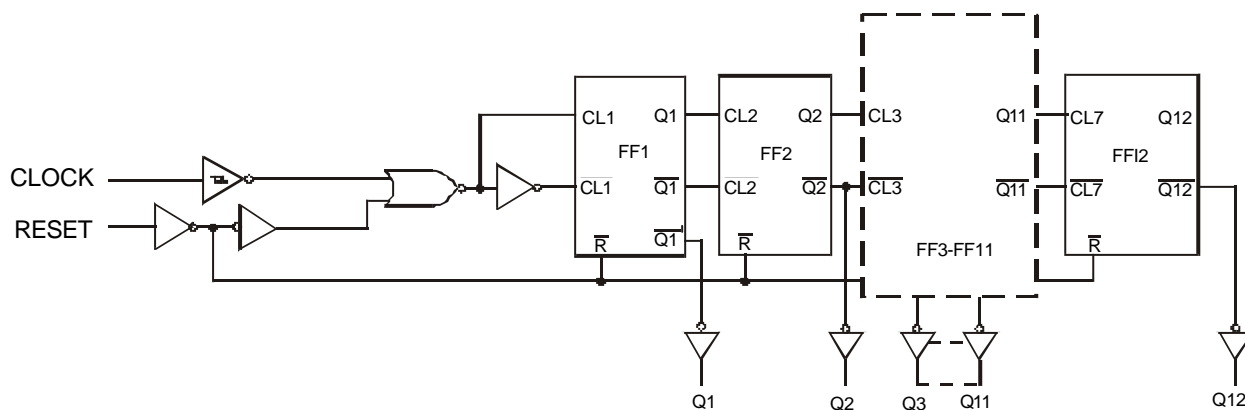


Figure 3. Switching Waveforms

TIMING DIAGRAM

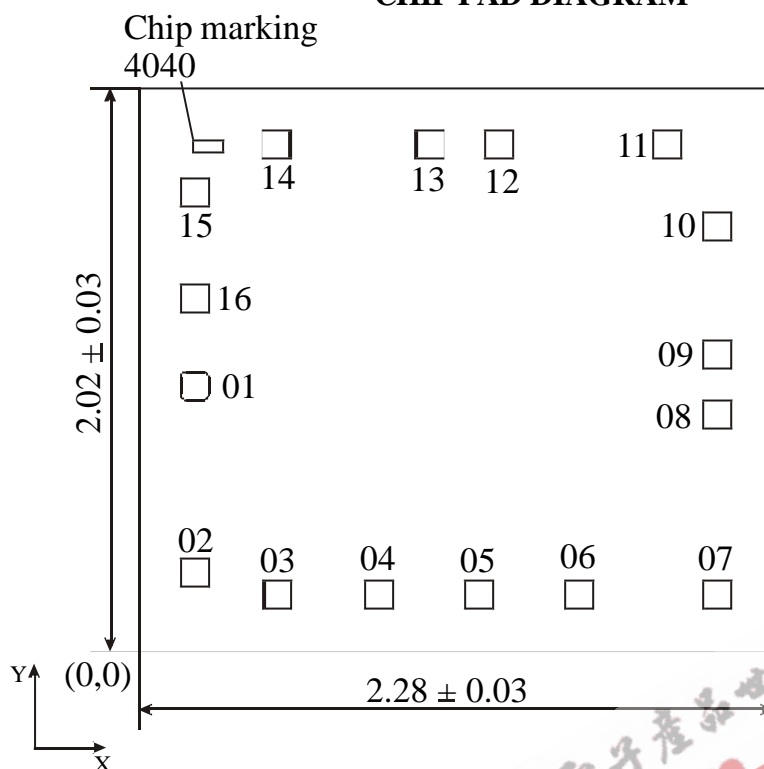


EXPANDED LOGIC DIAGRAM



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CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=0.199$, $y=1.792$.

Chip thickness: 0.46 ± 0.02 (0.35 ± 0.02) mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Q12	0.1525	0.9025	0.100 x 0.100
02	Q6	0.1525	0.2315	0.100 x 0.100
03	Q5	0.4515	0.1525	0.100 x 0.100
04	Q7	0.8115	0.1525	0.100 x 0.100
05	Q4	1.1715	0.1525	0.100 x 0.100
06	Q3	1.5315	0.1525	0.100 x 0.100
07	Q2	2.0270	0.3365	0.100 x 0.100
08	GND	2.0270	0.7995	0.100 x 0.100
09	Q1	2.0270	1.0135	0.100 x 0.100
10	INPUT	2.0270	1.4760	0.100 x 0.100
11	RES	1.8470	1.7675	0.100 x 0.100
12	Q9	1.2430	1.7675	0.100 x 0.100
13	Q8	0.9965	1.7675	0.100 x 0.100
14	Q10	0.4445	1.7675	0.100 x 0.100
15	Q11	0.1525	1.5980	0.100 x 0.100
16	V _{CC}	0.1525	1.2140	0.100 x 0.100

Note: Pad location is given as per passivation layer