IRLM220A

FEATURES

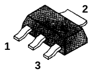
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 200V
- Lower $R_{DS(ON)}$: 0.609 Ω (Typ.)

BV_{DSS} = 200 V

$R_{DS(on)}$ = 0.8 Ω

I_D = 1.13 A

SOT-223



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic		Value	Units
V_{DSS}	Drain-to-Source Voltage		200	V
I_D	Continuous Drain Current (T_A=25°C)		1.13	A
	Continuous Drain Current (T_A=70°C)		0.9	
I_{DM}	Drain Current-Pulsed	(1)	9	A
V_{GS}	Gate-to-Source Voltage		±20	V
E_{AS}	Single Pulsed Avalanche Energy	(2)	29	mJ
I_{AR}	Avalanche Current	(1)	1.13	A
E_{AR}	Repetitive Avalanche Energy	(1)	0.2	mJ
dv/dt	Peak Diode Recovery dv/dt	(3)	5	V/ns
P_D	Total Power Dissipation (T_A=25°C) *		2	W
	Linear Derating Factor *		0.016	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range		- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds		300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics (T_C=25˚C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	200	--	--	V	V_{GS}=0V,I_D=250µA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.18	2.0	V/˚C	I_D=250µA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	1.0	--	100	V	V_{DS}=5V,I_D=250µA
I_{GSS}	Gate-Source Leakage , Forward	--	--	-100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	10		V_{GS}=--20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	100	µA	V_{DS}=200V
		--	--			V_{DS}=160V,T_C=125˚C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.8	Ω	V_{GS}=5V,I_D=0.57A (4)
g_{fs}	Forward Transconductance	--	2.8	--	S	V_{DS}=40V,I_D=0.57A (4)
C_{iss}	Input Capacitance	--	330	430	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	55	70		
C_{rss}	Reverse Transfer Capacitance	--	8	30		
$t_{d(on)}$	Turn-On Delay Time	--	6	25	ns	V_{DD}=100V,I_D=5A, R_G=9Ω ***See Fig 13*** (4)(5)
t_r	Rise Time	--	24	20		
$t_{d(off)}$	Turn-Off Delay Time	--	6	60		
t_f	Fall Time	--	6	20		
Q_g	Total Gate Charge	--	10.3	15	nC	V_{DS}=160V,V_{GS}=5V, I_D=5A ***See Fig 6 & Fig 12*** (4)(5)
Q_{gs}	Gate-Source Charge	--	2.0	--		
Q_{gd}	Gate-Drain ("Miller") Charge	--	4.4	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	1.13	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current (1)	--	--	9		
V_{SD}	Diode Forward Voltage (4)	--	--	1.5	V	T_J=25˚C,I_S=1.13A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	140	--	ns	T_J=25˚C,I_F=5A di_F/dt=100A/µs (4)
Q_{rr}	Reverse Recovery Charge	--	0.59	--	µC	

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
② L=35mH, I_{AS}=1.13A, V_{DD}=50V, R_G=27Ω, Starting T_J=25˚C
③ $I_{SD} \leq$ 5A, di/dt ≤ 180A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J=25˚C
④ Pulse Test : Pulse Width = 250µs, Duty Cycle ≤ 2%
⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

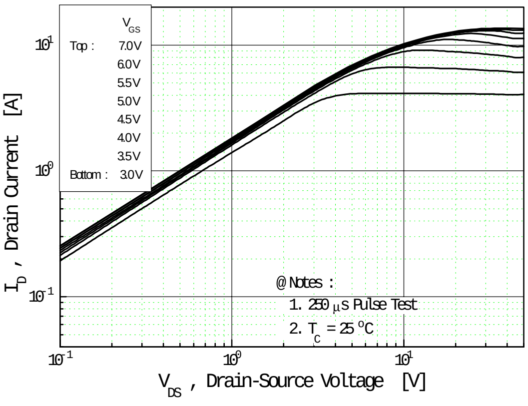


Fig 2. Transfer Characteristics

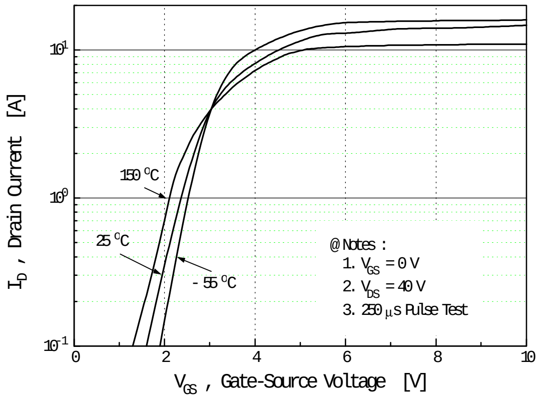


Fig 3. On-Resistance vs. Drain Current

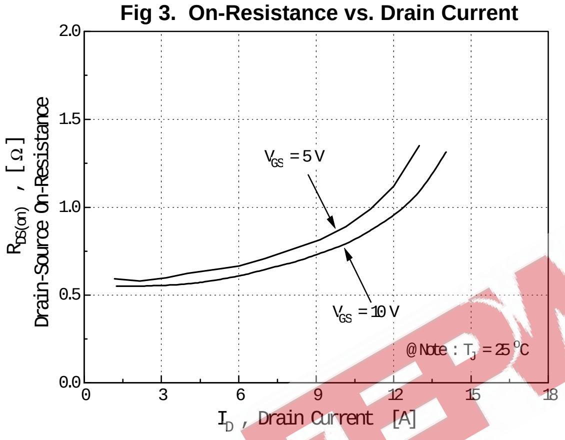


Fig 4. Source-Drain Diode Forward Voltage

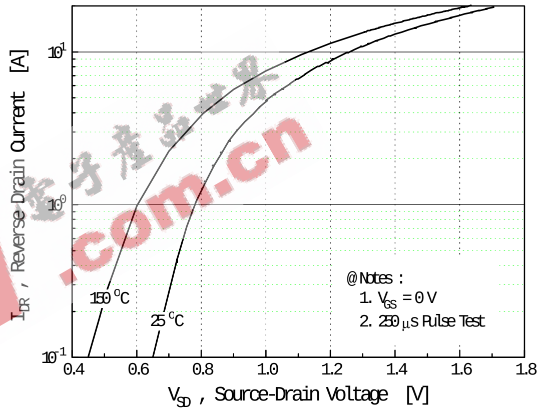


Fig 5. Capacitance vs. Drain-Source Voltage

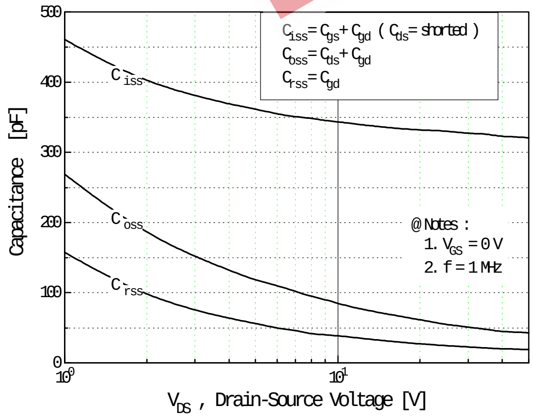


Fig 6. Gate Charge vs. Gate-Source Voltage

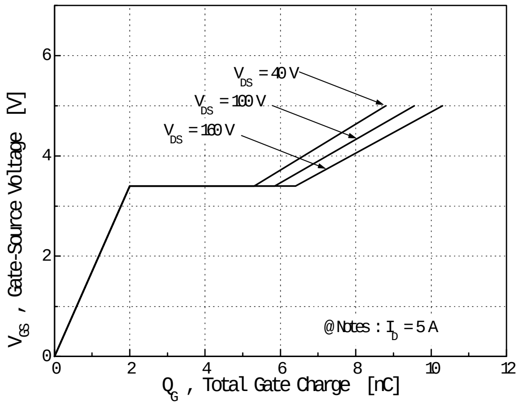


Fig 7. Breakdown Voltage vs. Temperature

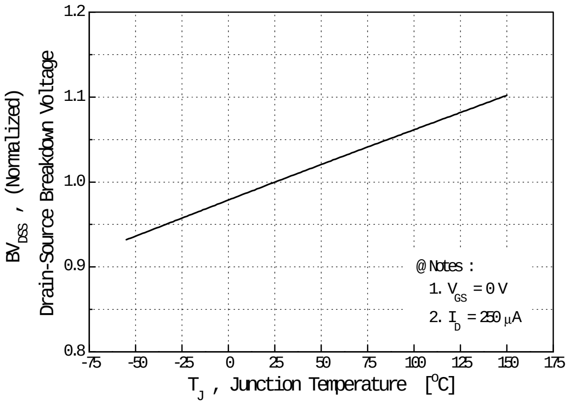


Fig 8. On-Resistance vs. Temperature

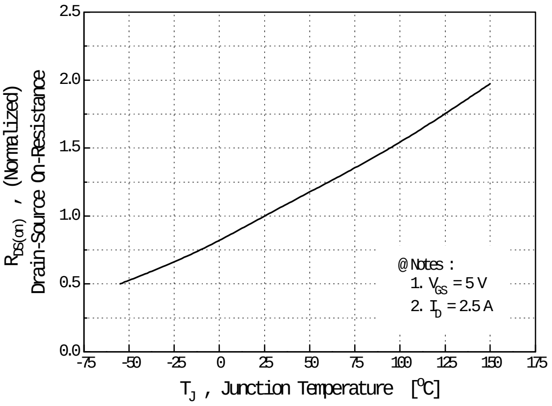


Fig 9. Max. Safe Operating Area

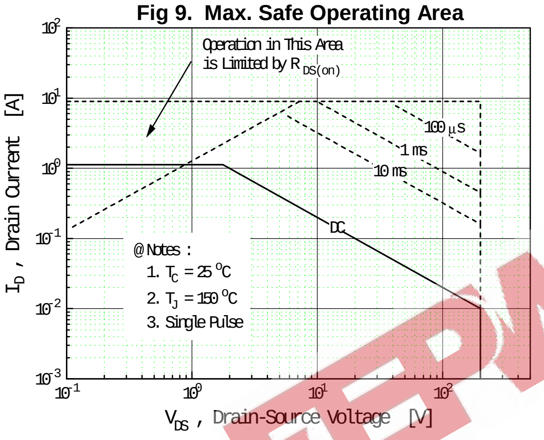


Fig 10. Max. Drain Current vs. Ambient Temperature

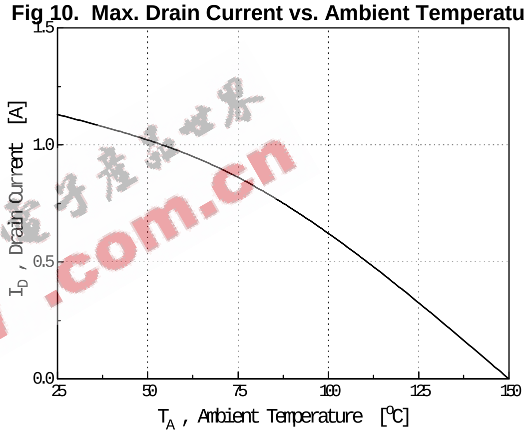


Fig 11. Thermal Response

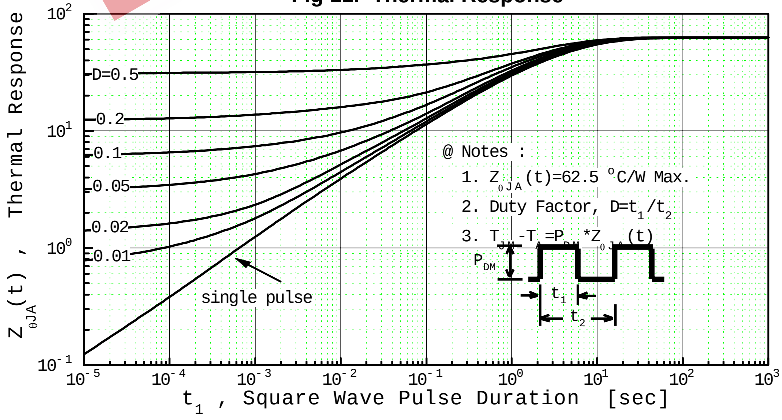


Fig 12. Gate Charge Test Circuit & Waveform

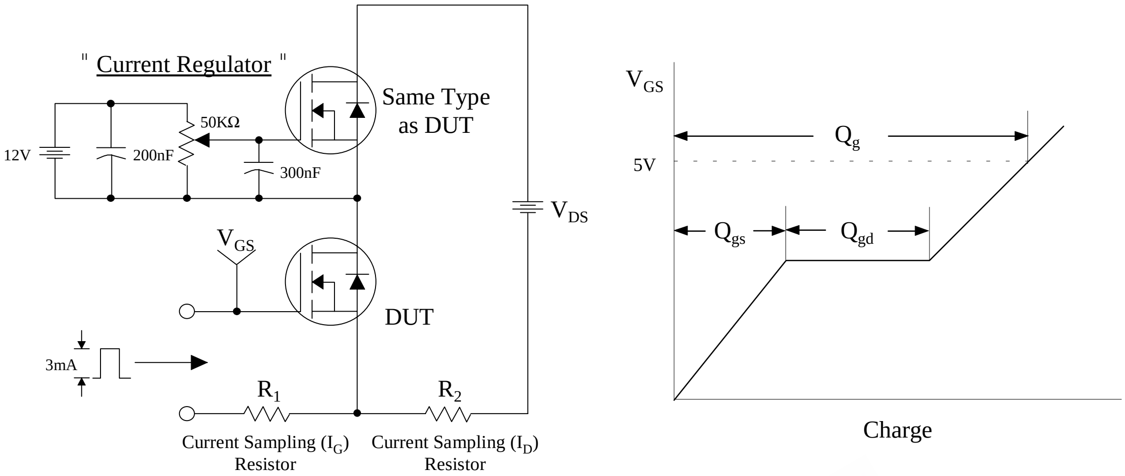


Fig 13. Resistive Switching Test Circuit & Waveforms

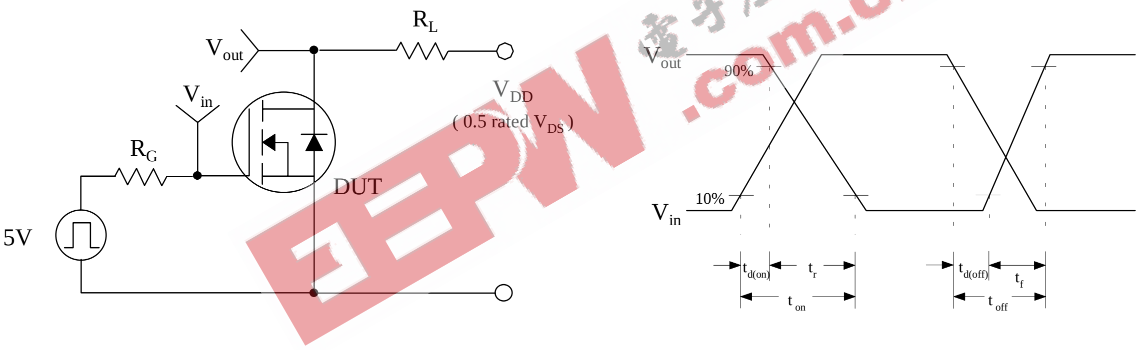


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

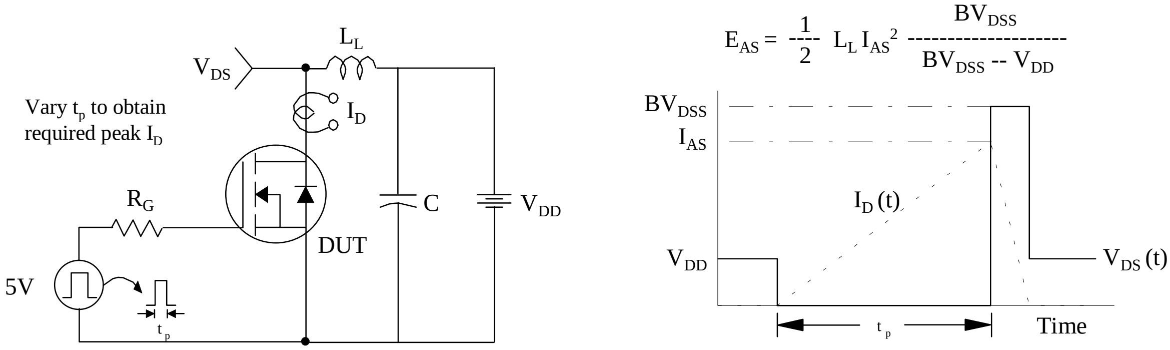
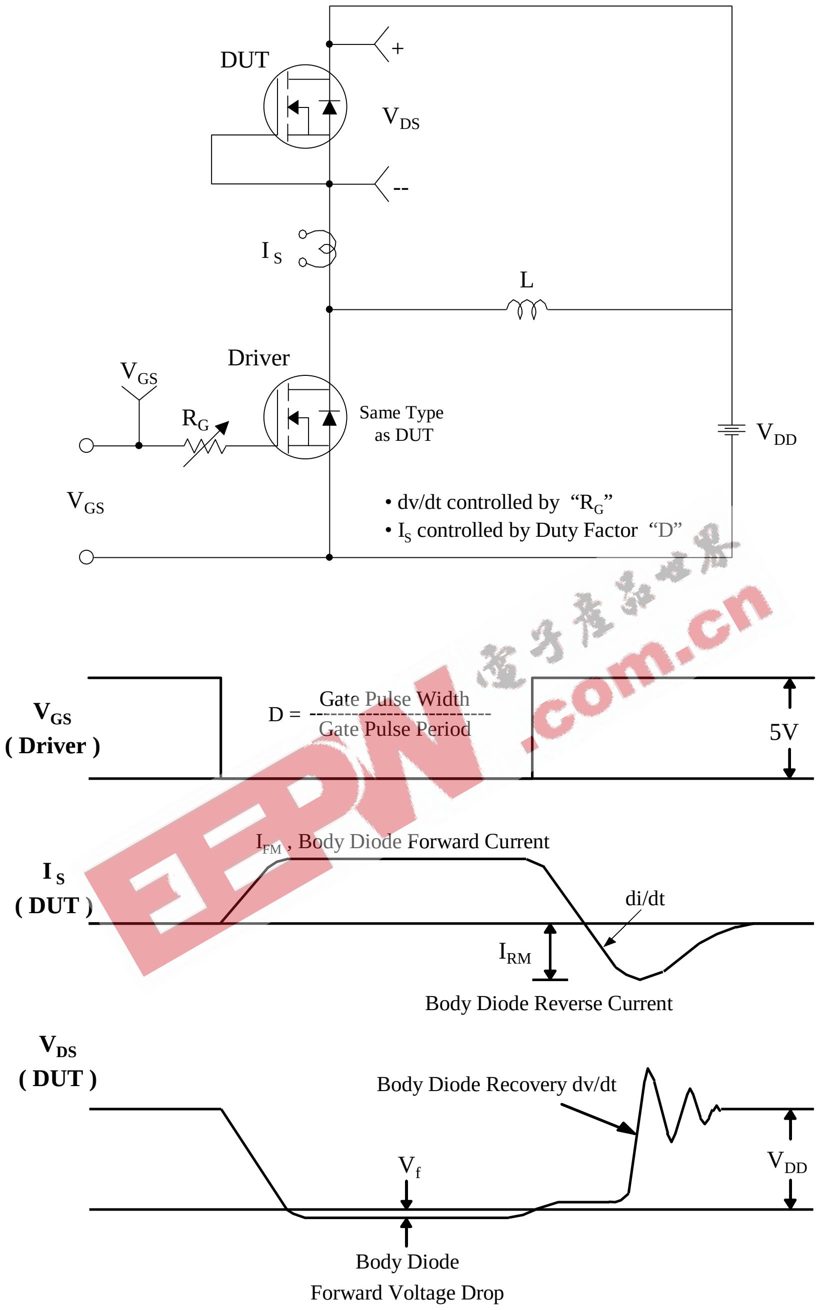


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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