## Low Power RTC with $V_{DD}$ Battery Backed SRAM and Embedded Temp Compensation ±5ppm with Auto Day Light Saving
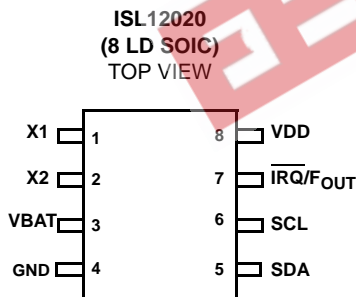
The ISL12020 device is a low power real time clock with an embedded Temp sensor for oscillator compensation, clock/calendar, power fail, low battery monitor, brown out indicator, single periodic or polled alarms, intelligent battery backup switching and 128 bytes of battery-backed user SRAM.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Daylight Savings time adjustment is done automatically, using parameters entered by the user. Power fail and battery monitors offer user-selectable trip levels. A time stamp function records the time and date of switchover from $V_{DD}$ to battery power, and also from battery to $V_{DD}$ power.

### Pinout

**ISL12020**
**(8 LD SOIC)**
TOP VIEW

| Pin | | Pin | |
|---|---|---|---|
| X1 | 1 | 8 | VDD |
| X2 | 2 | 7 | $\overline{IRQ}/F_{OUT}$ |
| VBAT | 3 | 6 | SCL |
| GND | 4 | 5 | SDA |

### Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes and Seconds
  - Day of the Week, Day, Month and Year

- On-chip Oscillator Compensation Over the Operating Temp Range
  - ±5ppm over -20°C to +70°C

- Day Light Saving Time
  - Customer Programmable

- 15 Selectable Frequency Outputs

- 1 Alarm
  - Settable to the Second, Minute, Hour, Day of the Week, Day, or Month
  - Single Event or Pulse Interrupt Mode

- Automatic Backup to Battery or Super Cap
  - Operation to $V_{BAT}$ = 1.8V
  - 1.0µA Battery Supply Current

- Battery Status Monitor, 2 Levels, Selectable by Customer to:
  - Seven Selectable Voltages for Each Level

- Power Status Brown Out Monitor

- Six Selectable Trip Level, from 4.675V to 2.295V Power Failure Detection

- Time Stamp during Power to Battery and Battery to Power Cross Over
  - Time Stamp. First $V_{DD}$ to $V_{BAT}$, and Last $V_{BAT}$ to $V_{DD}$

- 128 Bytes Battery-Backed User SRAM

- $I^2C$ Interface
  - 400kHz Clock Frequency

- 8 Ld SOIC Package ISL12020

- Pb-Free Plus Anneal Available (RoHS Compliant)

### Applications

- Utility Meters

- POS Equipment

- Medical Application

- Security Related Application

- Vending Machine

- White Goods

# ISL12020

## Ordering Information

| PART NUMBER (Note) | PART MARKING | V$_{DD}$ RANGE | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG DWG # |
|---|---|---|---|---|---|
| *Future Product* ISL12020IBZ* | 12020 IBZ | 2.7V to 5.5V | -40 to +85 | 8 Ld SOIC | M8.15 |
| ISL12020CBZ* | 12020 CBZ | 2.7V to 5.5V | -20 to +70 | 8 Ld SOIC | M8.15 |

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram
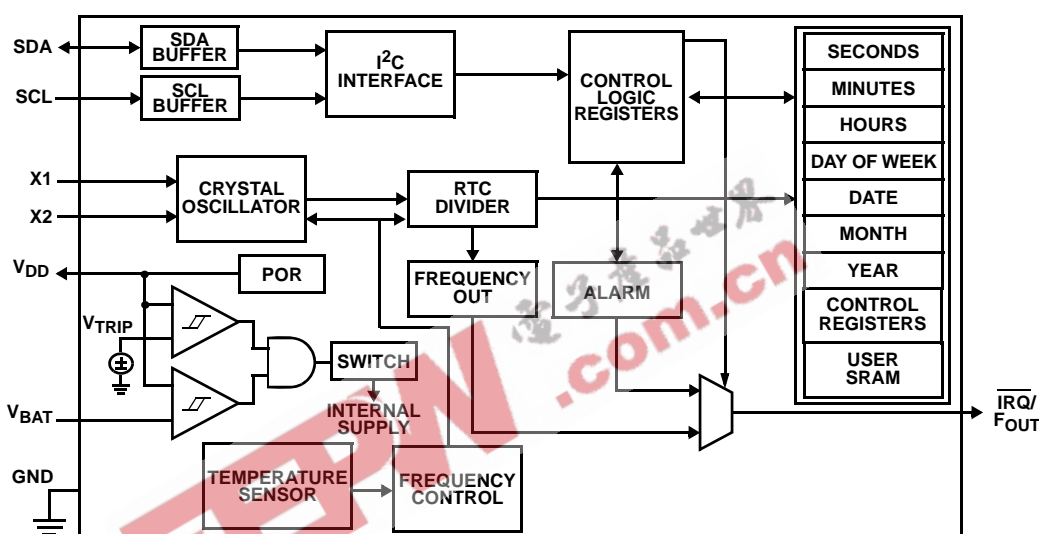


## Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | X1 | **X1.** The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 can also be driven directly from a 32.768kHz source. |
| 2 | X2 | **X2.** The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X2 should be left open when X1 is driven from external source. |
| 3 | VBAT | **VBAT.** This input provides a backup supply voltage to the device. V$_{BAT}$ supplies power to the device in the event that the V$_{DD}$ supply fails. This pin should be tied to ground if not used. |
| 4 | GND | **Ground**. |
| 5 | SDA | **Serial Data** (**SDA**). SDA is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs. |
| 6 | SCL | **Serial Clock** (**SCL**). The SCL input is used to clock all serial data into and out of the device. |
| 7 | IRQ/FOUT | **Interrupt Output IRQ, /Frequency Output FOUT.** Multi-functional pin that can be used as interrupt or frequency output pin. The function is set via the configuration register. |
| 8 | VDD | **VDD.** Power supply. |

# ISL12020

## Absolute Maximum Ratings

Voltage on VDD, VBAT, SCL, SDA, and $\overline{IRQ}/F_{OUT}$ pins
   (respect to ground). . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to 6.0V
Voltage on X1 and X2 pins
   (respect to ground). . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V to 2.5V
ESD Rating
   Human Body Model (Per MIL-STD-883 Method 3014) . . . . .>2kV
   Machine Model. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .>150V

## Thermal Information

Thermal Resistance (Typical, Note 1)          $\theta_{JA}$ (°C/W)
   8 Ld SOIC . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .     120
Storage Temperature. . . . . . . . . . . . . . . . . . . . . . . . .-65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . . . . . . . . . . . . . . . .+300°C
Pb-free reflow profile . . . . . . . . . . . . . . . . . . . . . . . . . .see link below
   http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## DC Operating Characteristics-RTC   Test Conditions: $V_{DD}$ = +2.7 to +5.5V, Temperature = -20°C to +70°C, unless otherwise stated.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP (Note 7) | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Main Power Supply | | 2.7 | | 5.5 | V | |
| $V_{BAT}$ | Battery Supply Voltage | | 1.8 | | 5.5 | V | 2 |
| $I_{DD1}$ | Supply Current | $V_{DD}$ = 5V | | 4.1 | 6.5 | µA | 3, 5 |
| | | $V_{DD}$ = 3V | | 3.5 | 5.5 | µA | 3, 5 |
| $I_{DD2}$ | Supply Current (I²C communications active) | $V_{DD}$ = 5V | | 300 | 500 | µA | 3, 4 |
| $I_{DD3}$ | Supply Current (Temperature Conversion Active) | $V_{DD}$ = 5V | | 250 | 400 | µA | 3, 4 |
| $I_{BAT}$ | Battery Supply Current | $V_{BAT}$ = 3V @ +25°C | | 1.0 | 1.6 | µA | 3 |
| | | $V_{BAT}$ = 3V | | 1.0 | 2.1 | µA | 3 |
| $I_{BATLKG}$ | Battery Input Leakage | $V_{DD}$ = 5.5V, $V_{BAT}$ = 1.8V | | | 100 | nA | |
| $I_{LI}$ | Input Leakage Current on SCL | | | 100 | | nA | 4 |
| $I_{LO}$ | I/O Leakage Current on SDA | | | 100 | | nA | 4 |
| $V_{BATM}$ | Battery Level Monitor Threshold | | -100 | | +100 | mV | |
| $V_{PBM}$ | Brown Out Level Monitor Threshold | | -100 | | +100 | mV | |
| $V_{TRIP}$ | $V_{BAT}$ Mode Threshold | | 2.1 | 2.2 | 2.6 | V | |
| $V_{TRIPHYS}$ | $V_{TRIP}$ Hysteresis | | 10 | 30 | 50 | mV | |
| $V_{BATHYS}$ | $V_{BAT}$ Hysteresis | | | 50 | | mV | 9 |
| | Frequency Stability vs Temperature | 2.7V ≤ $V_{DD}$ ≤ 3.6V, | | ±5 | | ppm | 9 |
| | Frequency Stability vs Voltage | 2.7V ≤ $V_{DD}$ ≤ 3.6V | | ±3 | | ppm | 9 |
| | ATR Sensitivity per LSB | BETA (3:0) = 1000 | | 1 | | ppm | 9 |
| | Temperature Sensor Accuracy | $V_{DD}$ = $V_{BAT}$ = 3.3 V | | ±3 | | °C | 9 |
| $\overline{IRQ}/F_{OUT}$ | | | | | | | |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = 5V, $I_{OL}$ = 3mA | | | 0.4 | V | |
| | | $V_{DD}$ = 2.7V, $I_{OL}$ = 1mA | | | 0.4 | V | |

## Power-Down Timing   Test Conditions: $V_{DD}$ = +2.7 to +5.5V, Temperature = -20°C to +70°C, unless otherwise stated.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP (Note 7) | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ SR- | $V_{DD}$ Negative Slew rate | | | | 10 | V/ms | 8 |

## ISL12020

**I²C Interface Specifications** Test Conditions: $V_{DD}$=+2.7 to +5.5V, Temperature = -20°C to +70°C, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP (Note 7) | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | SDA and SCL input buffer LOW voltage | | -0.3 | | 0.3 x $V_{DD}$ | V | |
| $V_{IH}$ | SDA and SCL Input Buffer HIGH Voltage | | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Hysteresis | SDA and SCL Input Buffer Hysteresis | | 0.05 x $V_{DD}$ | | | V | |
| $V_{OL}$ | SDA Output Buffer LOW Voltage, Sinking 3mA | $V_{DD}$ = 5V, $I_{OL}$ = 3mA | | | 0.4 | V | |
| $C_{PIN}$ | SDA and SCL Pin Capacitance | $T_A$ = +25°C, f = 1MHz, $V_{DD}$ = 5V, $V_{IN}$ = 0V, $V_{OUT}$ = 0V | | | 10 | pF | |
| $f_{SCL}$ | SCL Frequency | | | | 400 | kHz | |
| $t_{IN}$ | Pulse Width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed. | | | 50 | ns | |
| $t_{AA}$ | SCL Falling Edge To SDA Output Data Valid | SCL falling edge crossing 30% of $V_{DD}$, until SDA exits the 30% to 70% of $V_{DD}$ window. | | | 900 | ns | |
| $t_{BUF}$ | Time the Bus Must be Free Before The Start of a New Transmission | SDA crossing 70% of $V_{DD}$ during a STOP condition, to SDA crossing 70% of $V_{DD}$ during the following START condition. | 1300 | | | ns | |
| $t_{LOW}$ | Clock LOW Time | Measured at the 30% of $V_{DD}$ crossing. | 1300 | | | ns | |
| $t_{HIGH}$ | Clock HIGH Time | Measured at the 70% of $V_{DD}$ crossing. | 600 | | | ns | |
| $t_{SU:STA}$ | START Condition Setup Time | SCL rising edge to SDA falling edge. Both crossing 70% of $V_{DD}$. | 600 | | | ns | |
| $t_{HD:STA}$ | START Condition Hold Time | From SDA falling edge crossing 30% of $V_{DD}$ to SCL falling edge crossing 70% of $V_{DD}$. | 600 | | | ns | |
| $t_{SU:DAT}$ | Input Data Setup Time | From SDA exiting the 30% to 70% of $V_{DD}$ window, to SCL rising edge crossing 30% of $V_{DD}$. | 100 | | | ns | |
| $t_{HD:DAT}$ | Input Data Hold Time | From SCL falling edge crossing 30% of $V_{DD}$ to SDA entering the 30% to 70% of $V_{DD}$ window. | 0 | | 900 | ns | |
| $t_{SU:STO}$ | STOP Condition Setup Time | From SCL rising edge crossing 70% of $V_{DD}$, to SDA rising edge crossing 30% of $V_{DD}$. | 600 | | | ns | |
| $t_{HD:STO}$ | STOP Condition Hold Time | From SDA rising edge to SCL falling edge. Both crossing 70% of $V_{DD}$. | 600 | | | ns | |

# ISL12020

## I²C Interface Specifications
Test Conditions: $V_{DD}$=+2.7 to +5.5V, Temperature = -20°C to +70°C, unless otherwise specified. **(Continued)**

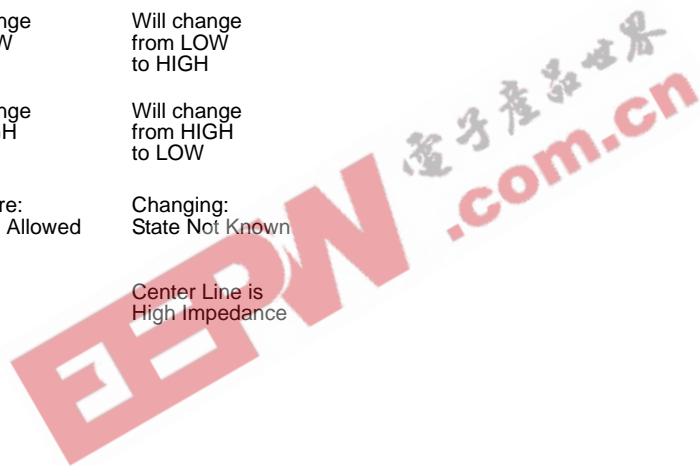| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP (Note 7) | MAX | UNITS | NOTES |
|--------|-----------|-----------------|-----|--------------|-----|-------|-------|
| $t_{DH}$ | Output Data Hold Time | From SCL falling edge crossing 30% of $V_{DD}$, until SDA enters the 30% to 70% of $V_{DD}$ window. | 0 | | | ns | |
| $t_R$ | SDA and SCL Rise Time | From 30% to 70% of $V_{DD}$. | 20 + 0.1 x Cb | | 300 | ns | |
| $t_F$ | SDA and SCL Fall Time | From 70% to 30% of $V_{DD}$. | 20 + 0.1 x Cb | | 300 | ns | |
| Cb | Capacitive loading of SDA or SCL | Total on-chip and off-chip | 10 | | 400 | pF | |
| $R_{PU}$ | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by $t_R$ and $t_F$. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ | 1 | | | kΩ | |

NOTES:

2. Temperature Conversion is inactive below 2.7V $V_{BAT}$

3. $\overline{IRQ}$/$F_{OUT}$ Inactive.

4. $V_{IL}$ = $V_{DD}$ x 0.1, $V_{IH}$ = $V_{DD}$ x 0.9, $f_{SCL}$ = 400kHz

5. $V_{DD}$ > $V_{BAT}$ +$V_{BATHYS}$

6. Bit BSW = 0 (Standard Mode), $V_{BAT} \geq$ 1.8V

7. Specified at +25°C.

8. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.

9. Parameter is not 100% tested.

10. These are I²C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.

## SDA vs SCL Timing
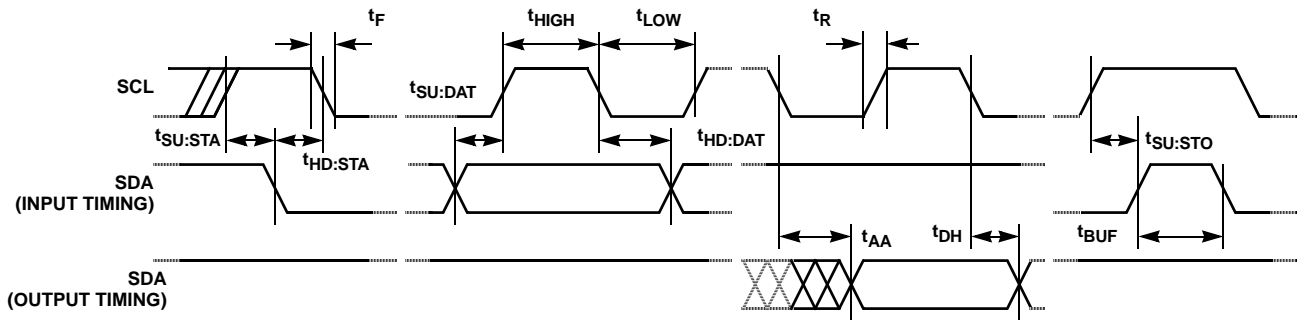


## Symbol Table

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

*intersil*

FN6450.0
March 29, 2007

# ISL12020

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V<sub>DD</sub> = 5V

**5.0V**

**1533Ω**

**FOR V$_{OL}$= 0.4V**
**AND I$_{OL}$ = 3mA**

**SDA AND IRQ/FOUT**

**100pF**
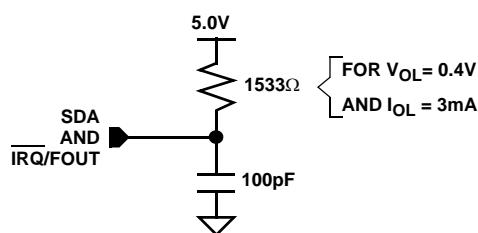
**FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V$_{DD}$ = 5.0V**

## General Description

The ISL12020 devices are low power real time clocks (RTCs) with embedded temperature sensors. They contain crystal frequency compensation circuitry over the operating temperature range, clock/calendar, power fail and low battery monitors, brown out indicator with separate (LVRSET) reset pin (ISL12021 only), 1 periodic or polled alarm, intelligent battery backup switching and 128 Bytes of battery-backed user SRAM.

The oscillator uses an external, low cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction. In addition, both the ISL12020 could be programmed for automatic Daylight Saving Time (DST) adjustment by entering local DST information.

The ISL1202x's alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the IRQ pin. There is a repeat mode for the alarm allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This V$_{BAT}$ pin allows the device to be backed up by battery or Super Cap with automatic switchover from V$_{DD}$ to V$_{BAT}$. The ISL12020 devices are specified for V$_{DD}$ = 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational in battery backup mode down to 1.8V (Standby Mode). The V$_{BAT}$ level is monitored and reported against preselected levels. The first report is registered when the V$_{BAT}$ level falls below 85% of nominal level, the second level is set for 75%. Battery levels are stored in V$_{BATM}$ registers.

The ISL12020 offers a "Brown Out" alarm once the V$_{DD}$ falls below a pre-selected trip level. In the ISL12020, this allows system Micro to save vital information to memory before complete power loss. There are six V$_{DD}$ levels that could be selected for initiation of brown out alarm.

## Pin Descriptions

### X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the device to supply a timebase for the real time clock. Internal compensation circuitry with internal temperature sensor provides frequency corrections for selected popular crystals to ±5ppm over the operating temperature range from -40°C to +85°C. (See "Application Section" on page 22 for recommended crystal). ISL12020 allows the user to input via I2C serial bus the temperature variation profile of crystals not listed in the "Application Section" on page 22. This oscillator compensation network can also be used to calibrate the initial crystal timing accuracy at room temperature. The device can also be driven directly from a 32.768kHz source at pin X1.
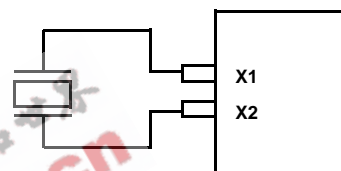
**X1**
**X2**

**FIGURE 2. RECOMMENDED CRYSTAL CONNECTION**

### VBAT

This input provides a backup supply voltage to the device. VBAT supplies power to the device in the event that the VDD supply fails. This pin can be connected to a battery, a Super Capacitor or tied to ground if not used. See the Battery Monitor parameter in the *DC Operating Characteristics-RTC on page 3*.

### IRQ/F$_{OUT}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The IRQ/F$_{OUT}$ mode is selected via the frequency out control bits of the control/status register.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active low output.

- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I$^2$C bus. It is an open drain output.

### Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the V$_{BAT}$ pin is activated to minimize power consumption.

*intersil*

### Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I$^2$C interface speeds. It is disabled when the backup power supply on the $V_{BAT}$ pin is activated.

### VDD, GND

Chip power supply and ground pins. The device will operate with a power supply from VDD = 2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the VDD pin to ground.

## Functional Description

### Power Control Operation

The power control circuit accepts a $V_{DD}$ and a $V_{BAT}$ input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL1202x for up to 10 years. Another option is to use a Super Capacitor for applications where $V_{DD}$ is interrupted for up to a month. See the "Application Section" on page 22 for more information.

### Normal Mode ($V_{DD}$) to Battery Backup Mode ($V_{BAT}$)

To transition from the VDD to VBAT mode, <u>both</u> of the following conditions must be met:

**Condition 1:**

$V_{DD} < V_{BAT} - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

**Condition 2:**

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

### Battery Backup Mode ($V_{BAT}$) to Normal Mode ($V_{DD}$)

The ISL12020 device will switch from the $V_{BAT}$ to $V_{DD}$ mode when <u>one</u> of the following conditions occurs:

**Condition 1:**

$V_{DD} > V_{BAT} + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

**Condition 2:**

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

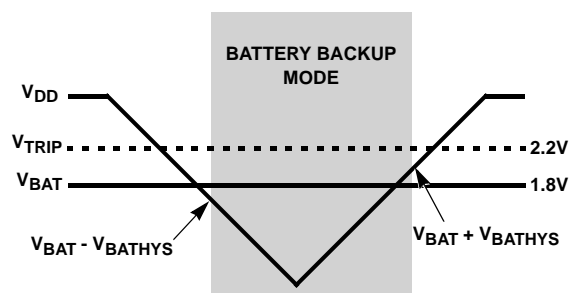These power control situations are illustrated in Figure 3 and Figure 4.
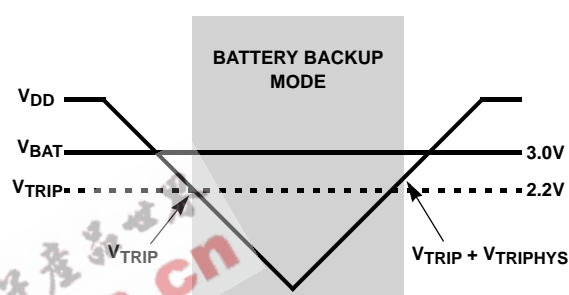


**FIGURE 3. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$**



**FIGURE 4. BATTERY SWITCHOVER WHEN $V_{BAT} > V_{TRIP}$**

The I$^2$C bus is deactivated in battery backup mode to reduce power consumption. Aside from this, all RTC functions are operational during battery backup mode. Except for SCL and SDA, all the inputs and outputs of the ISL12020 are active during battery backup mode unless disabled via the control register.

The device Time Stamps the switchover from $V_{DD}$ to $V_{BAT}$ and $V_{BAT}$ to $V_{DD}$, and the time is stored in $T_{SV2B}$ and $T_{SB2V}$ registers respectively. If multiple $V_{DD}$ power down sequences occur before status is read, the earliest $V_{DD}$ to $V_{BAT}$ power down time is stored and the most recent $V_{BAT}$ to $V_{DD}$ time is stored.

Temperature conversion and compensation can be enabled in battery backup mode. Bit BTSE in the BETA register controls this operation as described in that register section.

### Power Failure Detection

Both the ISL12020 provide a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both $V_{DD}$ and $V_{BAT}$).

### Brownout Detection

The ISL12020 monitor the $V_{DD}$ level continuously and provide warning if the $V_{DD}$ level drops below prescribed levels. There are six (6) levels that can be selected for the trip level. These values are 85% below popular $V_{DD}$ levels. The LVDD bit in the Status Register will be set to "1" when Brownout is detected. Note. The I$^2$C serial bus remains active unless the Battery Vtrip levels are reached.

### Battery Level Monitor

The ISL12020 have a built in warning feature once the Back Up battery level drops first to 85% and then to 75% of the battery's nominal VBAT level. When the battery voltage drops to between 85% and 75%, the LBAT85 bit is set in the status register. When the level drops below 75%, both LBAT85 and LBAT75 bits are set in the status register.

There is a Battery Timestamp Function available. Once the $V_{DD}$ is low enough to enable switchover to the battery, the RTC time/date are written into the TSVTB register. This information can be read from the TSVTB registers to discover the point in time of the $V_{DD}$ powerdown. If there are multiple powerdown cycles before reading these registers, the first values stored in these registers will be retained. These registers will hold the original powerdown value until they are cleared by writing "00h" to each register.

### Low Power Mode

The normal power switching of the ISL12020 is designed to switch into battery backup mode only if the $V_{DD}$ power is lost. This will ensure that the device can accept a wide range of backup voltages from many types of sources while reliably switching into backup mode. Another mode (called Low Power Mode) is available to allow direct switching from $V_{DD}$ to $V_{BAT}$ without requiring $V_{DD}$ to drop below $V_{TRIP}$. Since the additional monitoring of $V_{DD}$ vs $V_{TRIP}$ is no longer needed, that circuitry is shut down and less power is used while operating from $V_{DD}$. Power savings are typically 600nA at $V_{DD}$ = 5V. Low Power Mode is activated via the BSW bit in the control and status registers.

Low Power Mode is useful in systems where $V_{DD}$ is normally higher than $V_{BAT}$ at all times. The device will switch from $V_{DD}$ to $V_{BAT}$ when $V_{DD}$ drops below $V_{BAT}$, with about 50mV of hysteresis to prevent any switchback of $V_{DD}$ after switchover. In a system with $V_{DD}$ = 5V and backup lithium battery of $V_{BAT}$ = 3V, Low Power Mode can be used. However, it is not recommended to use Low Power Mode in a system with $V_{DD}$ = 3.3V ±10%, $V_{BAT} \geq 3.0V$, and when there is a finite I-R voltage drop in the $V_{DD}$ line.

## Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12020 powers up after the loss of both $V_{DD}$ and $V_{BAT}$, the clock will not begin incrementing until at least one byte is written to the clock register.

### Single Event and Interrupt

The alarm mode is enabled via the MSB bit. Choosing single event or interrupt alarm mode is selected via the IM bit. Note that when the frequency output function is enabled, the alarm function is disabled.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, an $\overline{IRQ}$ pin will be pulled low and the alarm status bit (ALM) will be set to "1".

The pulsed interrupt mode allows for repetitive or recurring alarm functionality. Hence, once the alarm is set, the device will continue to alarm for each occurring match of the alarm and present time. Thus, it will alarm as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled low for 250ms and the alarm status bit (ALM) will be set to "1".

The ALM bit can be reset by the user or cleared automatically using the auto reset mode (see ARST bit). The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit. For more information on the alarm, please see "ALARM Registers (10h to 15h)" on page 17.

### Frequency Output Mode

The ISL12020 has the option to provide a clock output signal using the IRQ/FOUT open drain output pin. The frequency output mode is set by using the FO bits to select 15 possible output frequency values from 1/32Hz to 32kHz. The frequency output can be enabled/disabled during battery backup mode using the FOBATB bit.

### General Purpose User SRAM

The ISL12020 provides 128 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the $I^2C$ bus is disabled in battery backup mode.

### $I^2C$ Serial Interface

The ISL12020 has an $I^2C$ serial bus interface that provides access to the control and status registers and the user SRAM. The $I^2C$ serial interface is compatible with other industry $I^2C$ serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

### Oscillator Compensation

The ISL12020 provides both initial timing correction and temperature correction due to variation of the crystal oscillator. Analog and Digital trimming control is provided for initial adjustment, and a temperature compensation function is provided to automatically correct for temperature drift of the crystal. Initial values for the temperature coefficient (ALPHA) and crystal capacitance (BETA) are required for best accuracy. The function can be enabled/disabled at any time and can be used in battery mode as well.

## *Register Descriptions*

The battery-backed registers are accessible following a slave byte of "1101111x" and reads or writes to addresses [00h:13h]. The defined addresses and default values are described in the Table 1. The battery backed general purpose SRAM has a different slave address (1010111x), so it is not possible to read/write that section of memory while accessing the registers.

### REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 8 sections. They are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (9 bytes): Address 07h to 0Fh.
3. Alarm (6 bytes): Address 10h to 15h.
4. Time Stamp for Battery Status (5 bytes): Address 16h to 1Ah.
5. Time Stamp for VDD Status (5 bytes): Address 1Bh to 1Fh.
6. Day Light Saving Time (8 bytes): 20h to 27h.
7. TEMP (2 bytes): 28h to 29h
8. Scratch Pad (6 bytes): Address 2Ah to 2Fh.

Write capability is allowable into the RTC registers (00h to 06h) only when the WRTC bit (bit 6 of address 08h) is set to "1". **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is not necessary to set the WRTC bit prior to writing into the control and status, alarm, and user SRAM registers.

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**TABLE 1. REGISTER MEMORY MAP**

| ADDR. | SECTION | REG NAME | BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RANGE | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | RTC | SC | 0 | SC22 | SC21 | SC20 | SC13 | SC12 | SC11 | SC10 | 0 to 59 | 00h |
| 01h | | MN | 0 | MN22 | MN21 | MN20 | MN13 | MN12 | MN11 | MN10 | 0 to 59 | 00h |
| 02h | | HR | MIL | 0 | HR21 | HR20 | HR13 | HR12 | HR11 | HR10 | 0 to 23 | 00h |
| 03h | | DT | 0 | 0 | DT21 | DT20 | DT13 | DT12 | DT11 | DT10 | 1 to 31 | 01h |
| 04h | | MO | 0 | 0 | 0 | MO20 | MO13 | MO12 | MO11 | MO10 | 1 to 12 | 01h |
| 05h | | YR | YR23 | YR22 | YR21 | YR20 | YR13 | YR12 | YR11 | YR10 | 0 to 99 | 00h |
| 06h | | DW | 0 | 0 | 0 | 0 | 0 | DW2 | DW1 | DW0 | 0 to 6 | 00h |
| 07h | CSR | SR | BUSY | OSCF | DSTADJ | ALM | LVDD | LBAT85 | LBAT75 | RTCF | N/A | 01h |
| 08h | | INT | ARST | WRTC | IM | FOBATB | FO3 | FO2 | FO1 | FO0 | N/A | 00h |
| 09h | | PWR_VDD | CLRTS | D | D | D | D | $V_{DD}$Trip2 | $V_{DD}$Trip1 | $V_{DD}$Trip0 | N/A | 00h |
| 0Ah | | PWR_VBAT | BSW | D | VB85Tp2 | VB85Tp1 | VB85Tp0 | VB75Tp2 | VB75Tp1 | VB75Tp0 | N/A | 00h |
| 0Bh | | ITRO | IDTR01 | IDTR00 | IATR05 | IATR04 | IATR03 | IATR02 | IATR01 | IATR00 | N/A | 08h |
| 0Ch | | ALPHA | D | ALPHA6 | ALPHA5 | ALPHA4 | ALPHA3 | ALPHA2 | ALPHA1 | ALPHA0 | N/A | 25h |
| 0Dh | | BETA | TSE | BTSE | BTSR | D | BETA3 | BETA2 | BETA1 | BETA0 | N/A | 08h |
| 0Eh | | FATR | 0 | 0 | FFATR5 | FATR4 | FATR3 | FATR2 | FATR1 | FATR0 | N/A | 00h |
| 0Fh | | FDTR | 0 | 0 | 0 | 0 | 0 | FDTR2 | FDTR1 | FDTR0 | N/A | 00h |
| 10h | ALARM | SCA0 | ESCA0 | SCA022 | SCA021 | SCA020 | SCA013 | SCA012 | SCA011 | SCA010 | 00 to 59 | 00h |
| 11h | | MNA0 | EMNA0 | MNA022 | MNA021 | MNA020 | MNA013 | MNA012 | MNA011 | MNA010 | 00 to 59 | 00h |
| 12h | | HRA0 | EHRA0 | D | HRA021 | HRA020 | HRA013 | HRA012 | HRA011 | HRA010 | 0 to 23 | 00h |
| 13h | | DTA0 | EDTA0 | D | DTA021 | DTA020 | DTA013 | DTA012 | DTA011 | DTA010 | 01 to 31 | 01h |
| 14h | | MOA0 | EMOA00 | D | D | MOA020 | MOA013 | MOA012 | MOA011 | MOA010 | 01 to 12 | 01h |
| 15h | | DWA0 | EDWA0 | D | D | D | D | DWA02 | DWA01 | DWA00 | 0 to 6 | 00h |
| 16h | TSV2B | VSC | 0 | VSC22 | VSC21 | VSC20 | VSC13 | VSC12 | VSC11 | VSC10 | 0 to 59 | 00h |
| 17h | | VMN | 0 | VMN22 | VMN21 | VMN20 | VMN13 | VMN12 | VMN11 | VMN10 | 0 to 59 | 00h |
| 18h | | VHR | VMIL | 0 | VHR21 | VHR20 | VHR13 | VHR12 | VHR11 | VHR10 | 0 to 23 | 00h |
| 19h | | VDT | 0 | 0 | VDT21 | VDT20 | VDT13 | VDT12 | VDT11 | VDT10 | 1 to 31 | 00h |
| 1Ah | | VMO | 0 | 0 | 0 | VMO20 | VMO13 | VMO12 | VMO11 | VMO10 | 1 to 12 | 00h |
| 1Bh | TSB2V | BSC | 0 | BSC22 | BSC21 | BSC20 | BSC13 | BSC12 | BSC11 | BSC10 | 0 to 59 | 00h |
| 1Ch | | BMN | 0 | BMN22 | BMN21 | BMN20 | BMN13 | BMN12 | BMN11 | BMN10 | 0 to 59 | 00h |
| 1Dh | | BHR | BMIL | 0 | BHR21 | BHR20 | BHR13 | BHR12 | BHR11 | BHR10 | 0 to 23 | 00h |
| 1Eh | | BDT | 0 | 0 | BDT21 | BDT20 | BDT13 | BDT12 | BDT11 | BDT10 | 1 to 31 | 00h |
| 1Fh | | BMO | 0 | 0 | 0 | BMO20 | BMO13 | BMO12 | BMO11 | BMO10 | 1 to 12 | 00h |

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**TABLE 1. REGISTER MEMORY MAP (Continued)**

| ADDR. | SECTION | REG NAME | BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | RANGE | DEFAULT |
|-------|---------|----------|-------|---|---|---|---|---|---|---|-------|---------|
| 20h | DSTCR | DstMoFd | DSTE | D | D | DstMoFd20 | DstMoFd13 | DstMoFd12 | DstMoFd11 | DstMoFd10 | 1 to 12 | 00h |
| 21h | | DstDwFd | DstDwEFd | D | D | D | D | DstDwFd12 | DstDwFd11 | DstDwFd10 | 0 to 6 | 00h |
| 22h | | DstDtFd | D | D | DstDtFd21 | DstDtFd20 | DstDtFd13 | DstDtFd12 | DstDtFd11 | DstDtFd10 | 1 to 31 | 00h |
| 23h | | DstHrFd | D | D | DstHrFd21 | DstHrFd20 | DstHrFd13 | DstHrFd12 | DstHrFd11 | DstHrFd10 | 0 to 23 | 00h |
| 24h | | DstMoRv | D | D | D | XDstMoRv20 | DstMoRv13 | DstMoR12v | DstMoRv11 | DstMoRv10 | 01 to 12 | 00h |
| 25h | | DstDwRv | DstDwERv | D | D | D | D | DstDwRv12 | DstDwRv11 | DstDwRv10 | 0 to 6 | 00h |
| 26h | | DstDtRv | D | D | DstDtRv21 | DstDtRv20 | DstDtRv13 | DstDtRv12 | DstDtRv11 | DstDtRv10 | 01 to 31 | 00h |
| 27h | | DstHrRv | D | D | DstHrRv21 | DstHrRv20 | DstHrRv13 | DstHrRv12 | DstHrRv11 | DstHrRv10 | 0 to 23 | 00h |
| 28h | TEMP | TK0L | TK07 | TK06 | TK05 | TK04 | TK03 | TK02 | TK01 | TK00 | 00 to FF | 00h |
| 29h | | TK0M | 0 | 0 | 0 | 0 | 0 | 0 | TK09 | TK08 | 00 to 03 | 00h |
| 2Ah | GPM | GPM1 | GPM17 | GPM16 | GPM15 | GPM14 | GPM13 | GPM12 | GPM11 | GPM10 | 00 to FF | 00h |
| 2Bh | | GPM2 | GPM27 | GPM26 | GPM25 | GPM24 | GPM23 | GPM22 | GPM21 | GPM20 | 00 to FF | 00h |
| 2Ch | | GPM3 | GPM37 | GPM36 | GPM35 | GPM34 | GPM33 | GPM32 | GPM31 | GPM30 | 00 to FF | 00h |
| 2Dh | | GPM4 | GPM47 | GPM46 | GPM45 | GPM44 | GPM43 | GPM42 | GPM41 | GPM40 | 00 to FF | 00h |
| 2Eh | | GPM5 | GPM57 | GPM56 | GPM55 | GPM54 | GPM53 | GPM52 | GPM51 | GPM50 | 00 to FF | 00h |
| 2Fh | | GPM6 | GPM67 | GPM66 | GPM65 | GPM64 | GPM63 | GPM62 | GPM61 | GPM60 | 00 to FF | 00h |

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## Real Time Clock Registers

### Addresses [00h to 06h]

#### RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can either be a 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, and DW (Day of the Week) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as "0".

#### 24 HOUR TIME

If the MIL bit of the HR register is "1", the RTC uses a 24-hour format. If the MIL bit is "0", the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a "1" representing PM. The clock defaults to 12-hour format time with HR21 = "0".

#### LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12020 does not correct for the leap year in the year 2100.

## Control and Status Registers (CSR)

### Addresses [07h to 0Fh]

The Control and Status Registers consist of the Status Register, Interrupt and Alarm Register, Analog Trimming and Digital Trimming Registers.

### Status Register (SR)

The Status Register is located in the memory map at address 07h. This is a volatile register that provides either control or status of RTC failure (RTCF), Battery Level Monitor (LBAT85, LBAT75), alarm trigger, Daylight Saving Time, crystal oscillator enable and temperature conversion in progress bit.

**TABLE 2. STATUS REGISTER (SR)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 07h | BUSY | OSCF | DSTDJ | ALM | LVDD | LBAT85 | LBAT75 | RTCF |

#### BUSY BIT (BUSY)

Busy Bit indicates temperature sensing is in progress. In this mode, Alpha, Beta and ITRO registers are disabled and cannot be accessed.

#### OSCILLATOR FAIL BIT (OSCF)

Indicates oscillator stopped.

#### DAYLIGHT SAVING TIME CHANGE BIT (DSTADJ)

DSTADJ is the Daylight Saving Time Adjusted Bit. It indicates the daylight saving time adjustment has happened. DSTADJ is reset to 0 upon power up. If DST event happens (at either the beginning or the end of DST), DSTADJ will be set to 1. A read of the SR will reset the DSTADJ, or it will be automatically reset on the following month.

#### ALARM BIT (ALM)

These bits announce if the alarm matches the real time clock. If there is a match, the respective bit is set to "1". This bit can be manually reset to "0" by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to "0", not "1". An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

#### LOW $V_{DD}$ INDICATOR BIT (LV$_{DD}$VDD)

Indicates $V_{DD}$ dropped below the pre-selected trip level. (Brown Out Mode). The Trip points for Brown Out levels are selected by three bits $V_{DD}$Trip2, $V_{DD}$Trip1 and $V_{DD}$Trip0 in PWR_$V_{DD}$ registers.

#### LOW BATTERY INDICATOR 85% BIT (LBAT85)

Indicates battery level dropped below the pre-selected trip levels (85% of battery voltage). The trip points are selected by three bits: VB85Tp2, VB85Tp1 and VB85Tp0 in the PWR_VBAT registers.

#### LOW BATTERY INDICATOR 75% BIT (LBAT75)

Indicates battery level dropped below the pre-selected trip levels (75% of battery voltage). The trip points are selected by three bits VB75Tp2, VB75Tp1 and VB75Tp0 in the PWR_VBAT registers.

#### REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a "1" after a total power failure. This is a read only bit that is set by hardware (ISL12020 internally) when the device powers up after having lost all power (defined as $V_{DD}$ = 0V and $V_{BAT}$ = 0V). The bit is set regardless of whether $V_{DD}$ or $V_{BAT}$ is applied first. The loss of only one of the supplies does not set the RTCF bit to "1". The first valid write to the RTC section after a complete power failure resets the RTCF bit to "0" (writing one byte is sufficient).

### Interrupt Control Register (INT)

**TABLE 3. INTERRUPT CONTROL REGISTER (INT)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 08h | ARST | WRTC | IM | FOBATB | FO3 | FO2 | FO1 | FO0 |

#### AUTOMATIC RESET BIT (ARST)

This bit enables/disables the automatic reset of the ALM, LVDD, LBAT85, and LBAT75 status bits only. When ARST bit is set to "1", these status bits are reset to "0" after a valid read of the respective status register (with a valid STOP

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condition). When the ARST is cleared to "0", the user must manually reset the ALM, LVDD, LBAT85, and LBAT75 bits.

## WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is "0". Upon initialization or power up, the WRTC must be set to "1" to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

## INTERRUPT/ALARM MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to "1", the alarm will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}$/$F_{OUT}$ pin when the RTC is triggered by the alarm as defined by the alarm registers (0Ch to 11h). When the IM bit is cleared to "0", the alarm will operate in standard mode, where the $\overline{IRQ}$/FOUT pin will be set low until the ALM status bit is cleared to "0".

**TABLE 4.**

| IM BIT | INTERRUPT/ALARM FREQUENCY |
|---|---|
| 0 | Single Time Event Set By Alarm |
| 1 | Repetitive/Recurring Time Event Set By Alarm |

## FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables the FOUT/$\overline{IRQ}$ pin during battery backup mode (i.e. $V_{BAT}$ power source active). When the FOBATB is set to "1" the FOUT/$\overline{IRQ}$ pin is disabled during battery backup mode. This means that both the frequency output and alarm output functions are disabled. When the FOBATB is cleared to "0", the FOUT/$\overline{IRQ}$ pin is enabled during battery backup mode. Note that the open drain FOUT/$\overline{IRQ}$ pin will need a pullup to the battery voltage to operate in battery backup mode.

## FREQUENCY OUT CONTROL BITS (FO <3:0>)

These bits enable/disable the frequency output function and select the output frequency at the $\overline{IRQ}$/FOUT pin. See Table 5 for frequency selection. When the frequency mode is enabled, it will override the alarm mode at the $\overline{IRQ}$/FOUT pin.

**TABLE 5. FREQUENCY SELECTION OF FOUT PIN**

| FREQUENCY, FOUT | UNITS | FO3 | FO2 | FO1 | FO0 |
|---|---|---|---|---|---|
| 0 | Hz | 0 | 0 | 0 | 0 |
| 32768 | Hz | 0 | 0 | 0 | 1 |
| 4096 | Hz | 0 | 0 | 1 | 0 |
| 1024 | Hz | 0 | 0 | 1 | 1 |
| 64 | Hz | 0 | 1 | 0 | 0 |
| 32 | Hz | 0 | 1 | 0 | 1 |

**TABLE 5. FREQUENCY SELECTION OF FOUT PIN (Continued)**

| FREQUENCY, FOUT | UNITS | FO3 | FO2 | FO1 | FO0 |
|---|---|---|---|---|---|
| 16 | Hz | 0 | 1 | 1 | 0 |
| 8 | Hz | 0 | 1 | 1 | 1 |
| 4 | Hz | 1 | 0 | 0 | 0 |
| 2 | Hz | 1 | 0 | 0 | 1 |
| 1 | Hz | 1 | 0 | 1 | 0 |
| 1/2 | Hz | 1 | 0 | 1 | 1 |
| 1/4 | Hz | 1 | 1 | 0 | 0 |
| 1/8 | Hz | 1 | 1 | 0 | 1 |
| 1/16 | Hz | 1 | 1 | 1 | 0 |
| 1/32 | Hz | 1 | 1 | 1 | 1 |

## POWER SUPPLY CONTROL REGISTER (PWR_VDD)

### Clear Time Stamp Bit (CLRTS)

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 09h | CLRTS | 0 | 0 | 0 | 0 | $V_{DD}$Trip2 | $V_{DD}$Trip1 | $V_{DD}$Trip0 |

This bit clears Time Stamp $V_{DD}$ to Battery (TSV2B) and Time Stamp Battery to $V_{DD}$ Registers (TSB2V). The default setting is 0 (CLRTS = 0) and the Enabled setting is 1 (CLRTS = 1)

### $V_{DD}$ Brown Out Trip Voltage BITS (VDDTrip)<2:0>

These bits set the 6 trip levels for the $V_{DD}$ alarm, indicating that $V_{DD}$ has dropped below a preset level, in this event, the LVDD bit in the Status Register is set to "1". See Table 6.

**TABLE 6. VDD TRIP LEVELS**

| $V_{DD}$Trip2 | $V_{DD}$Trip1 | $V_{DD}$Trip0 | TRIP VOLTAGE (V) |
|---|---|---|---|
| 0 | 0 | 0 | 2.295 |
| 0 | 0 | 1 | 2.550 |
| 0 | 1 | 0 | 2.805 |
| 0 | 1 | 1 | 3.060 |
| 1 | 0 | 0 | 4.250 |
| 1 | 0 | 1 | 4.675 |

## Battery Voltage Trip Voltage Register (PWR_VBAT)

This register controls the trip points for the two VBAT alarms, with levels set to approximately 85% and 75% of the nominal battery level.

**TABLE 7.**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Ah | BSW | 0 | VB85 Tp2 | VB85 Tp1 | VB85 Tp0 | VB75 Tp2 | VB75 Tp1 | VB75 Tp0 |

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## BATTERY SWITCHOVER BIT (BSW)

This bit selects either standard mode or low power mode battery switchover. In standard Mode (BSW = 0), the $V_{DD}$ switches over to battery at the low trip point, typically 2.2V. In Low Power Mode (BSW = 1), $V_{DD}$ switches over to battery at the battery voltage ($V_{BAT}$). Low power mode uses less power in battery backup for applications requiring longer backup times.

## BATTERY LEVEL MONITOR TRIP BITS (VB85TP <2:0>)

Three bits selects the first alarm (85% of Nominal VBAT) level for the battery voltage monitor. There are total of 7 levels that could be selected for the first alarm. Any of the of levels could be selected as the first alarm with no reference as to nominal Battery voltage level. See Table 8.

**TABLE 8. VB85T ALARM LEVEL**

| VB85Tp2 | VB85Tp1 | VB85Tp0 | BATTERY ALARM TRIP LEVEL (V) |
|---------|---------|---------|------------------------------|
| 0 | 0 | 0 | 2.125 |
| 0 | 0 | 1 | 2.295 |
| 0 | 1 | 0 | 2.550 |
| 0 | 1 | 1 | 2.805 |
| 1 | 0 | 0 | 3.060 |
| 1 | 0 | 1 | 4.250 |
| 1 | 1 | 0 | 4.675 |

## BATTERY LEVEL MONITOR TRIP BITS (VB75TP <2:0>)

Three bits selects the second alarm (75% of Nominal VBAT) level for the battery voltage monitor. There are total of 7 levels that could be selected for the second alarm. Any of the of levels could be selected as the second alarm with no reference as to nominal Battery voltage level. See Table 9.

**TABLE 9. BATTERY LEVEL MONITOR TRIP BITS (VB75TP <2:0>)**

| VB75Tp2 | VB75Tp1 | VB75Tp0 | BATTERY ALARM TRIP LEVEL (V) |
|---------|---------|---------|------------------------------|
| 0 | 0 | 0 | 1.875 |
| 0 | 0 | 1 | 2.025 |
| 0 | 1 | 0 | 2.250 |
| 0 | 1 | 1 | 2.475 |
| 1 | 0 | 0 | 2.700 |
| 1 | 0 | 1 | 3.750 |
| 1 | 1 | 0 | 4.125 |

## *Initial ATR and DTR setting Register (ITRO)*

These bits are to be used to trim the initial error (at room temperature) of the crystal. Both digital (DTR) and analog (ATR) trimming methods are available. The digital trimming uses clock pulse skipping and insertion for frequency adjustment. Analog trimming uses load capacitance adjustment to pull the oscillator frequency. A range of +64ppm to -63ppm is possible with combined Digital and Analog trimming.

## AGING AND INITIAL TRIM DIGITAL TRIMMING BITS (IDTR0) <2:0>

These bits allow ±32ppm initial trimming range for the crystal frequency. This is meant to be a coarse adjustment if the range needed is outside that of the IATR control. See Table 10. The IDTR0 register should only be changed while the TSE (Temp Sense Enable) bit is "0".

**TABLE 10. IDTR0 TRIMMING RANGE**

| IDTR01 | IDTR00 | TRIMMING RANGE |
|--------|--------|----------------|
| 0 | 0 | Default /Disabled |
| 0 | 1 | +32ppm |
| 1 | 0 | 0ppm |
| 1 | 1 | -32ppm |

## AGING AND INITIAL ANALOG TRIMMING BITS (IATR0)<6:0>

The analog trimming register allows +32ppm to -31ppm adjustment in 1ppm/bit increments. This enables fine frequency adjustment for trimming initial crystal accuracy error or to correct for aging drift. The IATR0 register should only be changed while the TSE (temp sense enable) bit is "0".

**TABLE 11. INITIAL ATR AND DTR SETTING REGISTER**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| 0Bh | IDTR01 | IDTR00 | IATR05 | IATR04 | IATR03 | IATR02 | IATR01 | IATR00 |

**TABLE 12. IATRO TRIMMING RANGE**

| IATR05 | IATR04 | IATR03 | IATR02 | IATR01 | IATR00 | TRIMMING RANGE |
|--------|--------|--------|--------|--------|--------|----------------|
| **0** | **0** | **0** | **0** | **0** | **0** | **+32** |
| 0 | 0 | 0 | 0 | 0 | 1 | +31 |
| 0 | 0 | 0 | 0 | 1 | 0 | +30 |
| 0 | 0 | 0 | 0 | 1 | 1 | +29 |
| 0 | 0 | 0 | 1 | 0 | 0 | +28 |
| 0 | 0 | 0 | 1 | 0 | 1 | +27 |
| 0 | 0 | 0 | 1 | 1 | 0 | +26 |
| 0 | 0 | 0 | 1 | 1 | 1 | +25 |
| 0 | 0 | 1 | 0 | 0 | 0 | +24 |
| 0 | 0 | 1 | 0 | 0 | 1 | +23 |
| 0 | 0 | 1 | 0 | 1 | 0 | +22 |
| 0 | 0 | 1 | 0 | 1 | 1 | +21 |

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## TABLE 12. IATRO TRIMMING RANGE (Continued)

| IATR05 | IATR04 | IATR03 | IATR02 | IATR01 | IATR00 | TRIMMING RANGE |
|--------|--------|--------|--------|--------|--------|----------------|
| 0 | 0 | 1 | 1 | 0 | 0 | +20 |
| 0 | 0 | 1 | 1 | 0 | 1 | +19 |
| 0 | 0 | 1 | 1 | 1 | 0 | +18 |
| 0 | 0 | 1 | 1 | 1 | 1 | +17 |
| 0 | 1 | 0 | 0 | 0 | 0 | +16 |
| 0 | 1 | 0 | 0 | 0 | 1 | +15 |
| 0 | 1 | 0 | 0 | 1 | 0 | +14 |
| 0 | 1 | 0 | 0 | 1 | 1 | +13 |
| 0 | 1 | 0 | 1 | 0 | 0 | +12 |
| 0 | 1 | 0 | 1 | 0 | 1 | +11 |
| 0 | 1 | 0 | 1 | 1 | 0 | +10 |
| 0 | 1 | 0 | 1 | 1 | 1 | +9 |
| 0 | 1 | 1 | 0 | 0 | 0 | +8 |
| 0 | 1 | 1 | 0 | 0 | 1 | +7 |
| 0 | 1 | 1 | 0 | 1 | 0 | +6 |
| 0 | 1 | 1 | 0 | 1 | 1 | +5 |
| 0 | 1 | 1 | 1 | 0 | 0 | +4 |
| 0 | 1 | 1 | 1 | 0 | 1 | +3 |
| 0 | 1 | 1 | 1 | 1 | 0 | +2 |
| 0 | 1 | 1 | 1 | 1 | 1 | +1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | -1 |
| 1 | 0 | 0 | 0 | 1 | 0 | -2 |
| 1 | 0 | 0 | 0 | 1 | 1 | -3 |
| 1 | 0 | 0 | 1 | 0 | 0 | -4 |
| 1 | 0 | 0 | 1 | 0 | 1 | -5 |
| 1 | 0 | 0 | 1 | 1 | 0 | -6 |
| 1 | 0 | 0 | 1 | 1 | 1 | -7 |
| 1 | 0 | 1 | 0 | 0 | 0 | -8 |
| 1 | 0 | 1 | 0 | 0 | 1 | -9 |
| 1 | 0 | 1 | 0 | 1 | 0 | -10 |
| 1 | 0 | 1 | 0 | 1 | 1 | -11 |
| 1 | 0 | 1 | 1 | 0 | 0 | -12 |
| 1 | 0 | 1 | 1 | 0 | 1 | -13 |
| 1 | 0 | 1 | 1 | 1 | 0 | -14 |
| 1 | 0 | 1 | 1 | 1 | 1 | -15 |
| 1 | 1 | 0 | 0 | 0 | 0 | -16 |
| 1 | 1 | 0 | 0 | 0 | 1 | -17 |
| 1 | 1 | 0 | 0 | 1 | 0 | -18 |
| 1 | 1 | 0 | 0 | 1 | 1 | -19 |
| 1 | 1 | 0 | 1 | 0 | 0 | -20 |
| 1 | 1 | 0 | 1 | 0 | 1 | -21 |
| 1 | 1 | 0 | 1 | 1 | 0 | -22 |
| 1 | 1 | 0 | 1 | 1 | 1 | -23 |
| 1 | 1 | 1 | 0 | 0 | 0 | -24 |
| 1 | 1 | 1 | 0 | 0 | 1 | -25 |
| 1 | 1 | 1 | 0 | 1 | 0 | -26 |
| 1 | 1 | 1 | 0 | 1 | 1 | -27 |
| 1 | 1 | 1 | 1 | 0 | 0 | -28 |
| 1 | 1 | 1 | 1 | 0 | 1 | -29 |
| 1 | 1 | 1 | 1 | 1 | 0 | -30 |
| 1 | 1 | 1 | 1 | 1 | 1 | -31 |

## ALPHA Register (ALPHA)

### TABLE 13. ALPHA REGISTER

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| 0Ch | 0 | ALPHA6 | ALPHA5 | ALPHA4 | ALPHA3 | ALPHA2 | ALPHA1 | ALPHA0 |

The Alpha variable is 7 bits and is defined as the temperature coefficient of Crystal, normally given in units of ppm/°C$^2$ = and with a typical value of -0.034. The ISL12020 devices use a scaled version of the absolute value of this coefficient in order to get an integer value. Therefore, Alpha <6:0> is defined as the (|Actual Alpha Value| x 1024) and converted to binary. For example, a crystal with Alpha of -0.034ppm/°C$^2$ is first scaled:

|1024*(-0.034)| = 35d and then converted to a binary number of 0100011b.

The practical range of Actual Alpha values is from -0.020 to -0.060.

The ALPHA register should only be changed while the TSE (Temp Sense Enable) bit is "0".

## BETA Register (BETA)

### TABLE 14.

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|
| 0Dh | TSE | BTSE | BTSR | 0 | BETA3 | BETA2 | BETA1 | BETA0 |

### TEMPERATURE SENSOR ENABLED BIT (TSE)

This bit enables the Temperature Sensing operation, including the temperature sensor, A/D converter and ATR/DTR register adjustment. The default mode after power up is disabled (TSE = 0). To enable the operation, TSE should be set to 1 (TSE = 1). When temp sense is disabled, the initial values for IATR and IDTR registers are used for frequency control.

All changes to the IDTR, IATR, ALPHA and BETA registers must be made with TSE = 0. After loading the new values, then TSE can be enabled and the new values are used.

### TEMP SENSOR CONVERSION IN BATTERY MODE BIT (BTSE)

This bit enables the Temperature Sensing and Correction in battery mode. BTSE = 0 defualt no conversion in battery mode. BTSE = 1 Temp Sensing enabled in battery mode. The BTSE is disabled when battery voltage is lower than 2.6V.

### FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT (BTSR)

This bit controls the frequency of Temp Sensing and Correction. BTSR = 0 default mode is every 10 minutes, BTSR = 1 is every 1.0 minute. Note that BTSE has to be enabled in both cases. See Table 15.

### TABLE 15. FREQUENCY OF TEMPERATURE SENSING AND CORRECTION BIT

| BTSE | BTSR | TC PERIOD IN BATTERY MODE |
|---|---|---|
| 0 | 0 | OFF |
| 0 | 1 | OFF |
| 1 | 0 | 10 Minutes |
| 1 | 1 | 1 Minute |

### GAIN FACTOR OF ATR BIT (BETA)<3:0>

Beta is specified to take care of the Cm variations of the crystal. Most crystals specify Cm around 2.2fF. For example, if Cm > 2.2fF, the actual ATR steps may reduce from 1ppm/step to approximately 0.80ppm/step. Beta is then used to adjust for this variation and restore the step size to 1ppm/step.

The value for BETA should only be changed while the TSE (Temp Sense Enable) bit is "0". The procedure for writing the BETA register involves two steps. First, Write the new value of BETA with TSE = 0. Then Write the same value of BETA with TSE = 1. This will insure the next temp sense cycle will use the new BETA value. BETA values are limited in the range from 0100 to 1100 as shown in Table 16.

### TABLE 16. BETA VALUES

| BETA<3:0> | ATR STEP ADJUSTMENT |
|---|---|
| 0100 | 0.500 |
| 0101 | 0.625 |
| 0110 | 0.750 |
| 0111 | 0.875 |
| 1000 | 1.00 |
| 1001 | 1.125 |
| 1010 | 1.250 |
| 1011 | 1.375 |
| 1100 | 1.500 |

## Final Analog Trimming Register (FATR)

This register shows the final setting of ATR after temperature correction. It is read-only, the user cannot overwrite a value to this register. This value is accessible as a means of monitoring the temperature compensation function. See Table 17.

### TABLE 17. FINAL ANALOG TRIMMING REGISTER

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Eh | 0 | 0 | FATR5 | FATR4 | FATR3 | FATR2 | FATR1 | FATR0 |

## Final Digital Trimming Register (FDTR)

This Register shows the final setting of DTR after temperature correction. It is read-only, the user cannot overwrite a value to this register. The value is accessible as a means of monitoring the temperature compensation function. The corresponding clock adjustment values are shown in Table 19. The DTR setting is only positive as it is used to correct for the negative drift of a normal crystal over temperature.

### TABLE 18. FINAL DIGITAL TRIMMING REGISTER

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Fh | | | | | | FDTR2 | FDTR1 | FDTR0 |

### TABLE 19. CLOCK ADJUSTMENT VALUES FOR FINAL DIGITAL TRIMMING REGISTER

| DTR<2:0> | DECIMAL | ppm ADJUSTMENT |
|---|---|---|
| 000 | 0 | 0 |
| 001 | 1 | 32 |
| 010 | 2 | 64 |
| 011 | 3 | 96 |
| 100 | 4 | 128 |
| 101 | 5 | 160 |
| 110 | 6 | 196 |
| 111 | 7 | -32 |

## ALARM Registers (10h to 15h)

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = "1"). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

- **Single Event Mode** is enabled by setting the bit 7 on any of the Alarm registers (ESCA0... EDWA0) to "1", the IM bit to "0", and disabling the frequency output. This mode permits a one-time match between the Alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to "1" and the IRQ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.

- **Interrupt Mode** is enabled by setting the bit 7 on any of the Alarm registers (ESCA0... EDWA0) to "1", the IM bit to

"1", and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time. This mode is convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading.

To clear a single event alarm, the ALM bit in the status register must be set to "0" with a write. Note that if the ARST bit is set to 1 (address 08h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

### Example 1

• Alarm set with single interrupt (IM = "0")

• A single alarm will occur on January 1 at 11:30am.

• Set Alarm registers as follows:

| ALARM REGISTER | BIT | | | | | | | | HEX | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| SCA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Seconds disabled |
| MNA0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h | Minutes set to 30, enabled |
| HRA0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91h | Hours set to 11, enabled |
| DTA0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81h | Date set to 1, enabled |
| MOA0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81h | Month set to 1, enabled |
| DWA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Day of week disabled |

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the ALM bit in the status register to "1" and also bringing the $\overline{IRQ}$ output low.

### Example 2

• Pulsed interrupt once per minute (IM = "1")

• Interrupts at one minute intervals when the seconds register is at 30 seconds.

• Set Alarm registers as follows:

| ALARM REGISTER | BIT | | | | | | | | HEX | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| SCA0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h | Seconds set to 30, enabled |
| MNA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Minutes disabled |
| HRA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Hours disabled |
| DTA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Date disabled |

| ALARM REGISTER | BIT | | | | | | | | HEX | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| MOA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Month disabled |
| DWA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Day of week disabled |

Once the registers are set, the following waveform will be seen at IRQ:

RTC AND ALARM REGISTERS ARE BOTH "30s"



60s
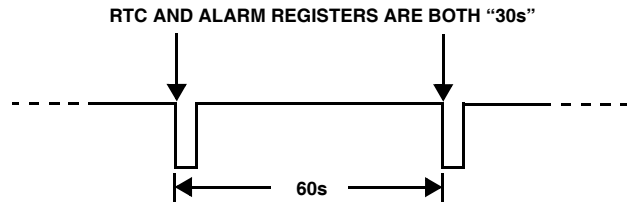
FIGURE 5. IRQ WAVEFORM

Note that the status register ALM bit will be set each time the alarm is triggered, but does not need to be read or cleared

### Time Stamp $V_{DD}$ to Battery Registers (TSV2B)

The TSV2B Register bytes are identical to the RTC register bytes, except they do not extend beyond the Month. The Time Stamp captures the FIRST $V_{DD}$ to Battery Voltage transition time, and will not update upon subsequent events, until cleared (only the first event is captured before clearing). Set CLRTS = 1 to clear this register (Add 09h, PWR_$V_{DD}$ register).

Note that the time stamp registers are cleared to all "0", including the month and day, which is different from the RTC and alarm registers (those registers default to 01h). This is the indicator that no time stamping has occurred since the last clear or initial powerup. Once a time stamp occurs, there will be a non-zero time stamp.

### Time Stamp Battery to $V_{DD}$ Registers (TSB2V)

The Time Stamp Battery to $V_{DD}$ Register bytes are identical to the RTC register bytes, except they do not extend beyond Month. The Time Stamp captures the LAST transition of $V_{BAT}$ to $V_D$ (only the last event of a series of power up/down events is retained). Set CLRTS = 1 to clear this register (Add 09h, PWR_$V_{DD}$ register).
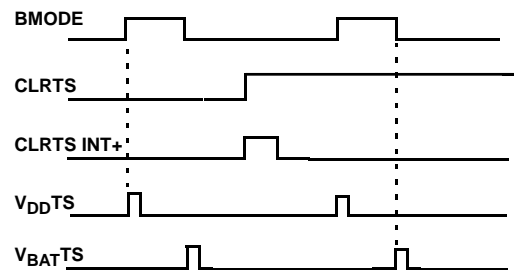


FIGURE 6.

### DST Control Registers (DSTCR)

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning time is controlled by the registers DstMoFd, DstDwFd, DstDtFd

and DstHrFd. DST ending time is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

The following tables describe the structure and functions of the DSTCR.

**DST FORWARD REGISTERS (20H TO 23H)**

DSTE is the DST Enabling Bit located in bit 7 of register 20h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time (including battery), the DSTE bit defaults to "0".

The beginning of DST is controlled by the following DST Registers.

DstMoFd sets the Month that DST starts. The default value for the DST begin month is April (04h).

DstDw sets the Day of the Week that DST starts. DstDwFdE sets the priority of the Day of the Week over the Date. For DstDwFdE=1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers.

The default for the DST Forward Day of the Week is Sunday (80h).

DstDtfd control which Date DST begins. The defaulted value for DST date is on the first date of the month. DstDtFd is only effective if DstDwFdE = 0.

DstHrFd controls the hour that DST begins. It includes the MIL bit which is in the corresponding RTC register. These

two registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value for DST hour is 2:00AM. The time is advanced from 2:00:00AM to 3:00:00AM for this setting.

**DST REVERSE REGISTERS (24H TO 27H)**

The end of DST is controlled by the following DST Registers.

DstMoRv sets the Month that DST ends. The default value for the DST end month is October (10h).

DstDwRv controls which count of the Day of the Week that DST should end. DstDwRvE sets the priority of the Day of the Week over the Date. For DstDwRvE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers.

The default for DST end is Sunday (80h).

DstDtRv controls which Date DST ends. The default value DST is set to end is the first date of the month. The DstDtRv is only effective if the DstDwRvE = 0.

DstHrRv controls the hour that DST ends. It includes the MIL bit which is in the corresponding RTC register. These two registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value sets the DST end at 2:00AM. The time is set back from 2:00:00AM to 1:00:00AM for this setting.

**TABLE 20. DST FORWARD REGISTERS**

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **DstMoFd** | DSTE | Not Used | Not Used | DstMoFd20 | DstMoFd13 | DstMoFd12 | DstMoFd11 | DstMoFd10 |
| **DstDwFd** | DstDwFdE | Not Used | Not Used | Not Used | Not Used | DstDwFd12 | DstDwFd11 | DstDwFd10 |
| **DstDtFd** | Not Used | Not Used | DstDtFd21 | DstDtFd20 | DstDtFd13 | DstDtFd12 | DstDtFd11 | DstDtFd10 |
| **DstHrFd** | MIL | Not Used | DstHrFd21 | DstHrFd20 | DstHrFd13 | DstHrFd12 | DstHrFd11 | DstHrFd10 |

**TABLE 21. DST REVERSE REGISTERS**

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **DstMoRv** | Not Used | Not Used | Not Used | DstMoRv20 | **DstMoRv1**3 | **DstMoRv1**2 | **DstMoRv1**1 | **DstMoRv1**0 |
| **DstDwRv** | DstDwRvE | Not Used | Not Used | Not Used | Not Used | DstDwRv12 | DstDwRv11 | DstDwRv10 |
| **DstDtRv** | Not Used | Not Used | **DstDtRv**21 | **DstDtRv**20 | **DstDtRv1**3 | **DstDtRv1**2 | **DstDtRv1**1 | **DstDtRv1**0 |
| **DstHrRv** | MIL | Not Used | **DstHrRv**21 | DstHrRv20 | **DstHrRv1**3 | **DstHrRv1**2 | **DstHrRv1**1 | **DstHrRv1**0 |

# ISL12020

### TEMP Registers (TEMP)

The temperature sensor produces an analog voltage output and is input to an A/D converter which outputs a 10-bit temperature value in degrees Kelvin. The output is coded to produce greater resolution for the temperature control. TK07:00 are the LSBs of the code, and TK09:08 are the MSBs of the code. The output code can be converted to degrees Centigrade by first converting from binary to decimal and then subtracting 369d.

Temperature in °C = [(TK <9:0>)/2] - 369     (EQ. 1)

The practical range for the temp sensor register output is from 658d to 908d, or -40°C to +85°C.

The TSE bit must be set to "1" to enable temperature sensing.

**TABLE 22.**

|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TK0L | TK07 | TK06 | TK05 | TK04 | TK03 | TK02 | TK01 | TK00 |
| TK0M | 0 | 0 | 0 | 0 | 0 | 0 | TK09 | TK08 |

## User Registers (accessed by using Slave Address 1010111x)

### Addresses [00h to 7Fh]

These registers are 128 bytes of battery-backed user SRAM.

## I²C Serial Interface

The ISL12020 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12020 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

### Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 7). On power up of the ISL12020, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12020 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 7). A START condition is ignored during the power-up sequence.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 7). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 8).

The ISL12020 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12020 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.
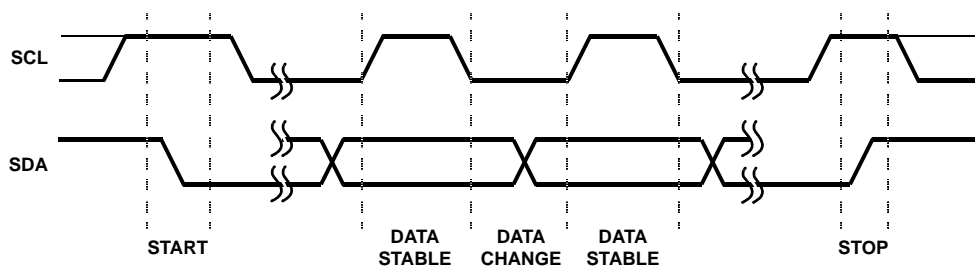


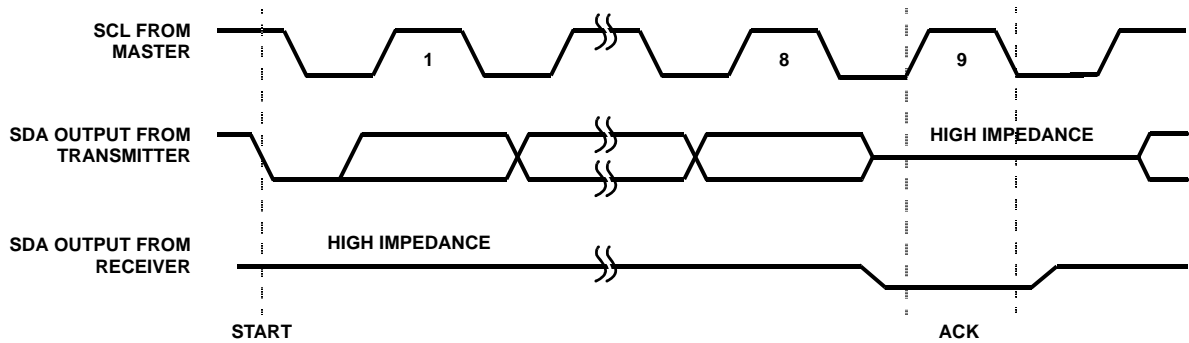**FIGURE 7. VALID DATA CHANGES, START AND STOP CONDITIONS**

*intersil*
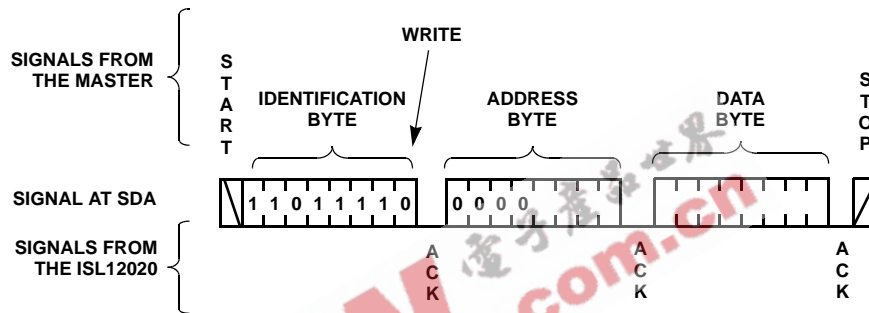
**FIGURE 8. ACKNOWLEDGE RESPONSE FROM RECEIVER**



**FIGURE 9. BYTE WRITE SEQUENCE (SLAVE ADDRESS FOR CSR SHOWN)**

## Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are "1101111" for the RTC registers and "1010111" for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{\text{W}}$ bit is a "1", then a read operation is selected. A "0" selects a write operation (refer to Figure 10).

After loading the entire Slave Address Byte from the SDA bus, the ISL12020 compares the device identifier and device select bits with "1101111" or "1010111". Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 12.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Control/Status Registers, the slave byte must be "1101111x" in both places.
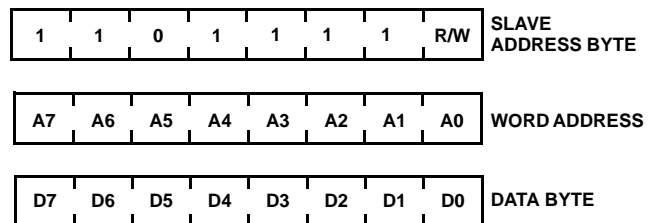


**FIGURE 10. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES**

## Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12020 responds with an ACK. At this time, the I$^2$C interface enters a standby state.

## Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 12). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{\text{W}}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{\text{W}}$ bit set to "1". After each of the three bytes, the ISL12020 responds with an ACK. Then

the ISL12020 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 12).

The Data Bytes are from the memory location indicated by an internal pointer. This pointers initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 13h, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

**TABLE 23. SUGGESTED SURFACE MOUNT CRYSTALS**

| MANUFACTURER | PART NUMBER |
|---|---|
| Citizen | CM200S |
| Epson | MC-405, MC-406 |
| Raltron | RSM-200S |
| SaRonix | 32S12 |
| Ecliptek | ECPSM29T-32.768K |
| ECS | ECX-306 |
| Fox | FSM-327 |

## *Application Section*

### *Battery Backup Details*

Note that any input signal conditioning circuitry that is added in regular operation or battery backup should have minimum supply current drain, or have the capability to be put in a low power standby mode. Op Amps such as the EL8176 have low normal supply current (50µA) and standby power drain (3µA), so can be used in battery backup applications.

### *Oscillator Crystal Requirements*

The ISL12020 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 23 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12020 if their specifications are very similar to the devices listed.

The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

### *Layout Considerations*

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 11 shows a suggested layout for the ISL12020 device using a surface mount crystal. Two main precautions should be followed:

- Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.

- Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.
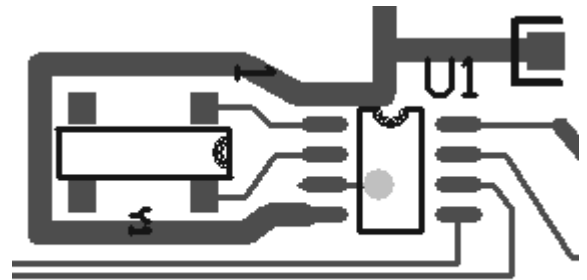


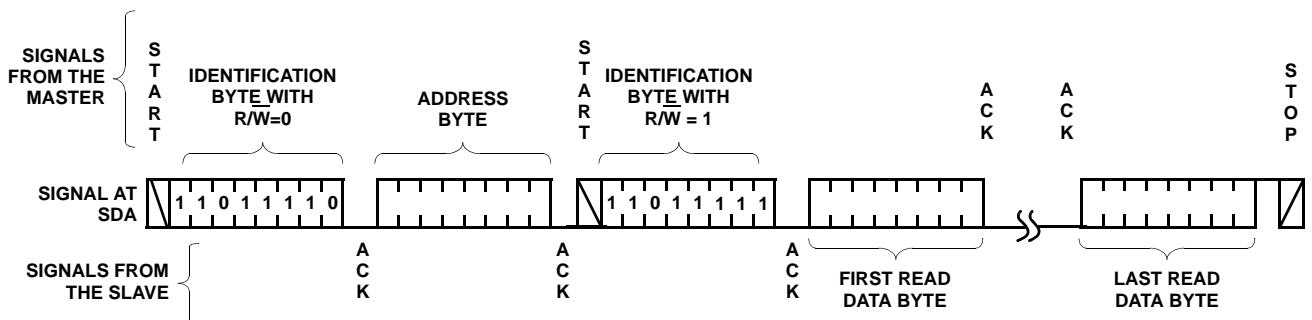**FIGURE 11. SUGGESTED LAYOUT FOR ISL12020 AND CRYSTAL**



**FIGURE 12. READ SEQUENCE (CSR SLAVE ADDRESS SHOWN)**

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the ~IRQ/F$_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the VBAT and VDD pins can be treated as a ground, and should be routed around the crystal.

### Super Capacitor Backup

The ISL12020 device provides a VBAT pin which is used for a battery backup input. A Super Capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL12020 is extremely low, it is possible to get months of backup operation using a Super Capacitor. Typical capacitor values are a few µF to 1F or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity Super Capacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a Super Capacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Following are some examples with equations to assist with calculating backup times and required capacitance for the ISL12020 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

### *Example 1. Calculating Backup Time Given Voltages and Capacitor Value*

In Figure 13, use C$_{BAT}$ = 0.47F and V$_{DD}$ = 5.0V. With V$_{DD}$ = 5.0V, the voltage at V$_{BAT}$ will approach 4.7V as the diode turns off completely. The ISL12020 is specified to operate down to V$_{BAT}$ = 1.8V. The capacitance charge/discharge equation is used to estimate the total backup time:

$$I = C_{BAT} \cdot dV/dT \qquad \text{(EQ. 2)}$$

Rearranging gives

$$dT = C_{BAT} \cdot dV/I_{TOT} \text{ to solve for backup time.} \qquad \text{(EQ. 3)}$$

C$_{BAT}$ is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I$_{TOT}$ is the total of the supply current of the ISL12020 (I$_{BAT}$) plus the leakage current of the capacitor and the diode, I$_{LKG}$. In these calculations, I$_{LKG}$ is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over +50°C, these leakages will increase and hence reduce backup time.

Note that I$_{BAT}$ changes with V$_{BAT}$ almost linearly. This allows us to make an approximation of I$_{BAT}$, using a value midway between the two endpoints. The typical linear equation for I$_{BAT}$ vs V$_{BAT}$ is:

$$I_{BAT} = 1.031E\text{-}7 \cdot (V_{BAT}) + 1.036E\text{-}7A \qquad \text{(EQ. 4)}$$

Using this equation to solve for the average current given 2 voltage points gives:

$$I_{BATAVG} = 5.155E\text{-}8 \cdot (V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7A \qquad \text{(EQ. 5)}$$

Combining with Equation 3 gives the equation for backup time:

$$t_{BACKUP} = C_{BAT} \cdot (V_{BAT2} - V_{BAT1}) / (I_{BATAVG} + I_{LKG}) \text{ seconds} \qquad \text{(EQ. 6)}$$

where

C$_{BAT}$ = 0.47F

V$_{BAT2}$ = 4.7V

V$_{BAT1}$ = 1.8V

I$_{LKG}$ = 0 (assumed minimal)

Solving Equation 5 for this example, I$_{BATAVG}$ = 4.387E-7A

$$t_{BACKUP} = 0.47 \cdot (2.9)/4.38E\text{-}7 = 3.107E6s$$

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be:

$$C_{BAT} = 0.70 \cdot 35.96 = 25.2 \text{ days} \qquad \text{(EQ. 7)}$$
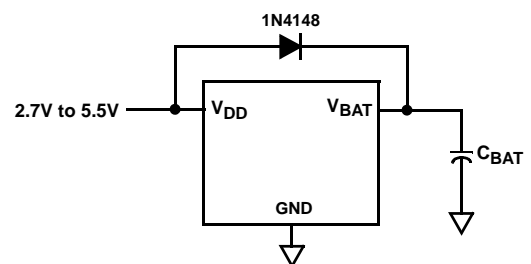


**FIGURE 13. SUPERCAPACITOR CHARGING CIRCUIT**

### *Example 2. Calculating a Capacitor Value for a Given Backup Time*

Referring to Figure 13 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given $V_{DD} = 5.0V$. As in Example 1, the $V_{BAT}$ voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 3 to solve for capacitance:

$$C_{BAT} = dT*I/dV \qquad \text{(EQ. 8)}$$

Using the terms described above, this equation becomes:

$$C_{BAT} = t_{BACKUP}*(I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \qquad \text{(EQ. 9)}$$

where

$t_{BACKUP}$ = 60 days*86, 400s/day = 5.18 E6s

$I_{BATAVG}$ = 4.387 E-7A (same as Example 1)

$I_{LKG}$ = 0 (assumed)

$V_{BAT2}$ = 4.7V

$V_{BAT1}$ = 1.8V

Solving gives

$C_{BAT}$ = 5.18 E6 * (4.387 E-7)/(2.9) = 0.784F

If the 30% tolerance is included for tolerances, then worst case cap value would be:

$C_{BAT}$ = 1.3 *.784 = 1.02F

## Small Outline Plastic Packages (SOIC)



**M8.15** (JEDEC MS-012-AA ISSUE C)
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 6/05
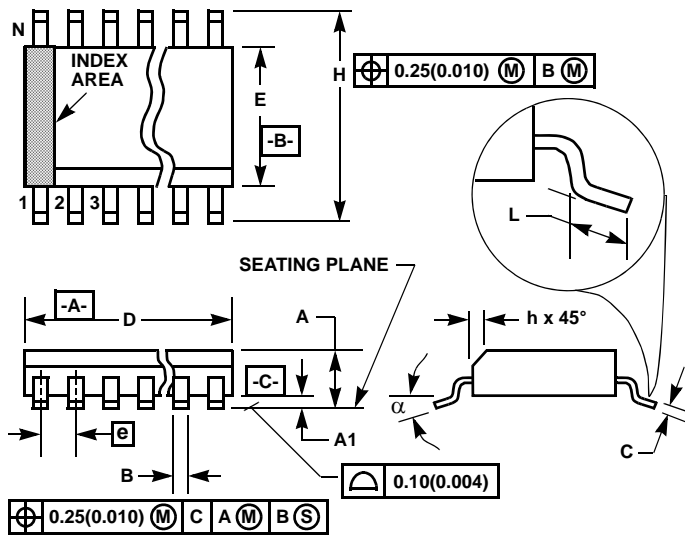
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
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