

**IW4027B**

## Dual JK Flip-Flop

The IW4027B is a Dual JK Flip-Flop which is edge-triggered and features independent Set, Reset, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Reset and Set are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

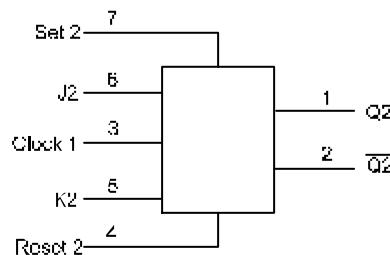
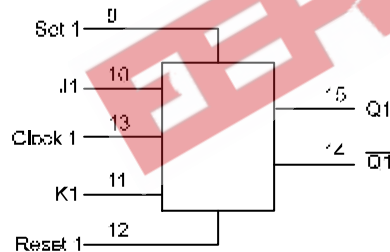
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply

**ORDERING INFORMATION**

IW4027BN	Plastic
IW4027BD	SOIC
IZ4027B	Chip

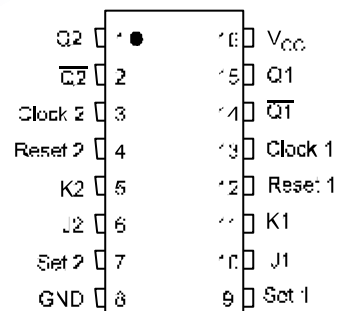
$T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 16 =  $V_{CC}$   
PIN 8 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	$Q_{n+1}$	$\overline{Q}_{n+1}$
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	X	X	X	H	H
L	L	$\downarrow$	L	L	No change	
L	L	$\uparrow$	H	L	H	L
L	L	$\uparrow$	L	H	L	H
L	L	$\uparrow$	H	H	$\overline{Q}_n$	$Q_n$

X = don't care

$Q_{n+1}$  = State After Clock Positive Transition

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP, SOIC Package	500**	mW
P <sub>tot</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*\*Derating: - Plastic DIP from -55 to +100°C  
 - SOIC Package from -55 to +65°C  
 - Plastic DIP: - 10 mW/°C from +100 to +125°C  
 - SOIC Package: - 7 mW/°C from +65 to +125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation V<sub>IN</sub> should be constrained to the range GND ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> =0.5 V or V <sub>CC</sub> - 0.5 V V <sub>OUT</sub> =1.0 V or V <sub>CC</sub> - 1.0 V V <sub>OUT</sub> =1.5 V or V <sub>CC</sub> - 1.5 V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>  V <sub>IL</sub> =1.5V, V <sub>IH</sub> =3.5V, I <sub>O</sub> =-1μA V <sub>IL</sub> =3.0V, V <sub>IH</sub> =7.0V, I <sub>O</sub> =-1μA V <sub>IL</sub> =4.0V, V <sub>IH</sub> =11V, I <sub>O</sub> =-1μA	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
			5.0	4.5	4.5	4.5	
			10	9.0	9.0	9.0	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>  V <sub>IL</sub> =1.5V, V <sub>IH</sub> =3.5V, I <sub>O</sub> =1μA V <sub>IL</sub> =3.0V, V <sub>IH</sub> =7.0V, I <sub>O</sub> =1μA V <sub>IL</sub> =4.0V, V <sub>IH</sub> =11V, I <sub>O</sub> =1μA	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
			5.0	0.5	0.5	0.5	
			10	1.0	1.0	1.0	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
			5.0	1.0	1.0	30	
			10	2.0	2.0	60	
			15	4.0	4.0	120	
			20	20	20	600	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OL</sub> =0.4 V V <sub>OL</sub> =0.5 V V <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
			5.0	-0.64	-0.51	-0.36	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OH</sub> =4.6 V V <sub>OH</sub> =2.5 V V <sub>OH</sub> =9.5 V V <sub>OH</sub> =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	
			5.0	-0.64	-0.51	-0.36	

**AC ELECTRICAL CHARACTERISTICS** ( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$f_{\text{max}}$	Maximum Clock Frequency	5.0	3.5	3.5	1.75	MHz
		10	8	8	4	
		15	12	12	6	
$t_{\text{PLH}}, t_{\text{PHL}}$	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	5.0	300	300	600	ns
		10	130	130	260	
		15	90	90	180	
$t_{\text{PLH}}$	Maximum Propagation Delay, Set to Q or Reset to Q	5.0	300	300	600	ns
		10	130	130	260	
		15	90	90	180	
$t_{\text{PHL}}$	Maximum Propagation Delay, Set to $\overline{Q}$ or Reset to $\overline{Q}$	5.0	400	400	800	ns
		10	170	170	340	
		15	120	120	240	
$t_{\text{TLH}}, t_{\text{THL}}$	Maximum Output Transition Time, Any Output	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$C_{\text{IN}}$	Maximum Input Capacitance	-	-	7.5	-	pF

**TIMING REQUIREMENTS** ( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, Clock	5.0	140	140	280	ns
		10	60	60	120	
		15	40	40	80	
$t_w$	Minimum Pulse Width, Set or Reset	5.0	180	180	360	ns
		10	80	80	160	
		15	50	50	100	
$t_{\text{su}}$	Minimum Data Setup Time	5.0	200	200	400	ns
		10	75	75	150	
		15	50	50	100	
$t_r, t_f$	Maximum Input Rise or Fall Time, Clock	5.0	45	45	90	$\mu\text{s}$
		10	5	5	10	
		15	2	2	4	



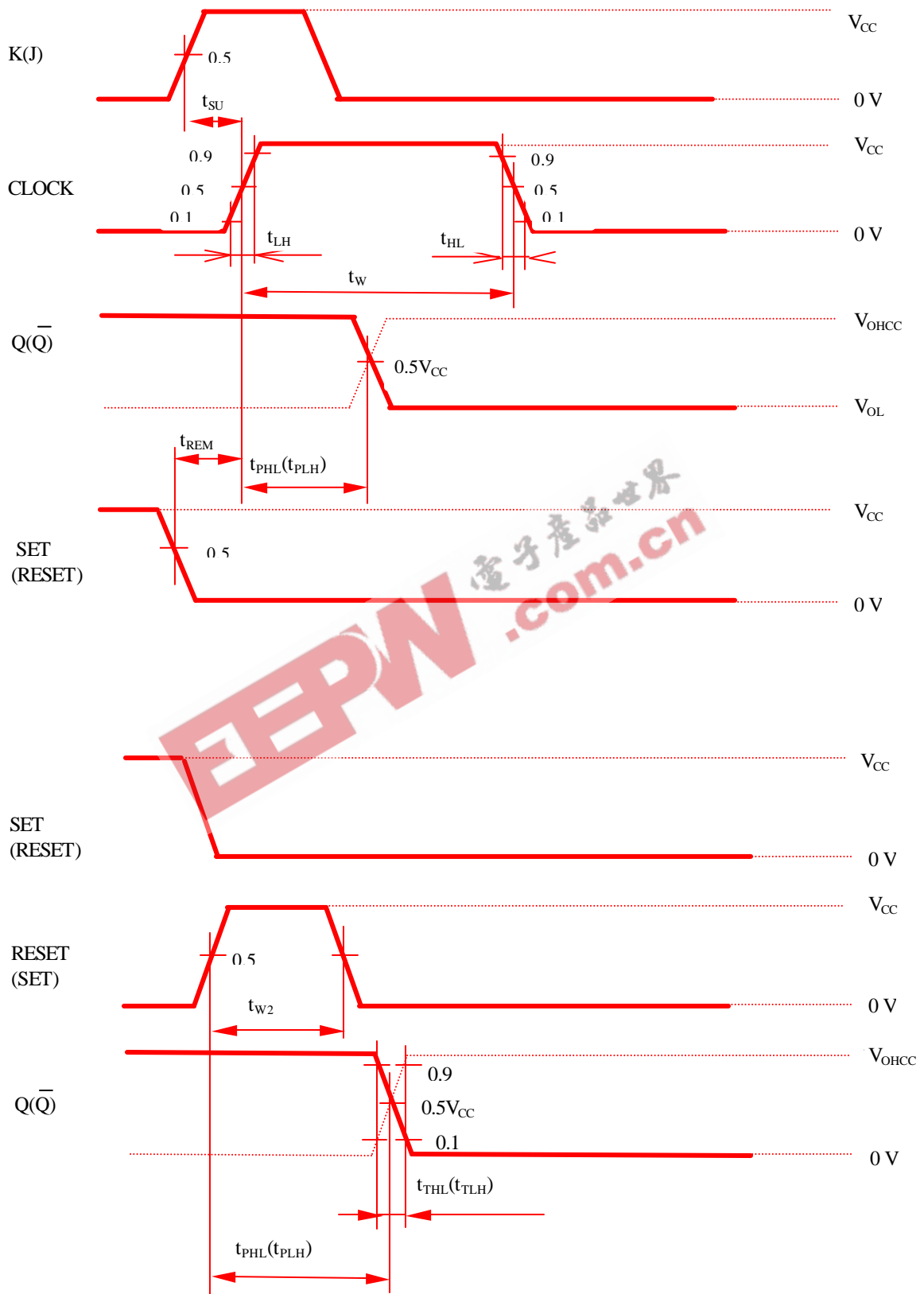
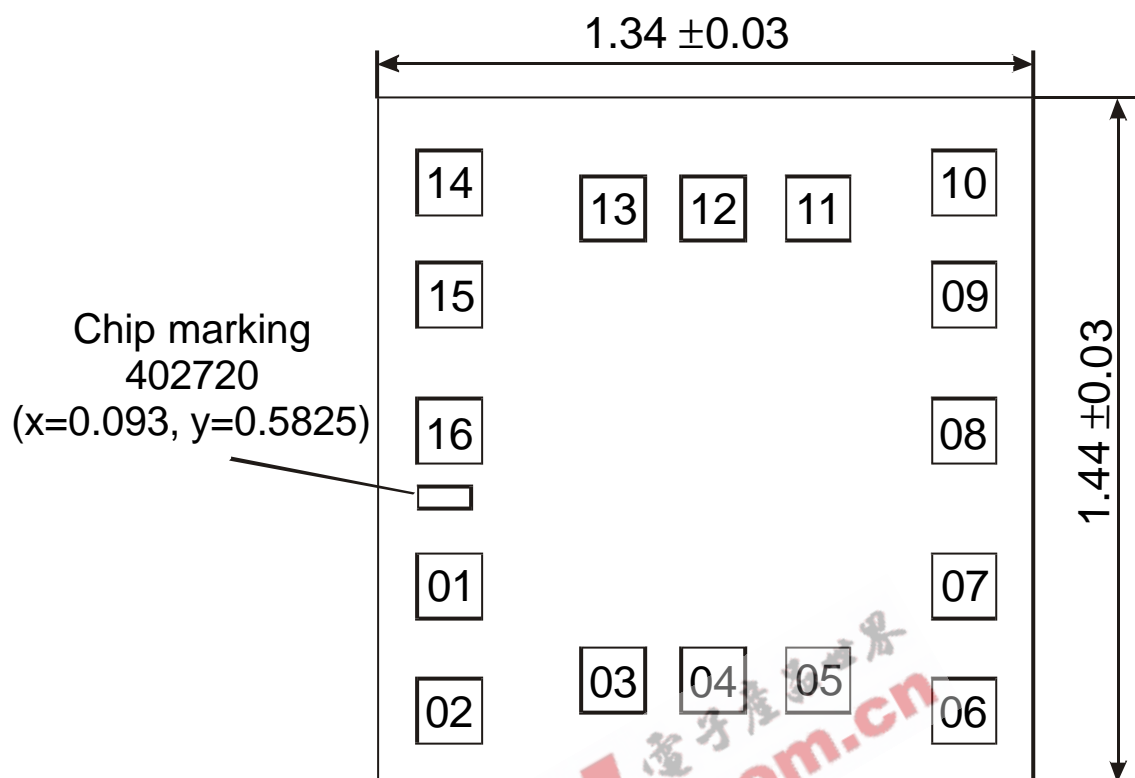


Figure 1. Switching Waveforms



CHIP PAD DIAGRAM IZ4027B

Pad size 0.100 x 0.100 mm (Pad size is given as per passivation layer)

Thickness of chip  $0.46 \pm 0.02$  mm

## PAD LOCATION

Pad No	Symbol	X	Y
01	Q2	0.116	0.4215
02	$\overline{Q2}$	0.111	0.126
03	Clock 2	0.474	0.1755
04	Reset 2	0.6555	0.1755
05	K2	0.8335	0.174
06	J2	1.124	0.1235
07	Set 2	1.124	0.4065
08	GND	1.1245	0.6855
09	Set 1	1.124	0.9335
10	J1	1.124	1.2165
11	K1	0.8335	1.166
12	Reset 1	0.6555	1.1645
13	Clock 1	0.474	1.1645
14	$\overline{Q1}$	0.111	1.214
15	Q1	0.116	0.9185
16	Vcc	0.116	0.7365