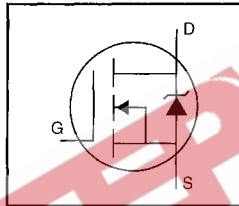


HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS}=4V$  &  $5V$
- 175°C Operating Temperature
- Fast Switching

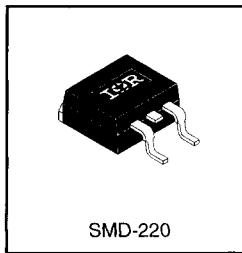


$V_{DSS} = 60V$
$R_{DS(on)} = 0.10\Omega$
$I_D = 17A$

**Description**

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SMD-220 is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The SMD-220 is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



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**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	17	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS}$ @ 5.0 V	12	
$I_{DM}$	Pulsed Drain Current ①	68	W
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	60	
$P_D$ @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	3.7	
	Linear Derating Factor	0.40	W/°C
	Linear Derating Factor (PCB Mount)**	0.025	
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	110	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Thermal Resistance**


	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	2.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	40	
$R_{\theta A}$	Junction-to-Ambient	—	—	62	

\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.


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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.060	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.10	Ω	V <sub>GS</sub> =5.0V, I <sub>D</sub> =10A ④ V <sub>GS</sub> =4.0V, I <sub>D</sub> =8.5A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	7.3	—	—	S	V <sub>DS</sub> =25V, I <sub>D</sub> =10A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =10V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> =-10V
Q <sub>g</sub>	Total Gate Charge	—	—	18	nC	I <sub>D</sub> =17A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.5	nC	V <sub>DS</sub> =48V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	12	nC	V <sub>GS</sub> =5.0V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	11	—	ns	V <sub>DD</sub> =30V I <sub>D</sub> =17A R <sub>G</sub> =9.0Ω R <sub>D</sub> =1.7Ω See Figure 10 ④
t <sub>r</sub>	Rise Time	—	110	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	23	—		
t <sub>f</sub>	Fall Time	—	41	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	870	—	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =25V f=1.0MHz See Figure 5
C <sub>oss</sub>	Output Capacitance	—	360	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	53	—		

## Source-Drain Ratings and Characteristics

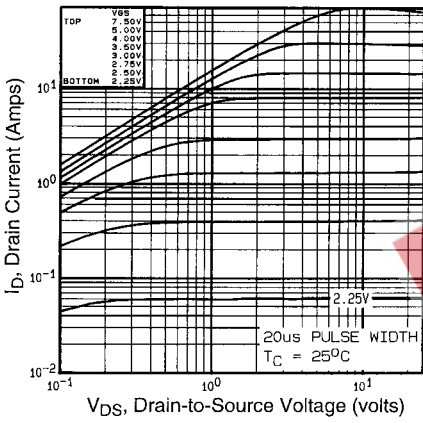
Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	68		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =17A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	110	260	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =17A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.49	1.5	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

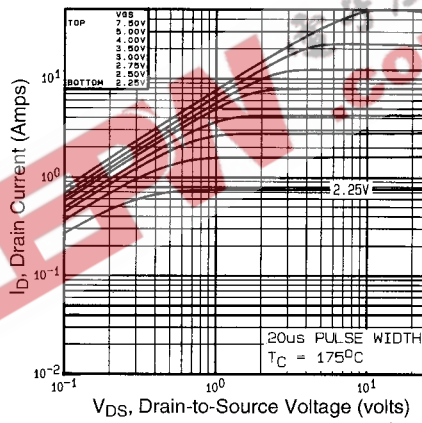
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=25V, starting T<sub>J</sub>=25°C, L=444μH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=17A (See Figure 12)
- ③ I<sub>SD</sub>≤17A, di/dt≤140A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



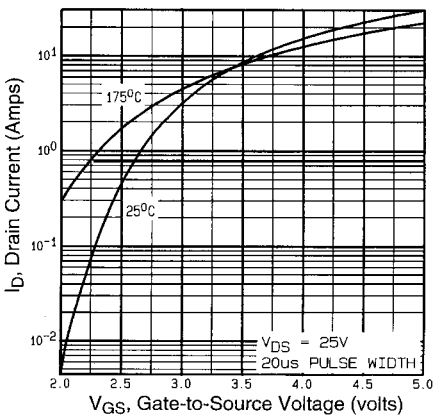
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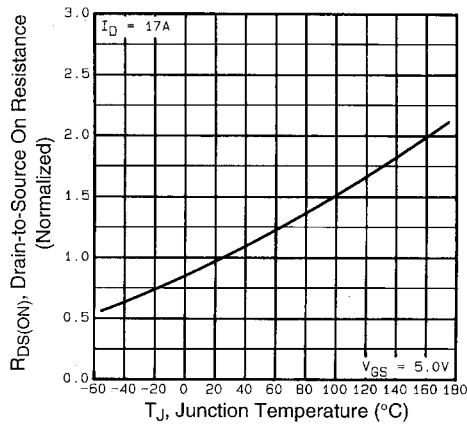
**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  $T_C=175^\circ\text{C}$



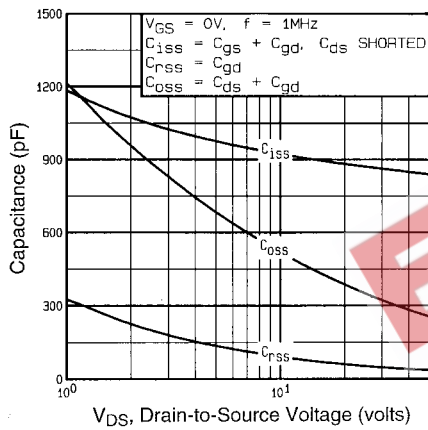
**Fig 3.** Typical Transfer Characteristics



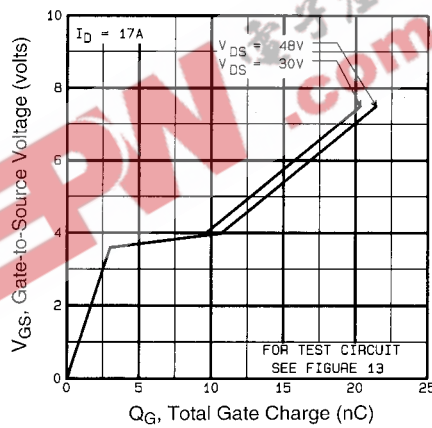
**Fig 4.** Normalized On-Resistance Vs. Temperature

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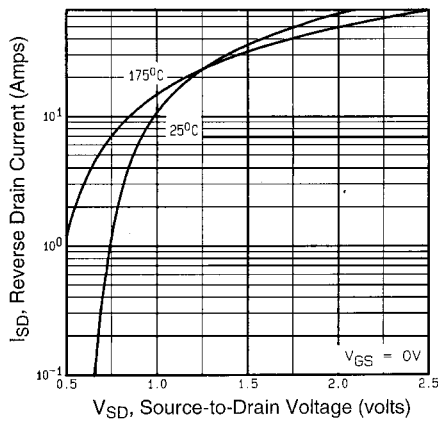
# IRLZ24S



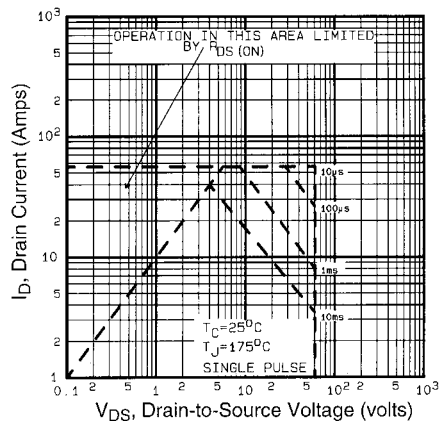
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

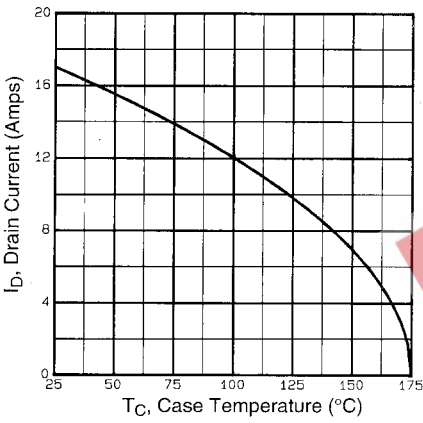


Fig 9. Maximum Drain Current Vs. Case Temperature

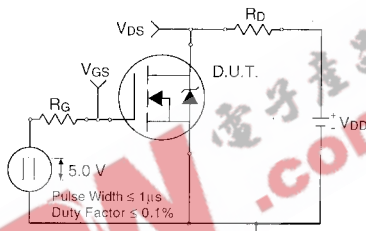


Fig 10a. Switching Time Test Circuit

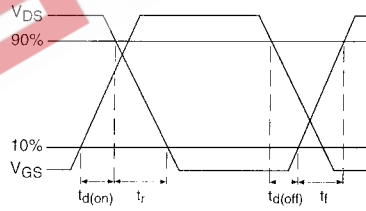


Fig 10b. Switching Time Waveforms

DATA SHEETS

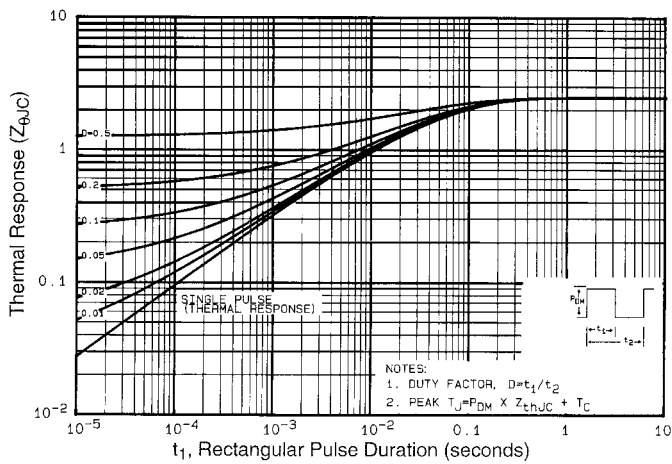


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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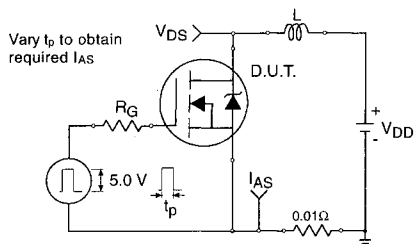


Fig 12a. Unclamped Inductive Test Circuit

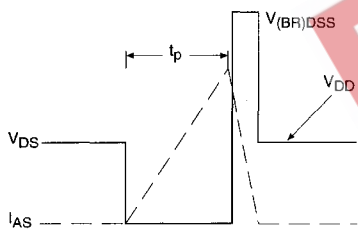


Fig 12b. Unclamped Inductive Waveforms

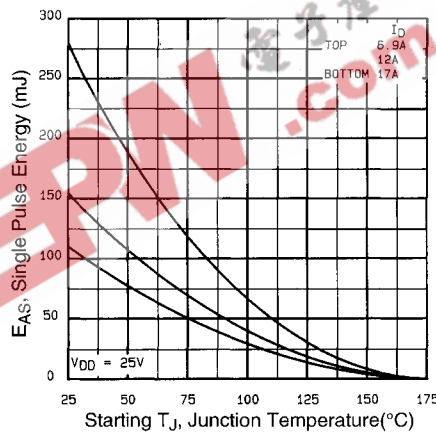


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

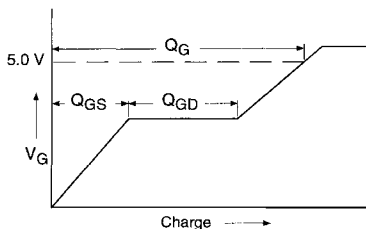


Fig 13a. Basic Gate Charge Waveform

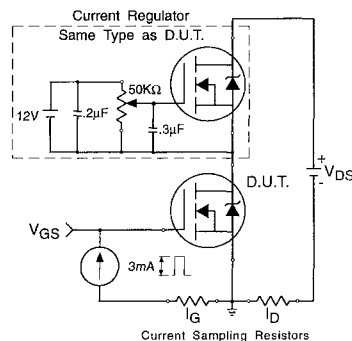


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515

Appendix D: Tape & Reel Information – See page 1519

