

IW4053B

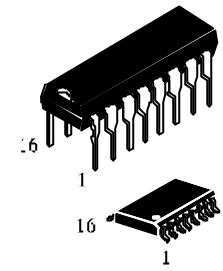
**Analog Multiplexer Demultiplexer
High-Performance Silicon-Gate CMOS**

The IW4053B analog multiplexer/demultiplexer is digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20V (if $V_{CC} - GND = 3V$, a $V_{CC} - V_{EE}$ of up to 13 V can be controlled; for $V_{CC} - V_{EE}$ level differences above 13V a $V_{CC} - GND$ of at least 4.5V is required).

These multiplexer circuits dissipate extremely low quiescent power over the full $V_{CC} - GND$ and $V_{CC} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the ENABLE input terminal all channels are off.

The IW4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an enable input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply



N SUFFIX
PLASTIC

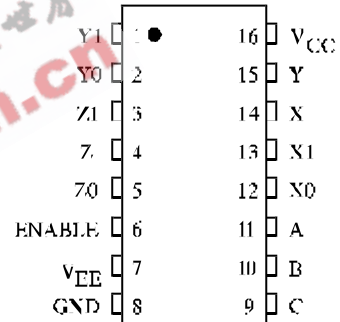
DW SUFFIX
SOIC

ORDERING INFORMATION

IW4053BN Plastic DIP
IW4053BD SOIC
IZ4053B chip

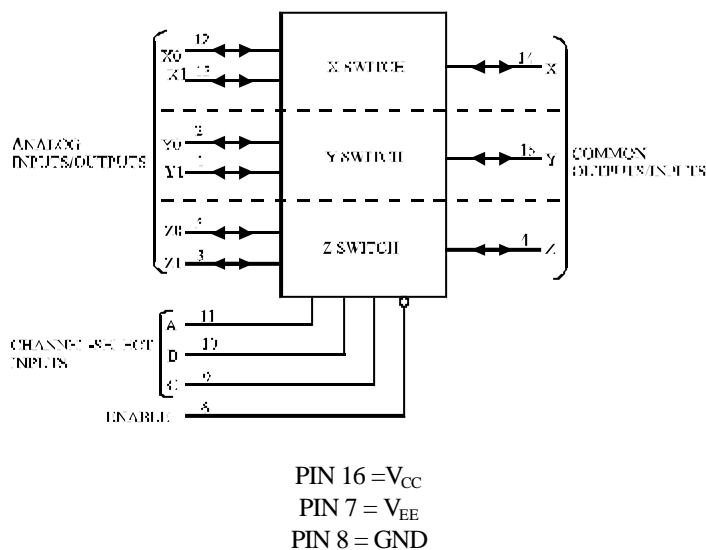
$T_A = -55^\circ$ to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM

Triple Single-Pole, Double-Position
Plus Common Off



FUNCTION TABLE

Control Inputs				ON Channels		
Enable	Select					
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

H = high level
 L = low level
 X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±10	mA
P _D	Power Dissipation in Still Air	500* ¹	mW
P _{tot}	Power Dissipation per Output Transistor	100	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

*¹ - for Plastic DIP from -55° to +100°C, for SO Package from -55° to +65°C.

+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C

SO Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V _{IN}	DC Input Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				³ -55 °C	£ 25 °C	£ 125 °C	
V _{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	V _{IS} =V _{CC} thru 1kΩ V _{EE} =GND=0 I _{IS} <2μA on all OFF Channels R _L =1kΩ to GND	5	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	V _{IS} =V _{CC} thru 1kΩ V _{EE} =GND=0 I _{IS} <2μA on all OFF Channels R _L =1kΩ to GND	5	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
I _{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V _{IN} =V _{CC} or GND V _{EE} =GND=0	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V _{CC} or GND V _{EE} =GND=0	5	5	5	150	μA
			10	10	10	300	
			15	20	20	600	
			20	100	100	3000	

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				³ -55 °C	£ 25 °C	£ 125 °C	
R _{ON}	Maximum "ON" Resistance	V _{EE} =GND=0 V _{IS} = GND to V _{CC}	5	800	1050	1150	Ω
			10	310	400	550	
			15	200	240	320	
ΔR _{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{EE} =GND=0	5	-	10*	-	Ω
			10	-	15*	-	
			15	-	5*	-	
I _{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V _{EE} =GND=0	18	±100	±100	±1000	nA
	Maximum Off- Channel Leakage Current, Common Channel	V _{EE} =GND=0	18	±100	±100	±1000	

* - Typical Value

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=20.0\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\cong -55$ $^{\circ}\text{C}$	$\text{£ } 25$ $^{\circ}\text{C}$	$\text{£ } 125$ $^{\circ}\text{C}$	
$t_{PHL}(t_{PLH})$	Maximum Propagation Delay , Analog Input to Analog Output (Figure 1) $R_L=200\text{k}\Omega$, $V_{EE}=\text{GND}=0$	5	60	60	70	ns
		10	30	30	40	
		15	20	20	30	
$t_{PHL1}(t_{PLH1})$	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 1) $R_L=200\text{ k}\Omega$, $V_{EE}=\text{GND}=0$	5	350	350	400	ns
		10	200	200	250	
		15	160	160	200	
$t_{PZL1}(t_{PZH1})$	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 2) $R_L=10\text{ k}\Omega$ $V_{EE}=\text{GND}=0$	5	720	720	720	ns
		10	320	320	320	
		15	240	240	240	
$t_{PZL2}(t_{PZH2})$	Maximum Propagation Delay , Enable to Analog Output (Figure 2) $R_L=10\text{ k}\Omega$ $V_{EE}=\text{GND}=0$	5	720	720	720	ns
		10	320	320	320	
		15	240	240	240	
$t_{PZL2}(t_{PZH2})$	Maximum Propagation Delay , Enable to Analog Output (Figure 2) $R_L=10\text{ k}\Omega$ $V_{EE}=-5\hat{\text{A}}$, $\text{GND}=0$	5	450	450	450	ns
		10	320	320	320	
		15	240	240	240	
$t_{PLZ1}(t_{PHZ1})$	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 2) $R_L=10\text{ k}\Omega$ $V_{EE}=\text{GND}=0$	5	720	720	720	ns
		10	320	320	320	
		15	240	240	240	
$t_{PLZ1}(t_{PHZ1})$	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 2) $R_L=10\text{ k}\Omega$ $V_{EE}=-5\hat{\text{A}}$, $\text{GND}=0$	5	450	450	450	ns
		10	320	320	320	
		15	240	240	240	
$t_{PLZ2}(t_{PHZ2})$	Maximum Propagation Delay , Enable to Analog Output (Figure 2) $R_L=1,0\text{ k}\Omega$ $V_{EE}=\text{GND}=0$	5	450	450	450	ns
		10	210	210	210	
		15	160	160	160	
$t_{PLZ2}(t_{PHZ2})$	Maximum Propagation Delay , Enable to Analog Output (Figure 2) $R_L=1,0\text{ k}\Omega$ $V_{EE}=-10\hat{\text{A}}$, $\text{GND}=0$	5	300	300	600	ns
		10	210	210	210	
		15	160	160	160	
C_{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs	-	-	7.5	-	pF
$C_{I/O}$	Maximum Capacitance $V_{EE}=\text{GND}=-5\text{V}$ C_{IS} C_{OS} Feedthrough C_{IOS}	5	-	5*	-	pF
		5	-	9*	-	
		5	-	0.2*	-	



ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	V _{IS} ** V	Limits	Unit
					Typical Value	
					25 °C	
B _w	Maximum On-Channel Bandwidth or Minimum Frequency Response (-3db)	V _{EE} =GND=0 R _L =1kΩ 20 log(V _{OS} /V _{IS})=-3db V _{OS} at Common OUT/IN	10	2,5	30	MHz
		V _{OS} at Any Channel	10	2,5	60	
f ₁	(-40db) Feedthrough Frequency (All Channels OFF)	V _{EE} =GND=0 R _L =1kΩ 20 log(V _{OS} /V _{IS})=-40db V _{OS} at Common OUT/IN	10	2,5	8	MHz
		V _{OS} at Any Channel	10	2,5	8	
f ₂	(-40db) Signal Crosstalk Frequency	V _{EE} =GND=0 R _L =1kΩ 20 log(V _{OS} /V _{IS})=-40db Between any 2 Sections : In Pin 2, Out Pin 14 In Pin 15, Out Pin 14	10	2,5	2.5	MHz
			10	2,5	6	
THD	Total Harmonic Distortion	V _{EE} =GND=0 f _{IS} =1kHz sine wave	5	1	0.3	%
			10	1,5	0.2	
			15	2,5	0.12	
V _{AO1}	Address-or Enable to Signal Crosstalk	V _{EE} =GND=0, R _L =10kΩ*** t _r ,t _f =20ns Square Wave	10	-	65	mV (Peak)

** Peak-to-peak voltage symmetrical about (V_{CC}-V_{EE})/2.

*** Both ends of channel.



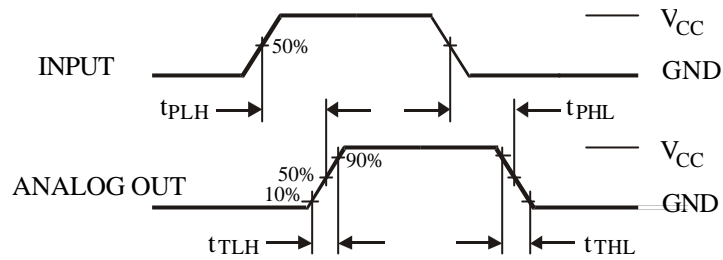


Figure 1. Switching Waveforms

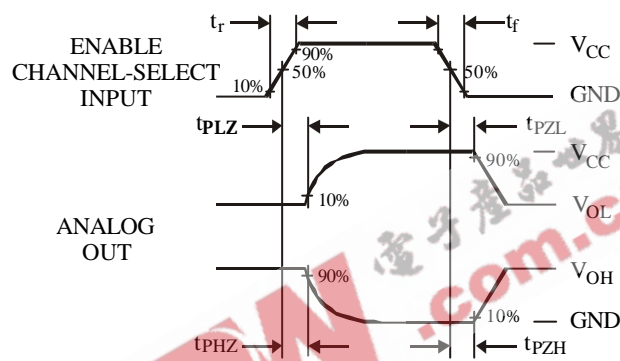
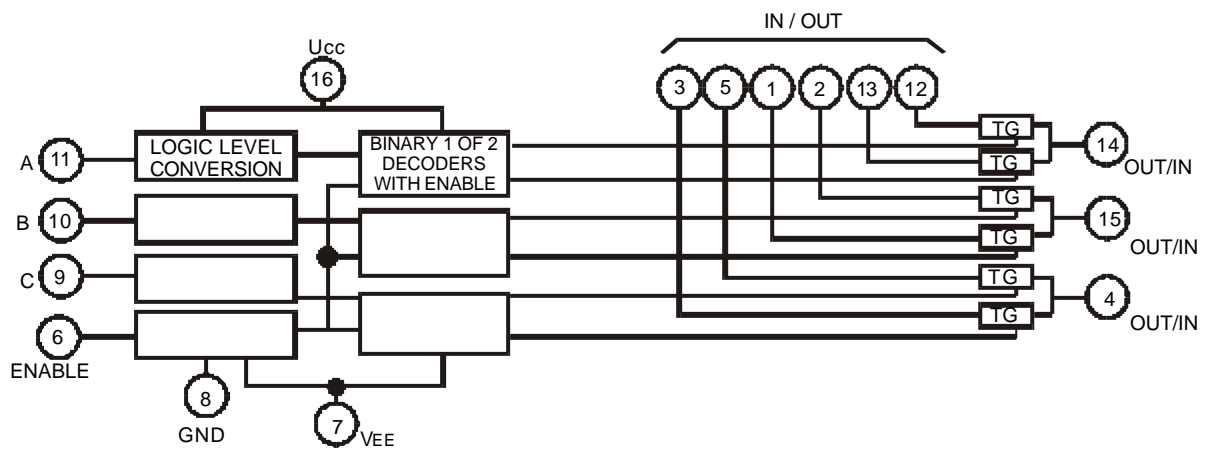
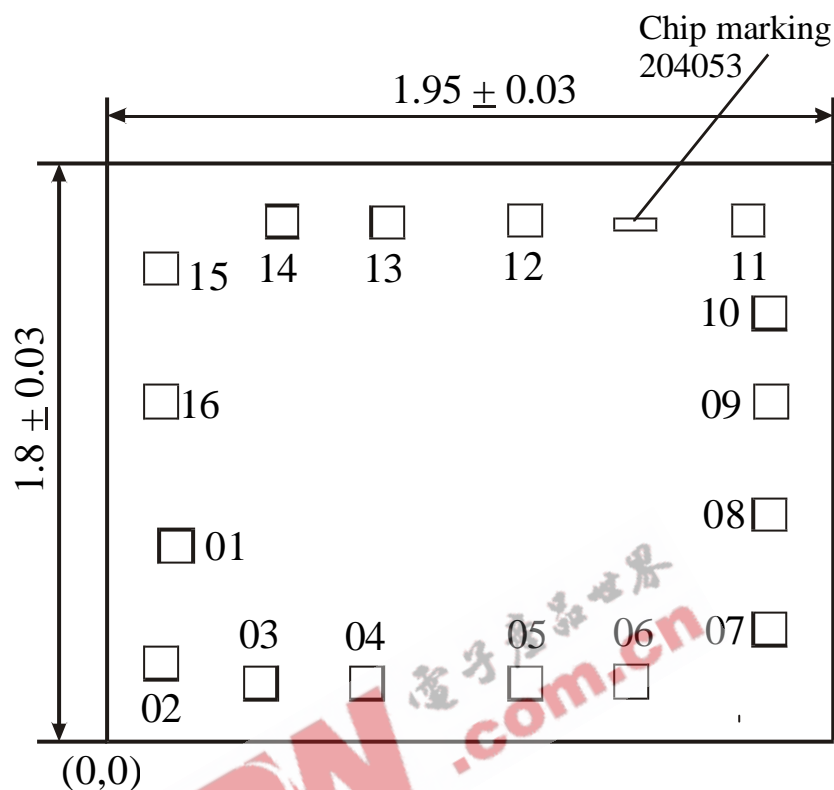


Figure 2. Switching Waveforms

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x=1.361$, $y=1.592$; right higher corner $x=1.423$, $y=1.652$.

Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Pin No	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	01	0.116	0.453	0.100 x 0.100
02	02	0.116	0.175	0.100 x 0.100
03	03	0.362	0.116	0.100 x 0.100
04	04	0.669	0.116	0.100 x 0.100
05	05	1.074	0.116	0.100 x 0.100
06	06	1.287	0.115	0.100 x 0.100
07	07	1.699	0.290	0.100 x 0.100
08	08	1.699	0.620	0.100 x 0.100
09	09	1.699	0.973	0.100 x 0.100
10	10	1.700	1.268	0.100 x 0.100
11	11	1.640	1.583	0.100 x 0.100
12	12	1.063	1.583	0.100 x 0.100
13	13	0.756	1.583	0.100 x 0.100
14	14	0.429	1.583	0.100 x 0.100
15	15	0.116	1.445	0.100 x 0.100
16	16	0.116	0.942	0.100 x 0.100

Note: Pad location is given as per passivation layer