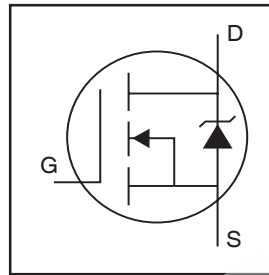


Features

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

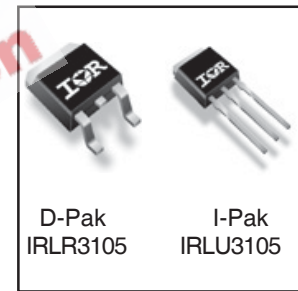


$V_{DSS} = 55V$
$R_{DS(on)} = 0.037\Omega$
$I_D = 25A$

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	25	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	18	
I_{DM}	Pulsed Drain Current ①	100	
$P_D @ T_C = 25^\circ C$	Power Dissipation	57	W
	Linear Derating Factor	0.38	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	61	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value②	94	
I_{AR}	Avalanche Current③	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy③		mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.4	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

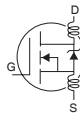
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$	
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	30	37	m Ω	$V_{GS} = 10V, I_D = 15A$ ④	
		—	35	43		$V_{GS} = 5.0V, I_D = 13A$ ④	
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$	
g_{fs}	Forward Transconductance	15	—	—	S	$V_{DS} = 25V, I_D = 15A$ ④	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$	
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$	
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$	
Q_g	Total Gate Charge	—	—	20	nC	$I_D = 15A$	
Q_{gs}	Gate-to-Source Charge	—	—	5.6		$V_{DS} = 44V$	
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	9.0	pF	$V_{GS} = 5.0V$, See Fig. 6 and 13	
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—		$V_{DD} = 28V$	
t_r	Rise Time	—	57	—	nH	$I_D = 15A$	
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 24\Omega$	
t_f	Fall Time	—	37	—	nH	$V_{GS} = 5.0V$, See Fig. 10 ④	
L_D	Internal Drain Inductance	—	4.5	—		Between lead, 6mm (0.25in.) from package and center of die contact	
L_S	Internal Source Inductance ②	—	7.5	—	pF		
C_{iss}	Input Capacitance	—	710	—			$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	150	—			$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	28	—			$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	890	—			$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	110	—			$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ③	—	210	—			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	25	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	100		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 15A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	52	78	ns	$T_J = 25^\circ\text{C}, I_F = 15A, V_{DD} = 28V$
Q_{rr}	Reverse Recovery Charge	—	82	120	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

* When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Notes ① through ④ are on page 11

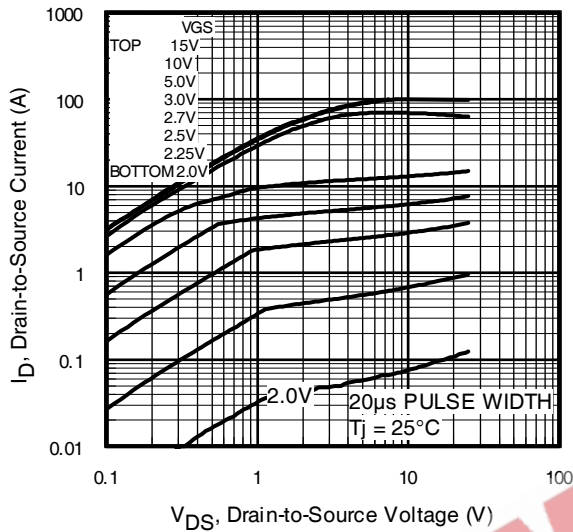


Fig 1. Typical Output Characteristics

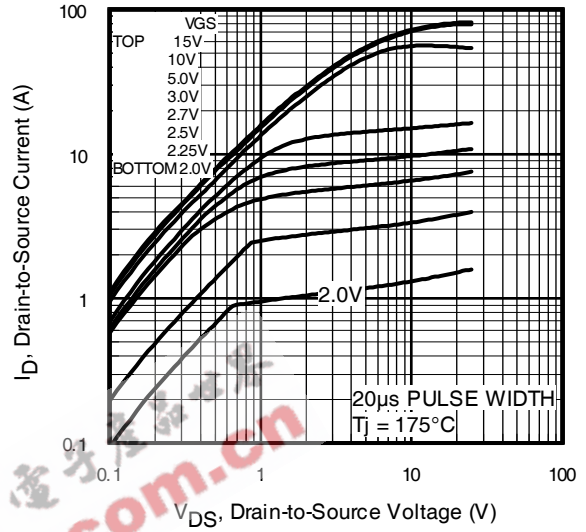


Fig 2. Typical Output Characteristics

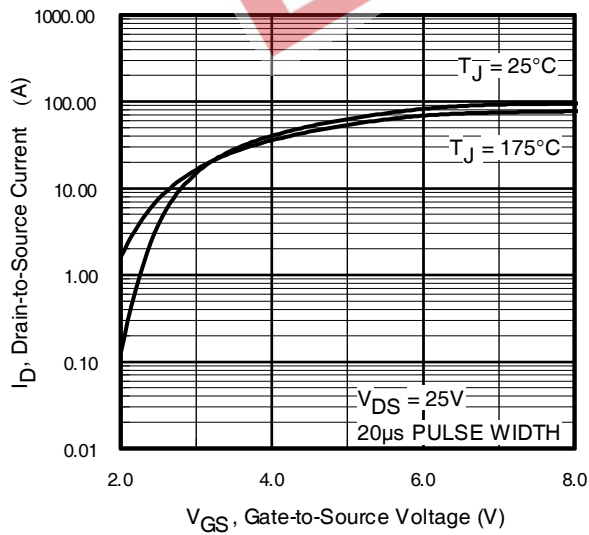


Fig 3. Typical Transfer Characteristics

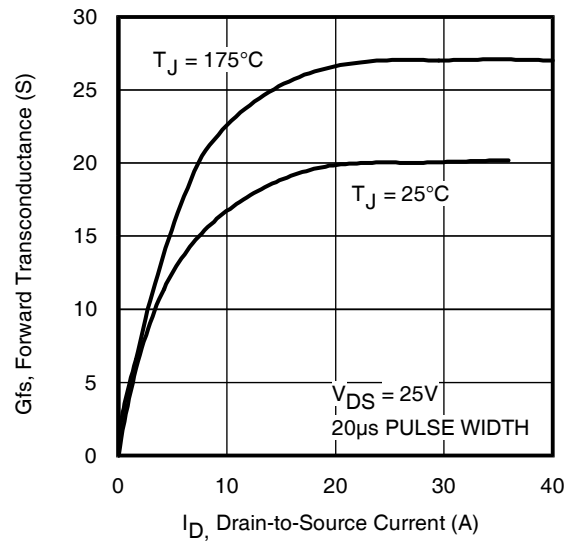


Fig 4. Typical Forward Transconductance Vs. Drain Current

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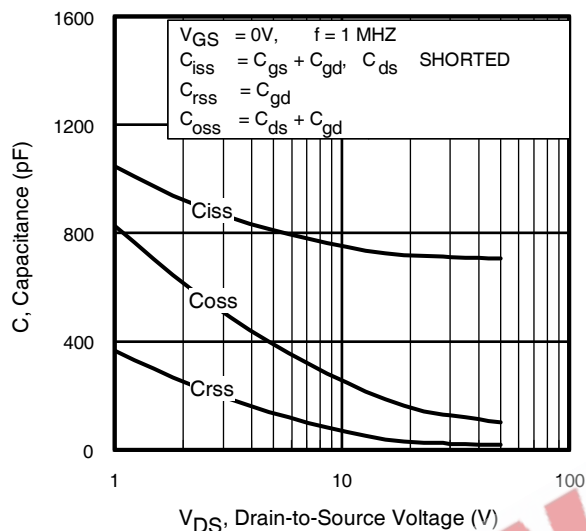


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

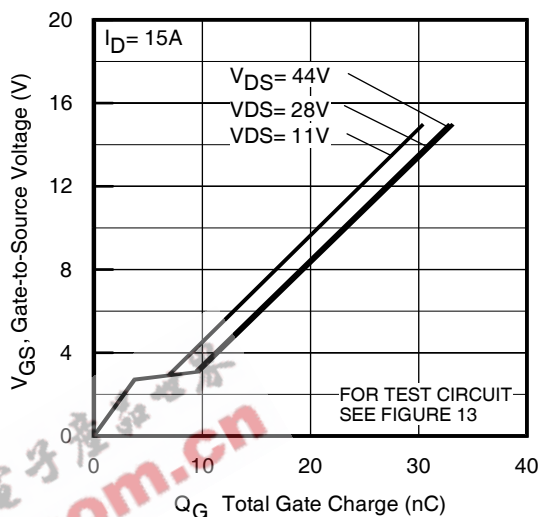


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

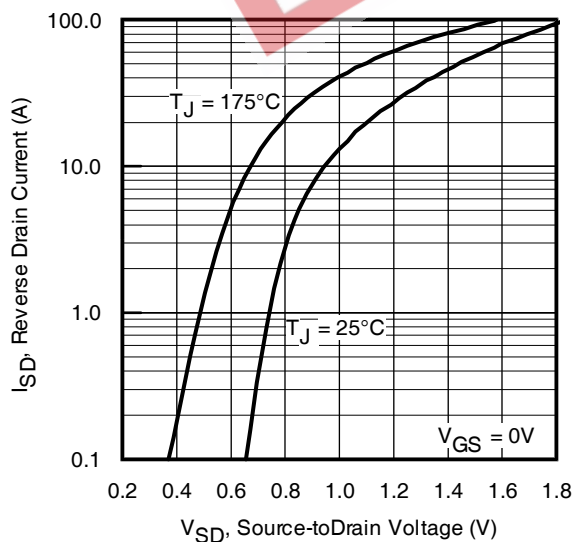


Fig 7. Typical Source-Drain Diode Forward Voltage

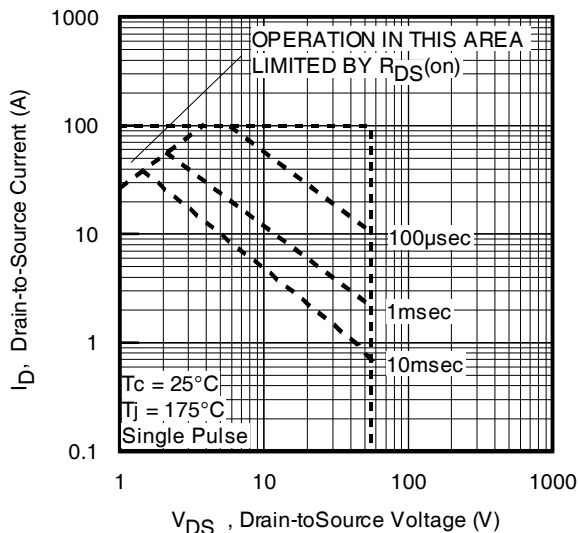


Fig 8. Maximum Safe Operating Area

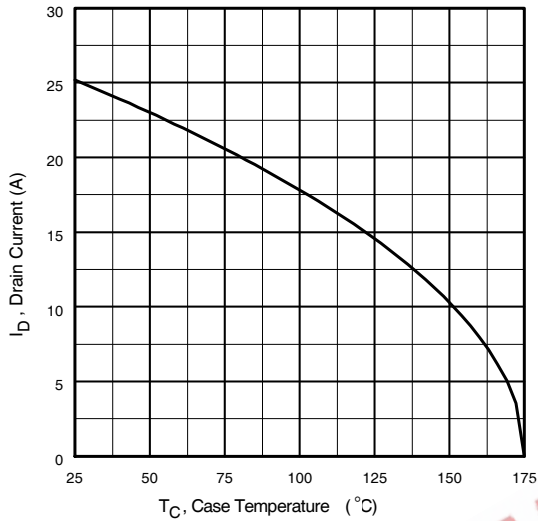


Fig 9. Maximum Drain Current Vs. Case Temperature

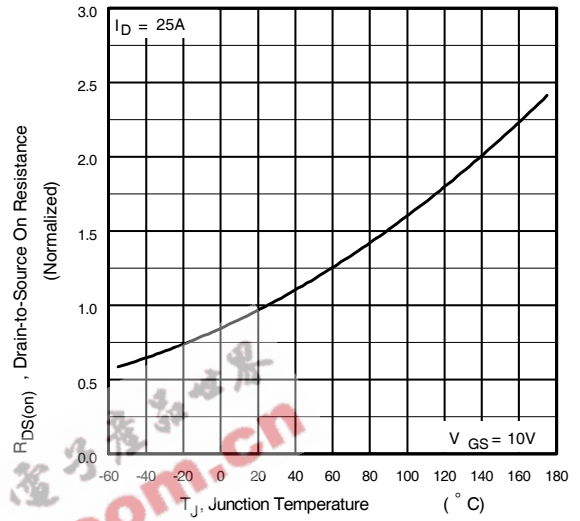


Fig 10. Normalized On-Resistance Vs. Temperature

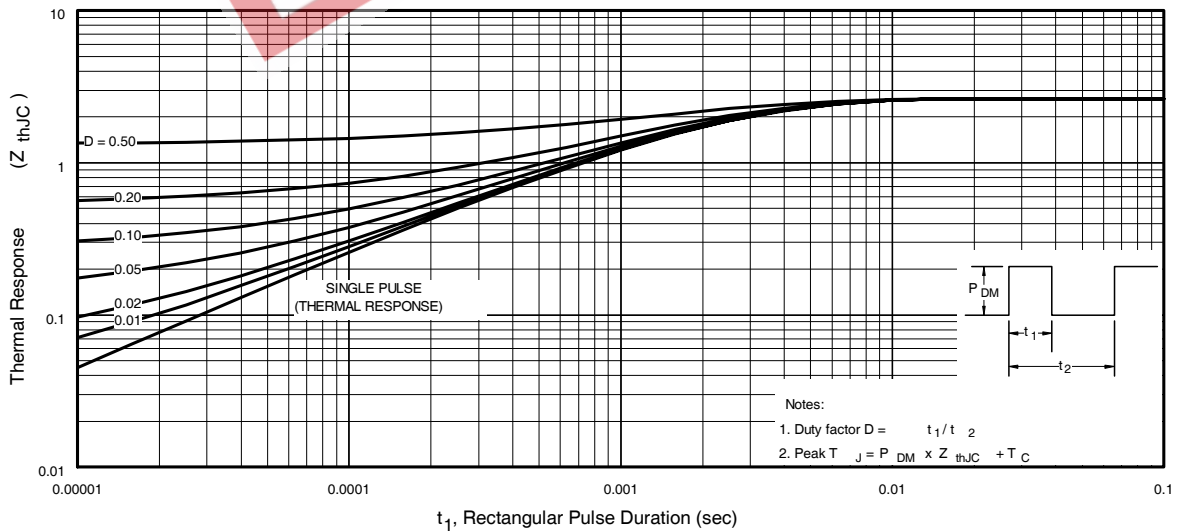


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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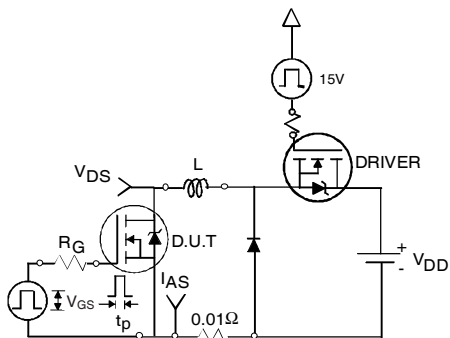


Fig 12a. Unclamped Inductive Test Circuit

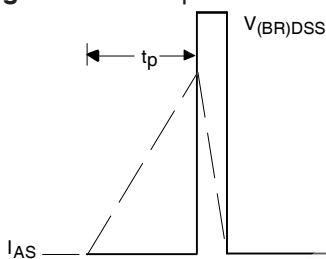


Fig 12b. Unclamped Inductive Waveforms

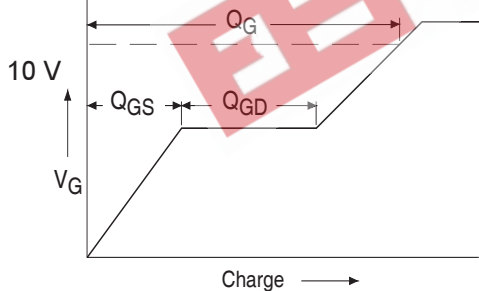


Fig 13a. Basic Gate Charge Waveform

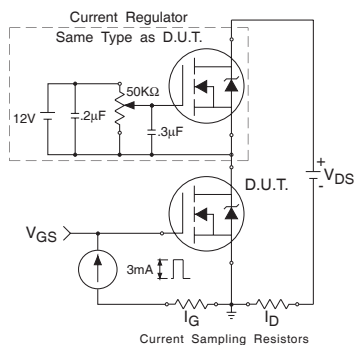


Fig 13b. Gate Charge Test Circuit

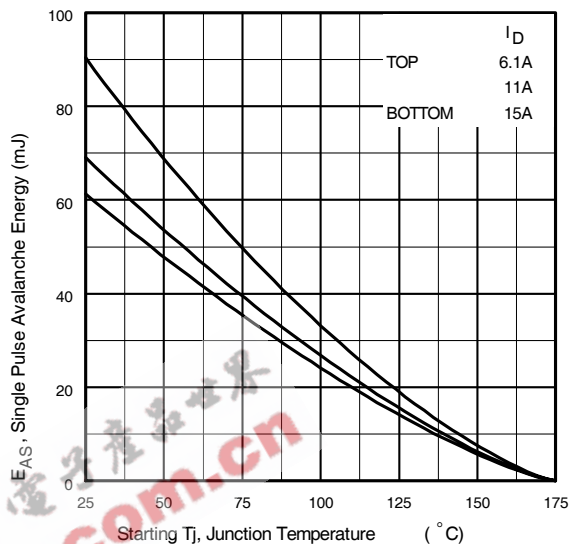


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

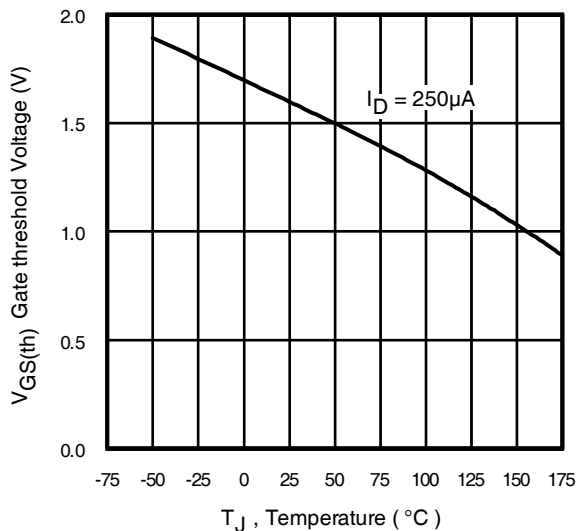


Fig 14. Threshold Voltage Vs. Temperature

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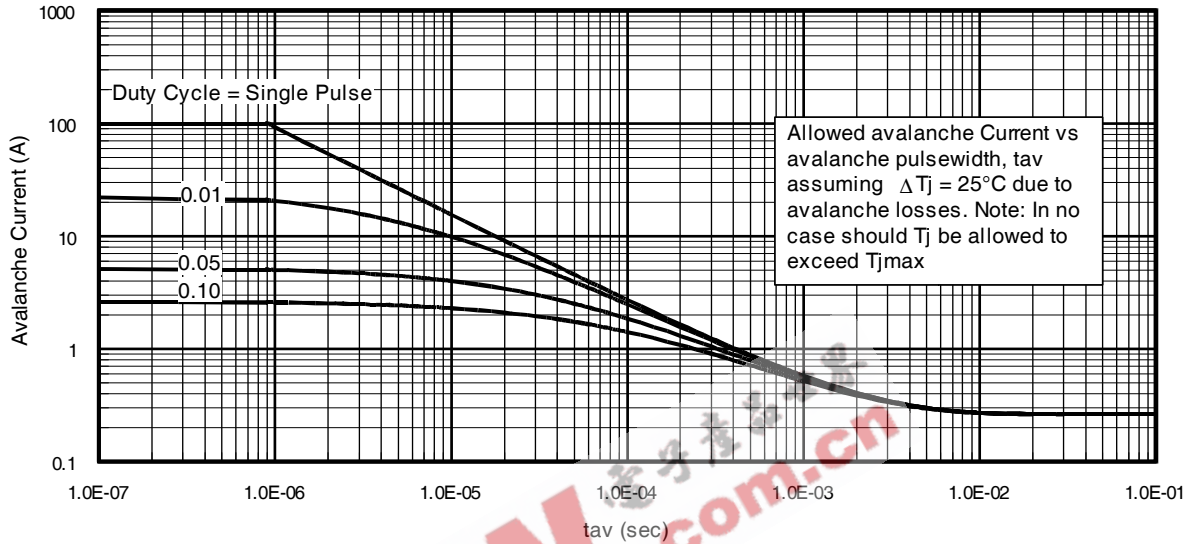


Fig 15. Typical Avalanche Current Vs.Pulsewidth

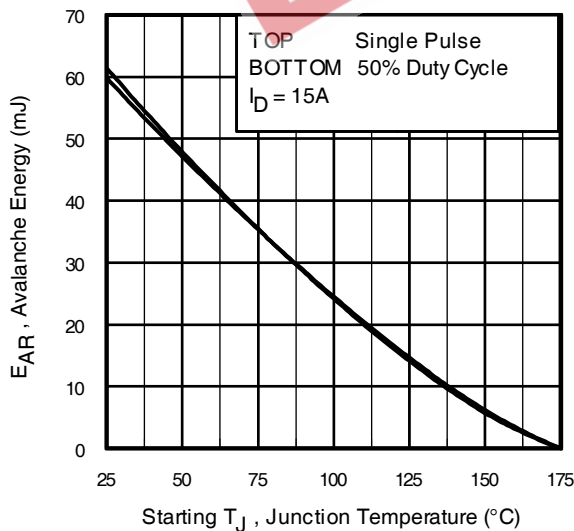


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

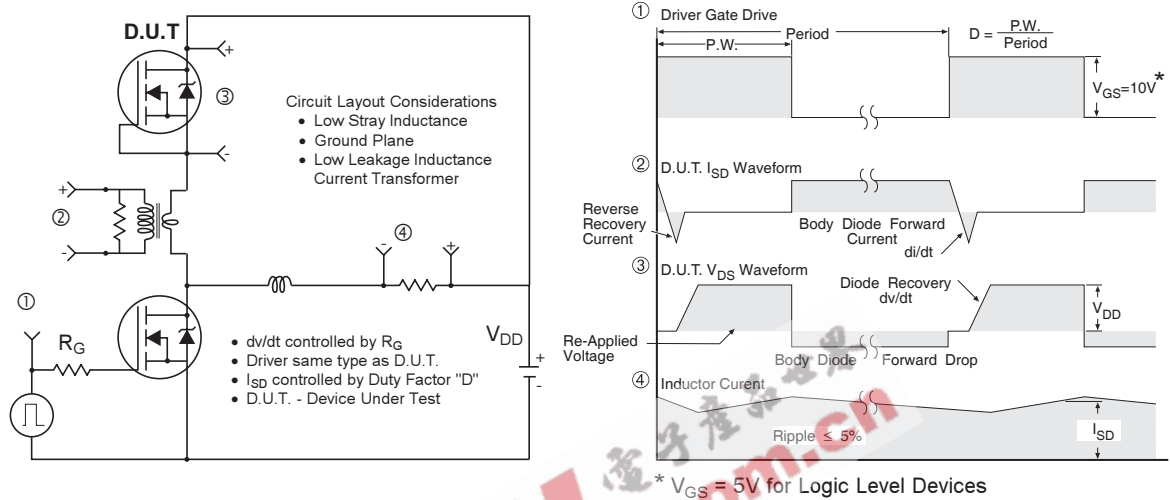


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

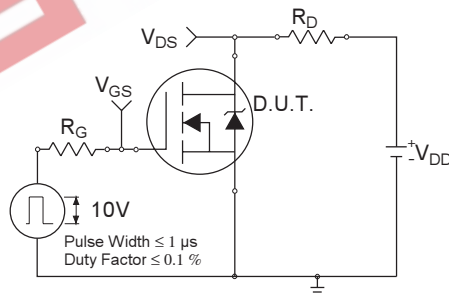


Fig 18a. Switching Time Test Circuit

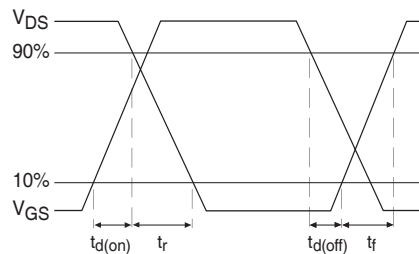
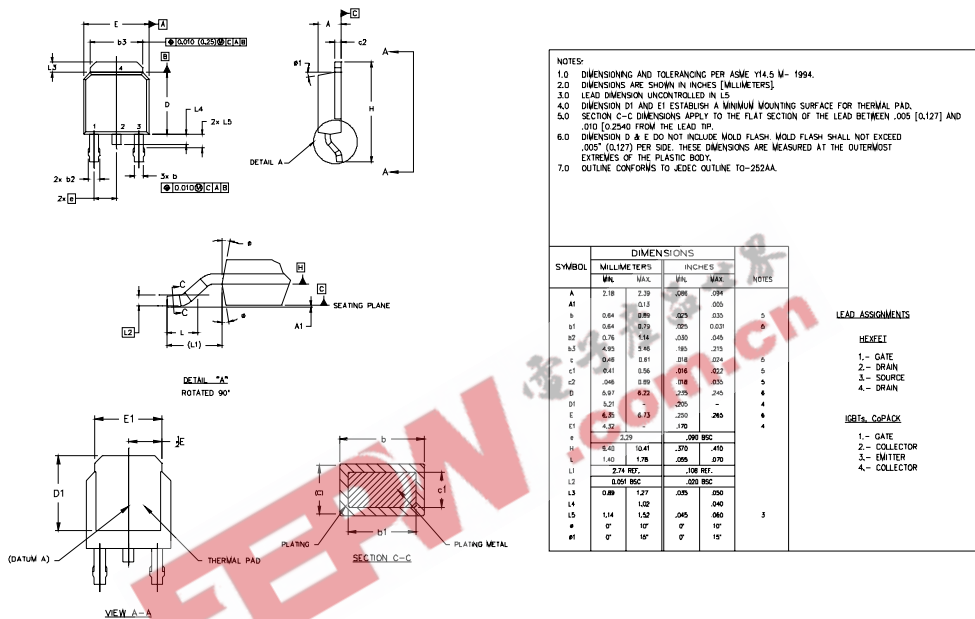


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

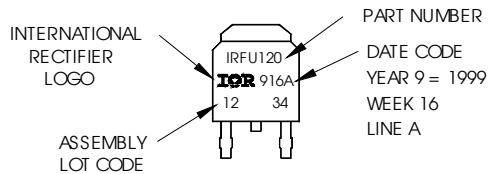
Dimensions are shown in millimeters (inches)



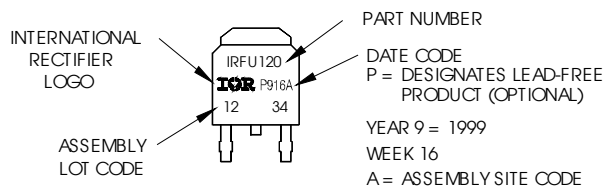
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

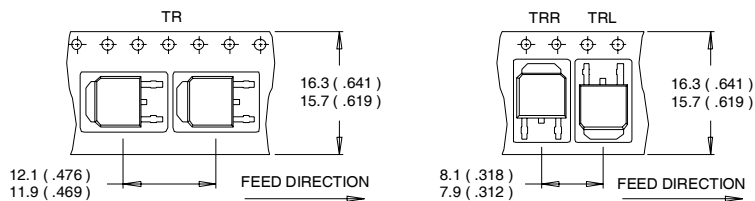


OR

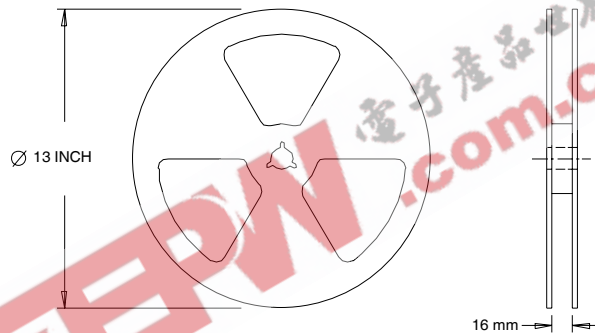


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ C$, $L = 0.55mH$
 $R_G = 25\Omega$, $I_{AS} = 15A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 25A$, $di/dt \leq 290A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ C$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Limited by T_{Jmax} ; see Fig 12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.

Data and specifications subject to change without notice.

This product has been designed and qualified for the Automotive [Q101]market. Qualification Standards can be found on IR's Web site.

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