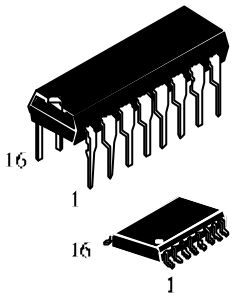
IW4027B

Dual JK Flip-Flop

The IW4027B is a Dual JK Flip-Flop which is edge-triggered and features independent Set, Reset, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Reset and Set are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

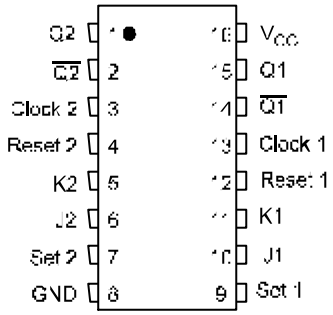
- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply



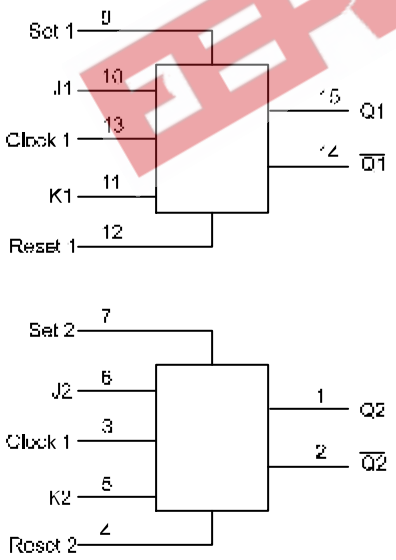
ORDERING INFORMATION

IW4027BN Plastic
IW4027BD SOIC
IZ4027B Chip
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	X	X	X	H	H
L	L	⊓	L	L	No change	
L	L	⊓	H	L	H	L
L	L	⊓	L	H	L	H
L	L	⊓	H	H	$\overline{Q}n$	Qn

X = don't care
Qn+1 = State After Clock Positive Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP, SOIC Package	500**	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating: - Plastic DIP from -55 to +100°C
- SOIC Package from -55 to +65°C
- Plastic DIP: - 10 mW/°C from +100 to +125°C
- SOIC Package: : - 7 mW/°C from +65 to +125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation V_{IN} should be constrained to the range $GND \leq V_{IN} \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	3.5	3.5	3.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	7	7	7	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	11	11	11	
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	1.5	1.5	1.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	3	3	3	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	4	4	4	
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=-1μA	5.0	4.5	4.5	4.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=-1μA	10	9.0	9.0	9.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=-1μA	15	13.5	13.5	13.5	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=1μA	5.0	0.5	0.5	0.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=1μA	10	1.0	1.0	1.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=1μA	15	1.5	1.5	1.5	
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0	1.0	1.0	30	μA
			10	2.0	2.0	60	
			15	4.0	4.0	120	
			20	20	20	600	
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC}					mA
		V_{OL}=0.4 V	5.0	0.64	0.51	0.36	
		V_{OL}=0.5 V	10	1.6	1.3	0.9	
		V_{OL}=1.5 V	15	4.2	3.4	2.4	
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC}					mA
		V_{OH}=4.6 V	5.0	-0.64	-0.51	-0.36	
		V_{OH}=2.5 V	5.0	−2.0	−1.6	−1.15	
		V_{OH}=9.5 V	10	−1.6	−1.3	−0.9	
		V_{OH}=13.5 V	15	−4.2	−3.4	−2.4	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Maximum Clock Frequency	5.0 10 15	3.5 8 12	3.5 8 12	1.75 4 6	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$	5.0 10 15	300 130 90	300 130 90	600 260 180	ns
t_{PLH}	Maximum Propagation Delay, Set to Q or Reset to Q	5.0 10 15	300 130 90	300 130 90	600 260 180	ns
t_{PHL}	Maximum Propagation Delay, Set to $\overline{Q}$ or Reset to Q	5.0 10 15	400 170 120	400 170 120	800 340 240	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_w	Minimum Pulse Width, Clock	5.0 10 15	140 60 40	140 60 40	280 120 80	ns
t_w	Minimum Pulse Width, Set or Reset	5.0 10 15	180 80 50	180 80 50	360 160 100	ns
t_{su}	Minimum Data Setup Time	5.0 10 15	200 75 50	200 75 50	400 150 100	ns
t_r, t_f	Maximum Input Rise or Fall Time, Clock	5.0 10 15	45 5 2	45 5 2	90 10 4	μs

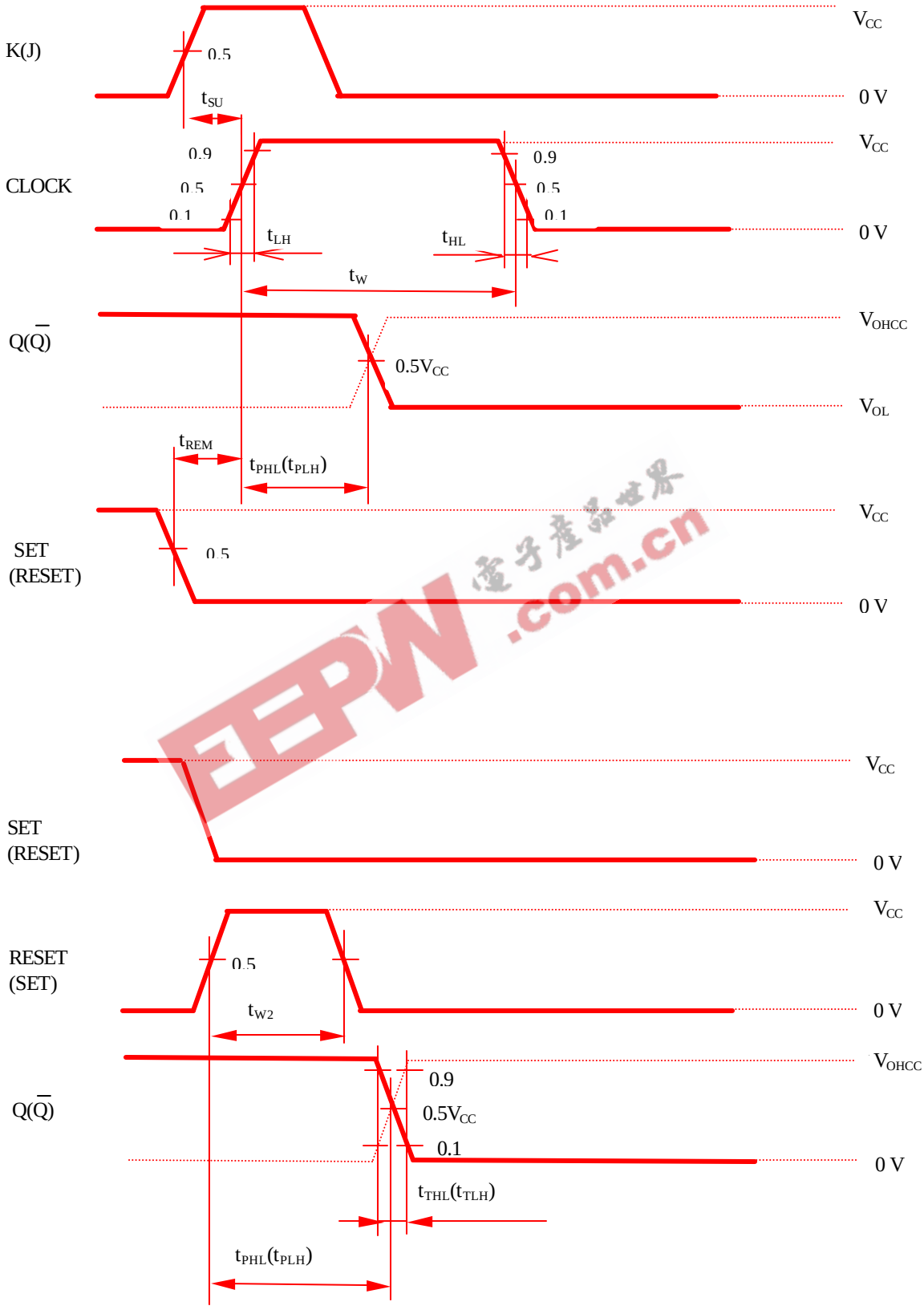
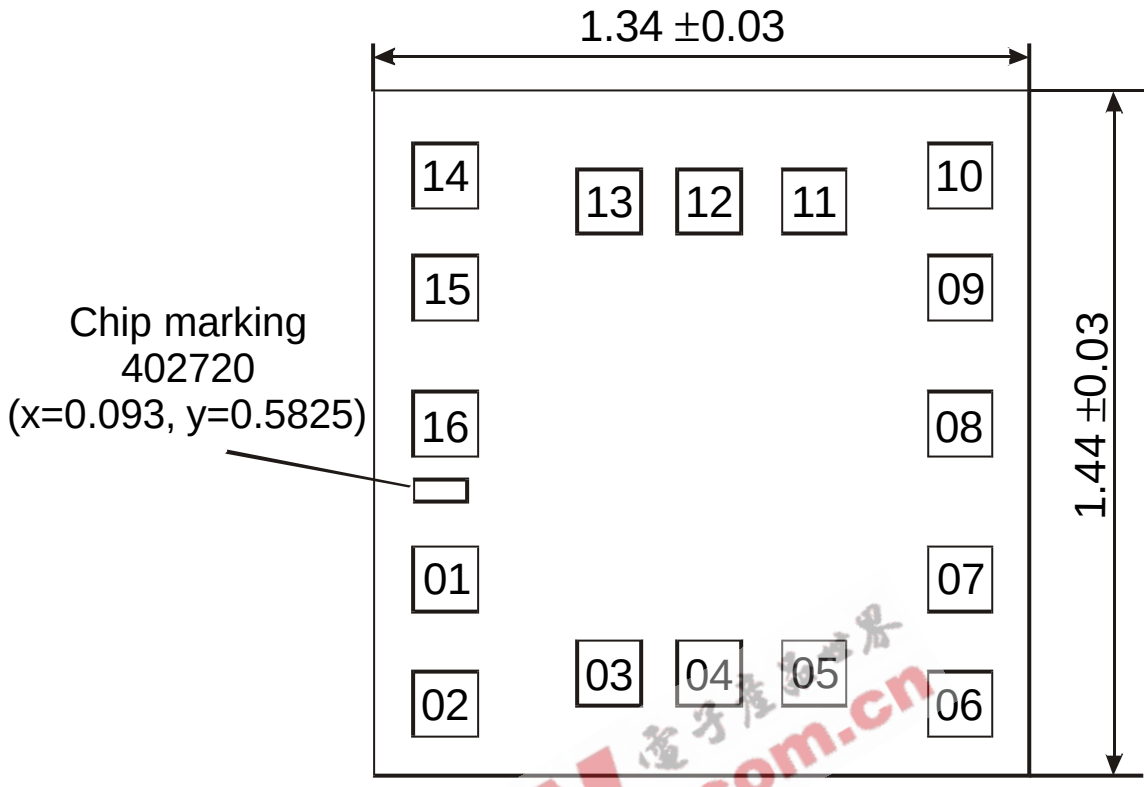


Figure 1. Switching Waveforms



CHIP PAD DIAGRAM IZ4027B

Pad size 0.100 x 0.100 mm (Pad size is given as per passivation layer)
Thickness of chip 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	Q2	0.116	0.4215
02	$\overline{Q2}$	0.111	0.126
03	Clock 2	0.474	0.1755
04	Reset 2	0.6555	0.1755
05	K2	0.8335	0.174
06	J2	1.124	0.1235
07	Set 2	1.124	0.4065
08	GND	1.1245	0.6855
09	Set 1	1.124	0.9335
10	J1	1.124	1.2165
11	K1	0.8335	1.166
12	Reset 1	0.6555	1.1645
13	Clock 1	0.474	1.1645
14	$\overline{Q1}$	0.111	1.214
15	Q1	0.116	0.9185
16	Vcc	0.116	0.7365