

Applications

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power
- Lead-Free

V_{DSS}	R_{DS(on)} max	I_D
20V	20mΩ	36A

Benefits

- Ultra-Low Gate Impedance
- Very Low R_{DS(on)} at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	36 ⑤	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ 10V	31	
I _{DM}	Pulsed Drain Current①	140	
P _D @ T _C = 25°C	Maximum Power Dissipation③	47	W
P _D @ T _C = 70°C	Maximum Power Dissipation③	33	W
	Linear Derating Factor	0.31	W/°C
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	3.2	°C/W
R _{θJA}	Junction-to-Ambient	—	50	
R _{θJA}	Junction-to-Ambient (PCB mount)④	—	110	

Notes ① through ⑤ are on page 10

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	15	20	mΩ	V _{GS} = 10V, I _D = 18A ③
		—	21	28		V _{GS} = 4.5V, I _D = 14A ③
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 16V, V _{GS} = 0V
		—	—	100		V _{DS} = 16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-200		V _{GS} = -16V

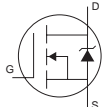
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	17	—	—	S	V _{DS} = 10V, I _D = 14A
Q _g	Total Gate Charge	—	6.5	9.7	nC	I _D = 14A
Q _{gs}	Gate-to-Source Charge	—	1.8	—		V _{DS} = 10V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	2.9	—		V _{GS} = 4.5V
Q _{oss}	Output Gate Charge	—	7.1	—		V _{GS} = 0V, V _{DS} = 10V
t _{d(on)}	Turn-On Delay Time	—	8.7	—		V _{DD} = 10V
t _r	Rise Time	—	78	—	ns	I _D = 14A
t _{d(off)}	Turn-Off Delay Time	—	10	—		R _G = 1.8Ω
t _f	Fall Time	—	4.5	—		V _{GS} = 4.5V ③
C _{iss}	Input Capacitance	—	670	—		V _{GS} = 0V
C _{oss}	Output Capacitance	—	470	—		V _{DS} = 10V
C _{rss}	Reverse Transfer Capacitance	—	68	—	pF	f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	72	mJ
I _{AR}	Avalanche Current②	—	14	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	36⑤	—	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ④	—	140	—		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 18A, V _{GS} = 0V ③
		—	0.88	—		T _J = 125°C, I _S = 18A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	35	53	ns	T _J = 25°C, I _F = 18A, V _R = 10V
Q _{rr}	Reverse Recovery Charge	—	34	51	nC	di/dt = 100A/μs ③
t _{rr}	Reverse Recovery Time	—	35	53	ns	T _J = 125°C, I _F = 18A, V _R = 10V
Q _{rr}	Reverse Recovery Charge	—	35	53	nC	di/dt = 100A/μs ③

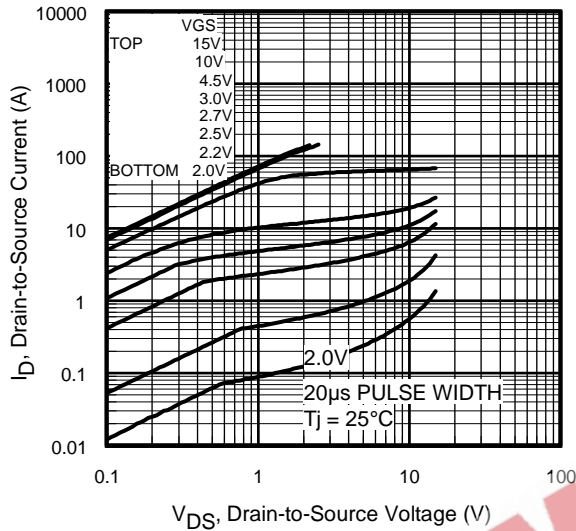


Fig 1. Typical Output Characteristics

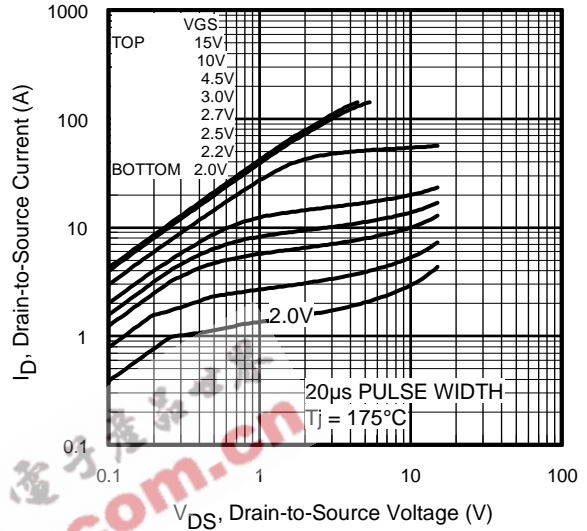


Fig 2. Typical Output Characteristics

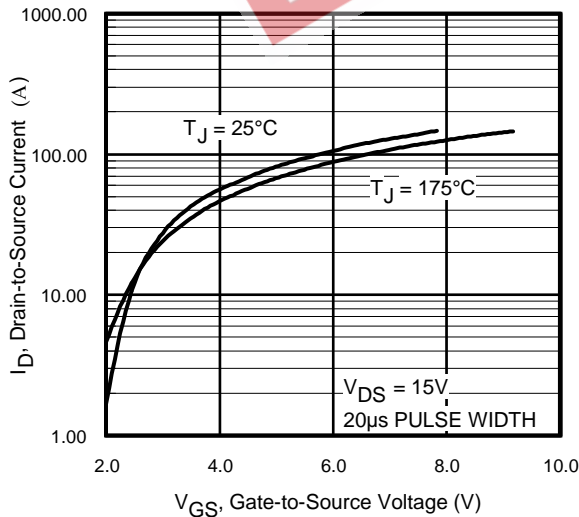


Fig 3. Typical Transfer Characteristics

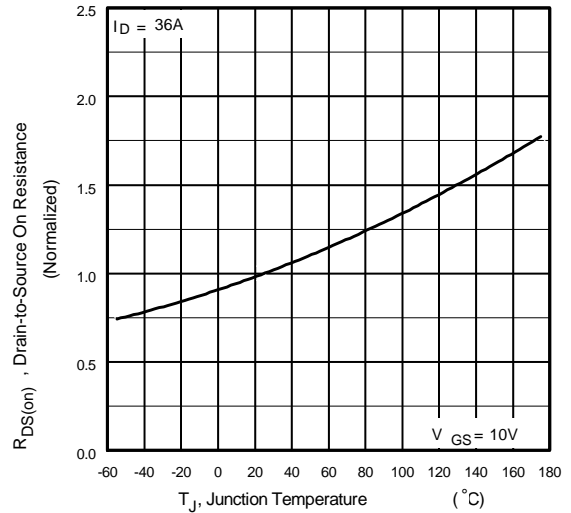


Fig 4. Normalized On-Resistance Vs. Temperature

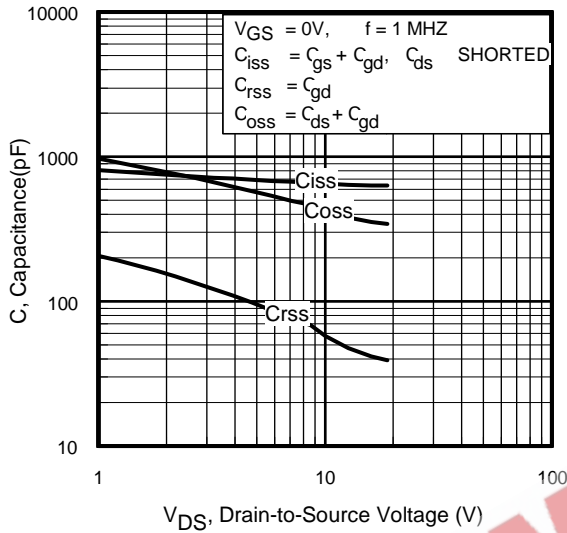


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

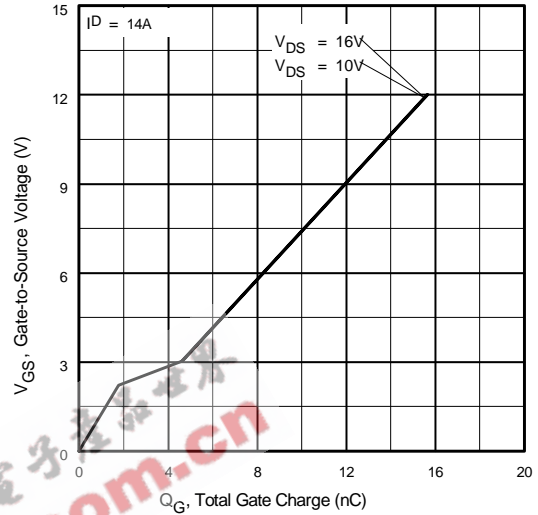


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

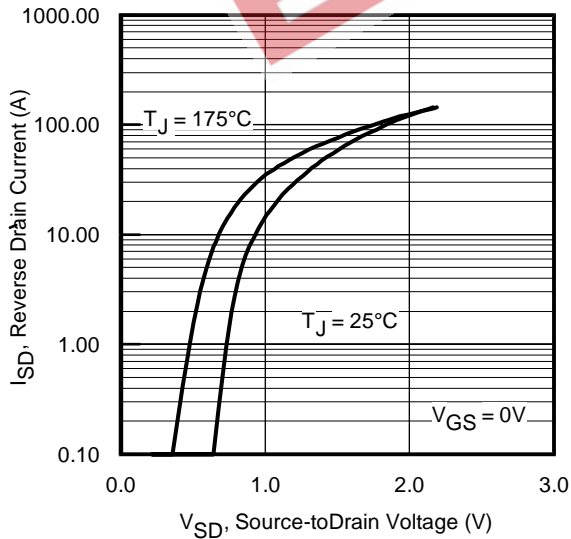


Fig 7. Typical Source-Drain Diode Forward Voltage

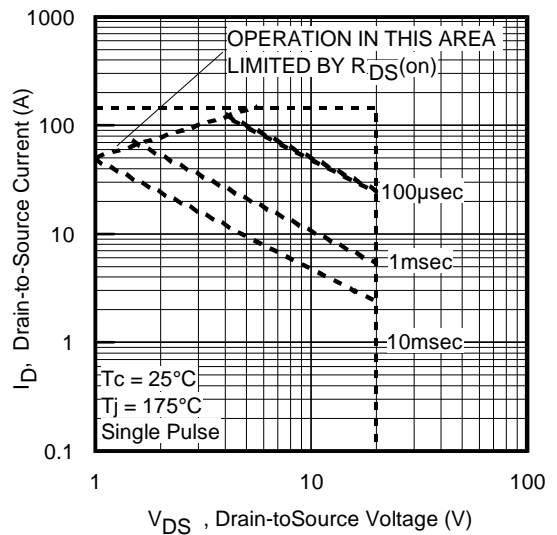


Fig 8. Maximum Safe Operating Area

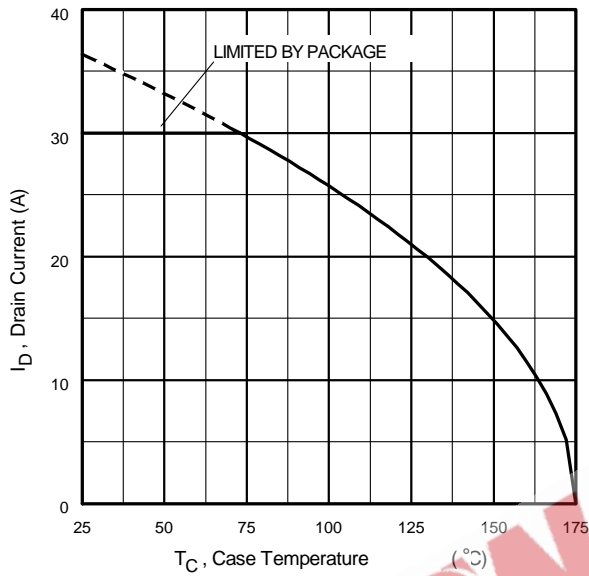


Fig 9. Maximum Drain Current Vs. Case Temperature

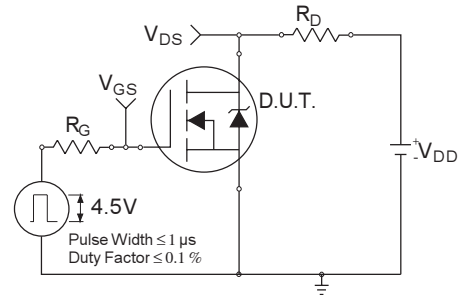


Fig 10a. Switching Time Test Circuit

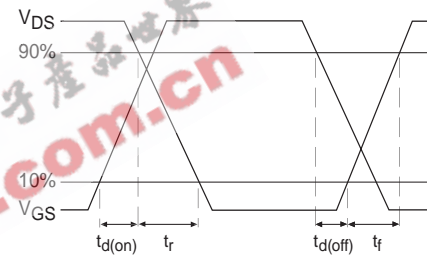


Fig 10b. Switching Time Waveforms

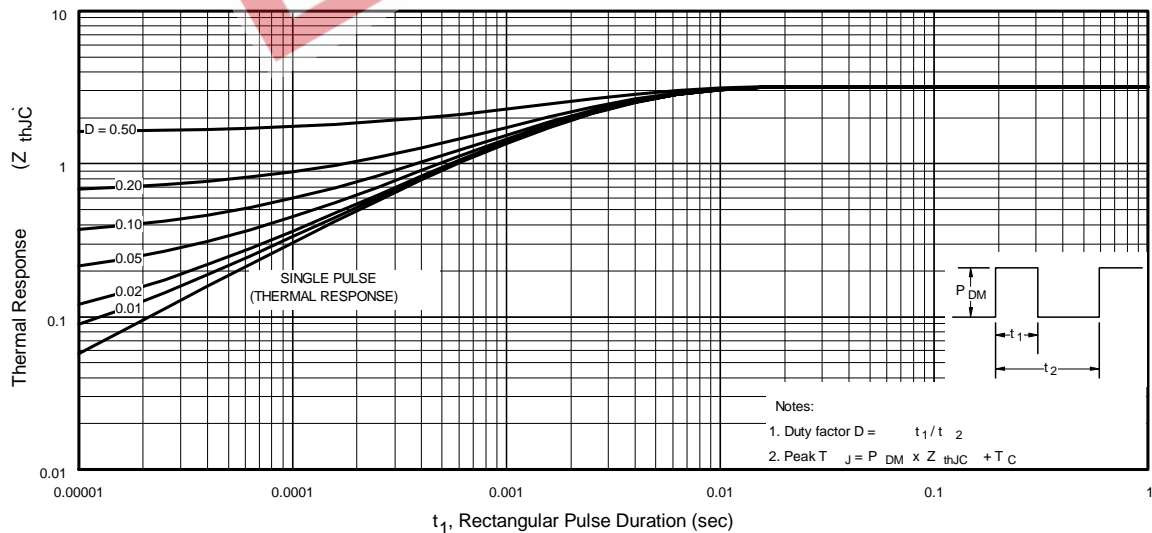


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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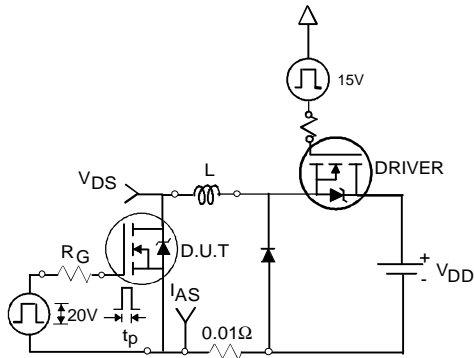


Fig 12a. Unclamped Inductive Test Circuit

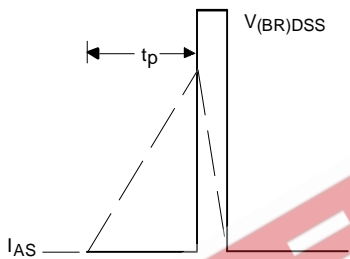


Fig 12b. Unclamped Inductive Waveforms

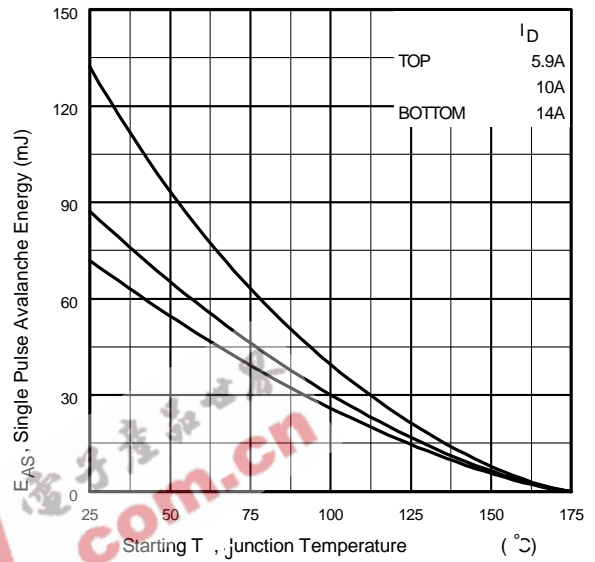


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

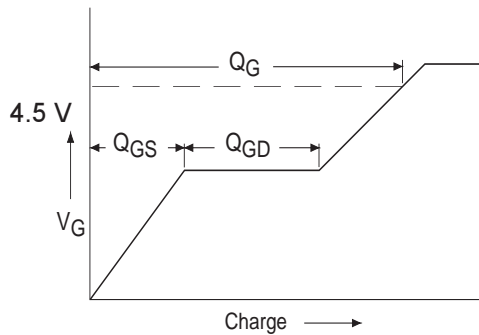


Fig 13a. Basic Gate Charge Waveform

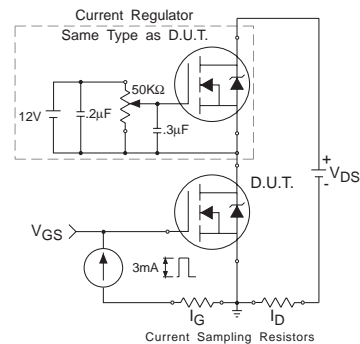
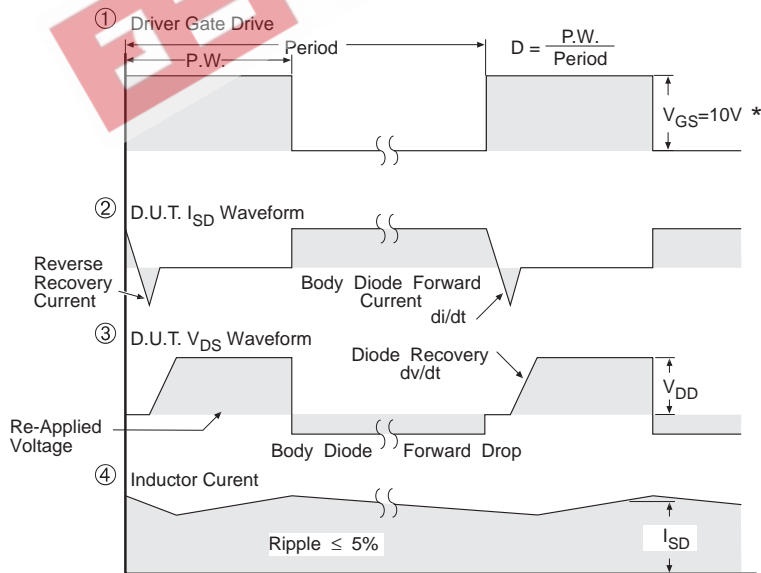
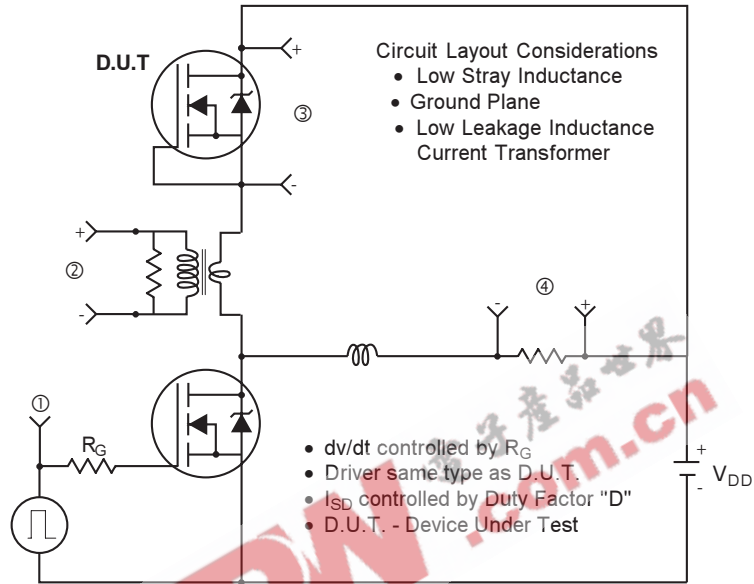


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

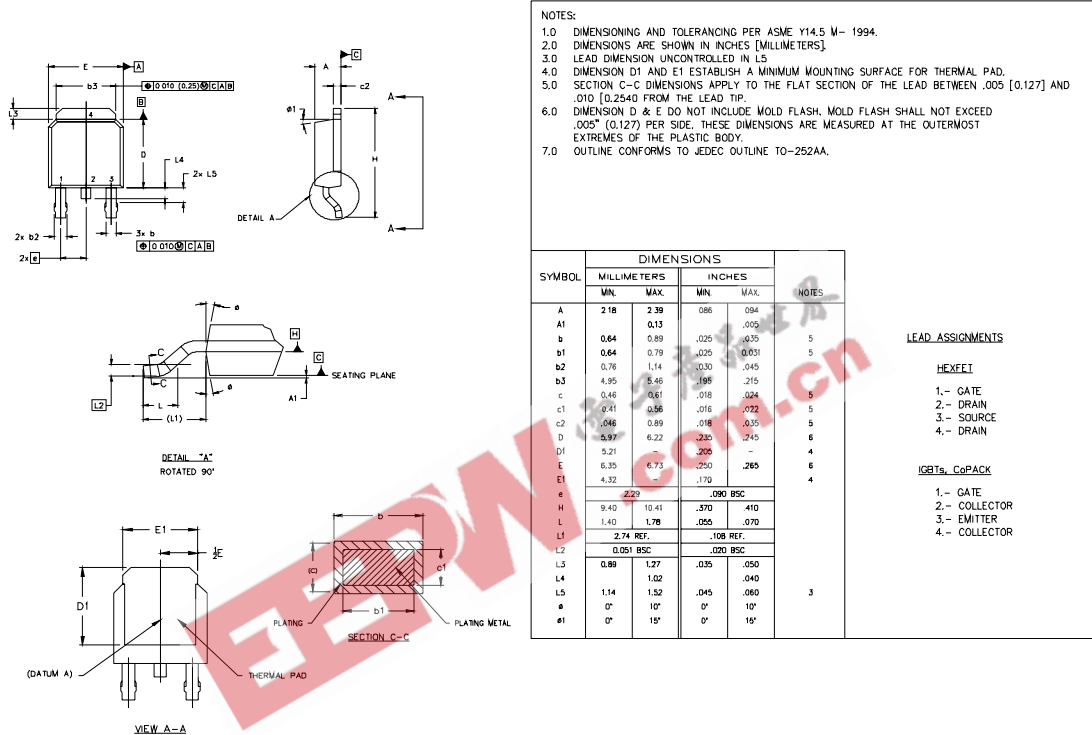
Fig 14. For N-Channel HEXFET® Power MOSFETs

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D-Pak (TO-252AA) Package Outline

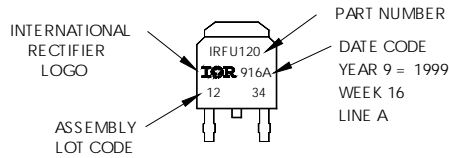
Dimensions are shown in millimeters (inches)



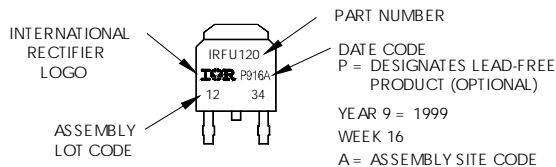
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 1999 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



OR

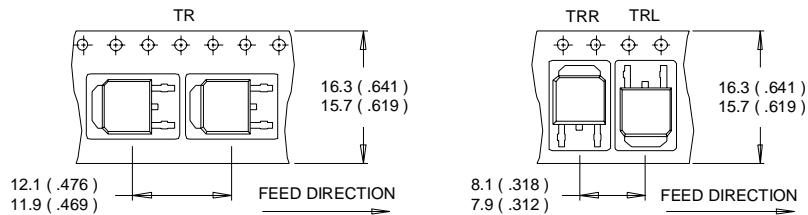


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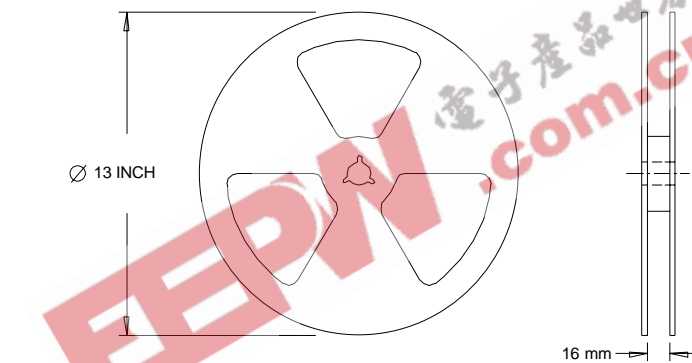
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D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.69\text{ mH}$
 $R_G = 25\Omega$, $I_{AS} = 14\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑤ Calculated continuous current based on maximum allowable junction temperature; Package limitation current is 30A

Data and specifications subject to change without notice.
These products have been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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