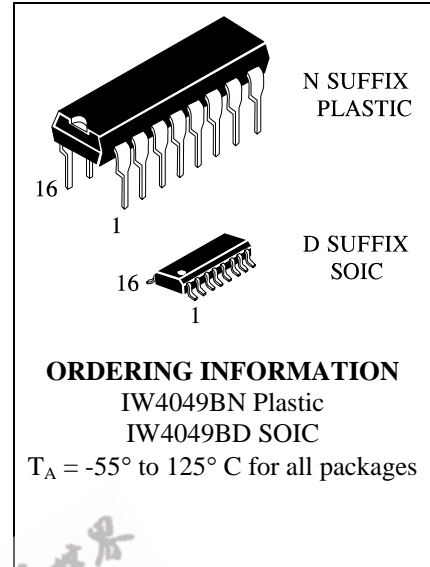


IW4049B

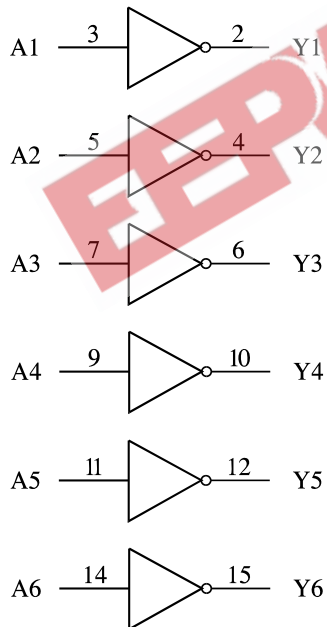
Hex Buffer/Converter
High-Voltage Silicon-Gate CMOS

The IW4049B is inverting hex buffers and feature logic-level conversion using only one supply (voltage V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 0.5 V min @ 5.0 V supply
 1.0 V min @ 10.0 V supply
 1.0 V min @ 15.0 V supply
- High-to-low level conversion



LOGIC DIAGRAM



PINS 13, 16 = NO CONNECTION
 PIN 1 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

V_{CC}	1	16	NC
Y1	2	15	Y6
A1	3	14	A6
Y2	4	13	NC
A2	5	12	Y5
Y3	6	11	A5
A3	7	10	Y4
GND	8	9	A4

NC = NO CONNECTION

FUNCTION TABLE

Inputs	Output
A	Y
H	L
L	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	V_{CC}^{**} to +18	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

** The IW4049B has high-to-low level voltage conversion capability but not low-to-high level; therefore it is recommended that $V_{IN} \geq V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	V_{CC}^{**}	18	V
V_{OUT}	DC Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

** The IW4049B has high-to-low level voltage conversion capability but not low-to-high level; therefore it is recommended that $V_{IN} \geq V_{CC}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.5V V _{OUT} = 1.0 V V _{OUT} = 1.5V	5.0	4	4	4	V
			10	8	8	8	
			15	12.5	12.5	12.5	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} = V _{CC} - 0.5V V _{OUT} = V _{CC} - 1.0 V V _{OUT} = V _{CC} - 1.5V	5.0	1	1	1	V
			10	2	2	2	
			15	2.5	2.5	2.5	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	4.5	3.3	2.6	1.8	mA
			5	4	3.2	2.4	
			10	10	8	5.6	
			15	26	24	18	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-2.6	-2.1	-1.55	mA
			5.0	-0.81	-0.65	-0.48	
			10	-2.0	-1.65	-1.18	
			15	-5.2	-4.3	-3.1	

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{IN} V	V_{CC} V	Guaranteed Limit			Unit
				$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5	5	120	120	240	ns
		10	10	65	65	130	
		10	5	90	90	180	
		15	15	50	50	100	
		15	5	90	90	180	
t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5	5	65	65	130	ns
		10	10	40	40	80	
		10	5	30	30	60	
		15	15	30	30	60	
		15	5	20	20	40	
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5	5	160	160	320	ns
		10	10	80	80	160	
		15	15	60	60	120	
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5	5	60	60	120	ns
		10	10	40	40	80	
		15	15	30	30	60	
C_{IN}	Maximum Input Capacitance	-	-		22.5		pF

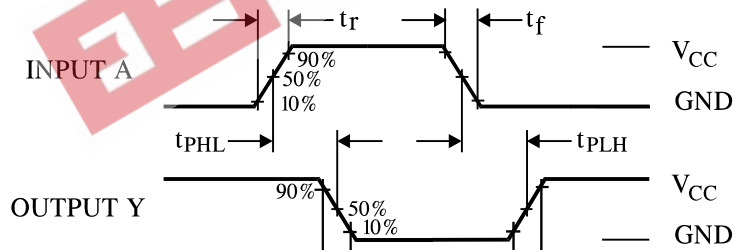
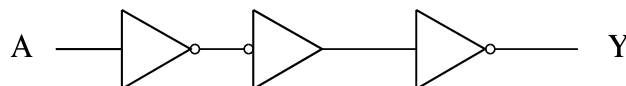
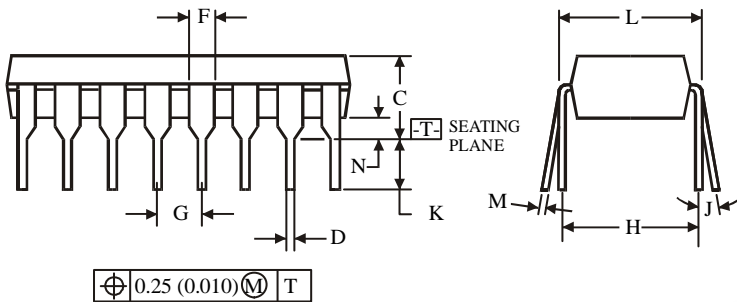
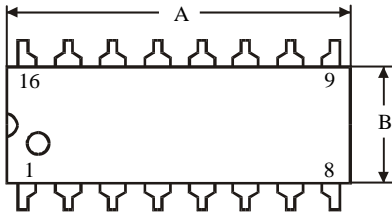
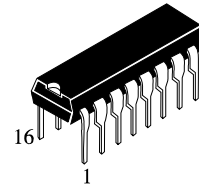


Figure 1. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/6 of the Device)



**N SUFFIX PLASTIC
(MS - 001BB)**

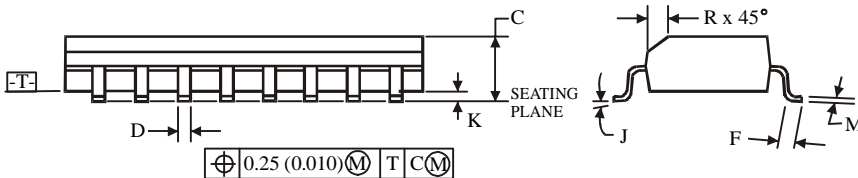
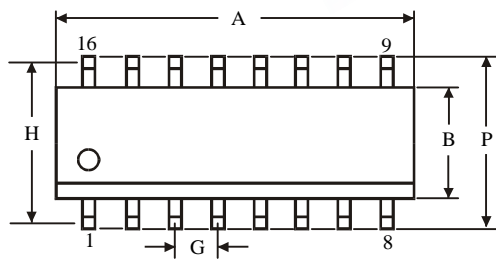
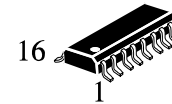


Symbol	Dimensions, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

**D SUFFIX SOIC
(MS - 012AC)**



Symbol.	Dimensions, mm	
	MIN	MAX
A	9.80	10.0
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A, for B - 0.25 mm (0.010) per side.