

# P-Channel JFET



## J270 – J271 / SST270 – SST271

### FEATURES

- Surface Mount

### APPLICATIONS

- P-Channel Amplifier

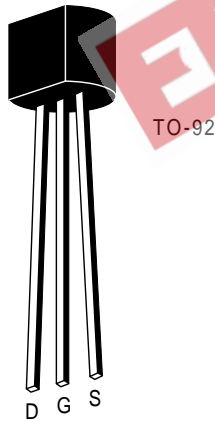
### DESCRIPTION

The J270/SST270 Series is an all-purpose amplifier for designs requiring P-channel operation. These devices feature high gain, low noise and tight  $V_{GS(OFF)}$  limits for simple circuit design. They are available in low-cost SOT-23 and TO-92 packages and are fully compatible with automatic insertion techniques.

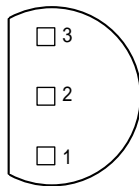
### ORDERING INFORMATION

Part	Package	Temperature Range
J270-271	Plastic TO-92	-55°C to +135°C
SST270-271	Plastic SOT-23	-55°C to +135°C

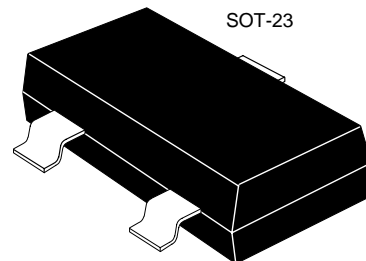
### PIN CONFIGURATION



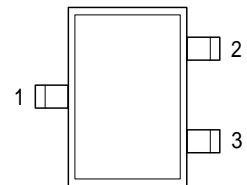
- 1 DRAIN
- 2 GATE
- 3 SOURCE



BOTTOM VIEW



- 1 GATE
- 2 SOURCE
- 3 DRAIN



TOP VIEW

5508

PRODUCT MARKING (SOT-23)	
SST270	P20
SST271	P21



# J270 – J271 / SST270 – SST271

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNIT
Gate-Drain Voltage	V <sub>GD</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	30	V
Gate Current	I <sub>G</sub>	-50	mA
Power Dissipation	P <sub>D</sub>	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T <sub>J</sub>	-55 to 150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T <sub>L</sub>	300	°C

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TYP <sup>1</sup>	270		271		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
STATIC								
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	45	30		30		V	I <sub>G</sub> = 1μA, V <sub>DS</sub> = 0V
V <sub>GS(OFF)</sub>	Gate-Source Cutoff Voltage		0.5	2.0	1.5	4.5		V <sub>DS</sub> = -15V, I <sub>D</sub> = -1nA
I <sub>DSS</sub>	Saturation Drain Current <sup>2</sup>		-2	-15	-6	-50	mA	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V
I <sub>GSS</sub>	Gate Reverse Current	10				200	pA	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0V
		5					nA	T <sub>A</sub> = 125°C
I <sub>G</sub>	Gate Operating Current	10					pA	V <sub>DG</sub> = -15V, I <sub>D</sub> = -1mA
V <sub>GS(F)</sub>	Gate-Source Forward Voltage	-0.7					V	I <sub>G</sub> = -1mA, V <sub>DS</sub> = 0V
DYNAMIC								
g <sub>fs</sub>	Common-Source Forward Transconductance		6	15	8	18	mS	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f = 1kHz
g <sub>os</sub>	Common-Source Output Conductance			200		500	μS	
C <sub>iss</sub>	Common-Source Input Capacitance	20					pF	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V f = 1MHz
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	4						
e <sub>n</sub>	Equivalent Input Noise Voltage	20					$\frac{nV}{\sqrt{Hz}}$	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V f = 1kHz

- NOTES: 1. For design aid only, not subject to production testing.  
 2. Pulse test; PW = 300μs, duty cycle ≤ 3%.