

DUAL J-K FLIP-FLOP  
(COMMON CLOCK)

MC524 • MC574  
MC424 • MC474

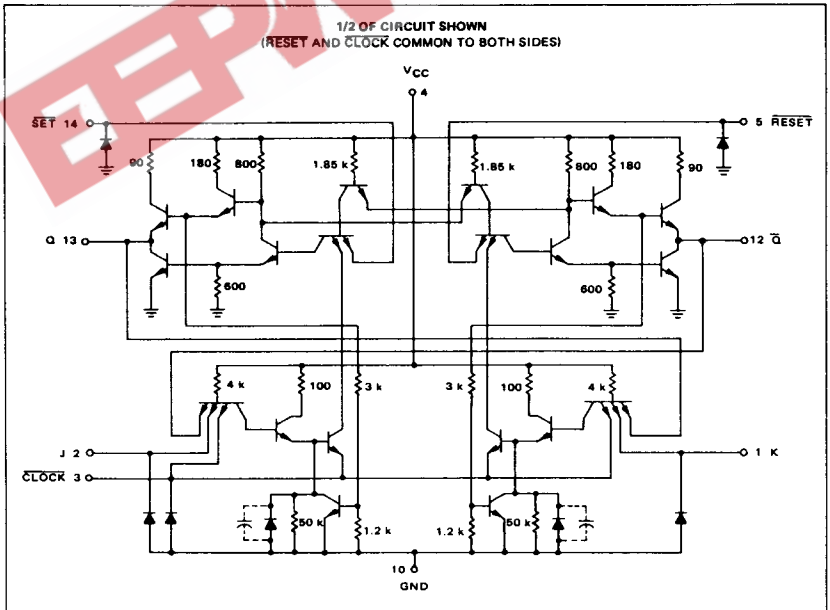
These devices are dual clocked flip-flops that trigger on the negative edge of the clock pulse and perform the J-K logic function. Each flip-flop in the package has one clocked J, one clocked K, and one direct SET input. A direct RESET and the CLOCK input are common to both flip-flops. Both Q and  $\bar{Q}$  outputs are available on each flip-flop.

Information is changed on the J and K inputs while the clock is in the low state, since the inputs are inhibited in this condition. Information is transferred into a temporary

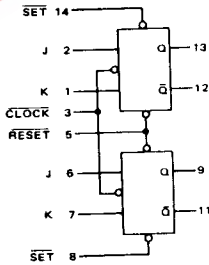
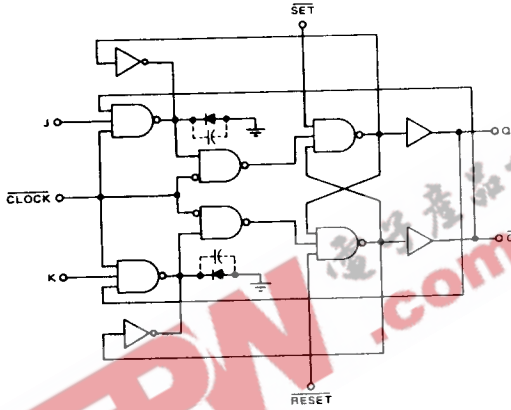
memory when the clock goes to the high state. When the clock returns low, the information is transferred to the bi-stable section and the Q and  $\bar{Q}$  outputs. The information on the J and K inputs should not be changed while the clock is in the high state. Each flip-flop can be set or reset directly by applying the low state to the direct SET or RESET inputs.

Since these flip-flops are charge-storage devices, there is a restriction on the clock fall time that must be observed.

TYPE NO.	INPUT LOADING FACTOR (If)							OUTPUT DRIVE (I <sub>OL</sub> )	TEMPERATURE RANGE	
	CLOCK	SET	RESET	J, K	CLOCK	SET	RESET			
MC524 MC574	3.0	1.8	3.8	1.0	(-2.66 mA)	(-2.4 mA)	(-4.8 mA)	(-1.33 mA)	16 MC500 series Gates (22.0 mA) 8 MC500 series Gates (12.0 mA)	-85°C to +125°C
MC424 MC474	3.0	1.7	3.4	1.0	(-3.32 mA)	(-2.8 mA)	(-5.6 mA)	(-1.66 mA)	13 MC400 series Gates (22.5 mA) 7 MC400 series Gates (12.8 mA)	0°C to +75°C



LOGIC DIAGRAM  
1/2 OF DEVICE SHOWN



$t_n$		$t_{n+1}$	
J	K	Q	$\bar{Q}$
0	0	$Q_n$	$\bar{Q}_n$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_n$	$Q_n$

Total Power Dissipation = 110 mW typ/pkg  
 Switching Times  
 $t_{pd}$  = 12 ns typ  
 $t_{pd+}$  = 10 ns typ  
 Operating Frequency = 45 MHz typ





OPERATING CHARACTERISTICS

Clock fall time  $\leq 100$  ns.  
 Triggers on clock pulse widths  $\geq 12$  ns.  
 Provides direct SET and RESET inputs. The application of a "0" state to the SET will cause Q to go to the "1" state; application of a "0" state to the RESET will cause both Q pins to go to the "1" state. The SET or RESET can be applied 20 ns after the clock has changed to the low state. It should not be applied when the clock is in the high state.

Data at the J and K inputs must be present before the clock goes to a high state. If the information on the J and K inputs is changed while the clock is in a high state, the flip-flop will require typically  $1.0 \mu\text{s}$  to recognize a "1" state to "0" state information change on the J and K terminals. The flip-flop typically requires 10 ns to recognize a "0" state to a "1" state change.

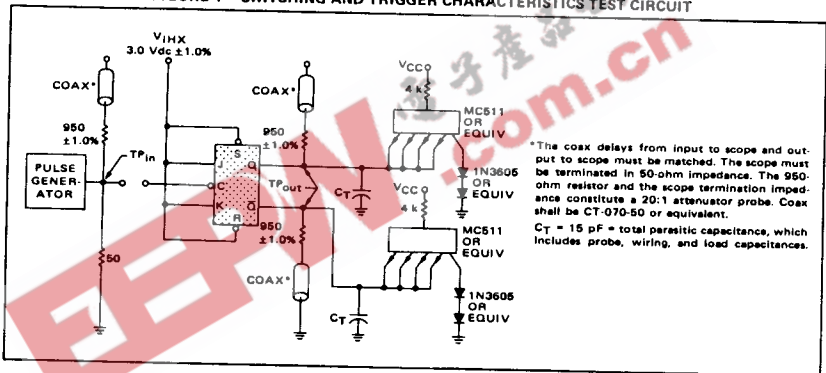
Negative edge triggering - When the clock changes from the high state to the low state, the information in the temporary storage section is transferred to the bistable network and the Q and  $\bar{Q}$  outputs. While the clock is in a low state, the J and K terminals are inhibited.

Unused J and K inputs should be tied to the clock or to a voltage between 2.0 and 5.0 Vdc. Unused SET or RESET inputs must be tied to a voltage between 2.0 and 5.0 Vdc.

The maximum allowable skew time for these devices is 9.0 ns. This is the total of the minimum propagation delay (5.0 ns) and the minimum time to recognize a "0" to "1" state information change (4.0 ns).

Operating frequency of the flip-flops is not significantly affected by capacitive loading due to the buffered outputs.

FIGURE 1 - SWITCHING AND TRIGGER CHARACTERISTICS TEST CIRCUIT



\*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 60-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.  
 $C_t = 15 \text{ pF}$  = total parasitic capacitance, which includes probe, wiring, and load capacitances.

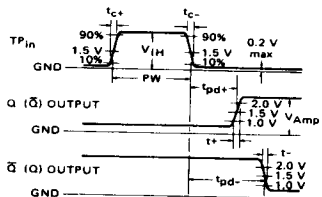
SWITCHING TIMES

TEST	TEST SYMBOL	INPUT PULSE	MIN	MAX	UNIT
Delay Time Off	$t_{pd+}$	X	-	20	ns
Delay Time On	$t_{pd-}$	X	-	20	ns
Rise Time	$t_r$	X	-	4.0	ns
Fall Time	$t_f$	X	-	2.5	ns
Amplitude	$V_{amp}$	X	3.0	-	Volt

WORST CASE TESTS  
 (Devices must toggle with each clock pulse)

TEST	SYMBOL	LIMITS	INPUT CONDITIONS
Toggle Frequency	$f_{Tog}$	35 MHz max	W
Pulse Width	PW	12 ns min	X
Input High Voltage	$V_{IH}$	2.4 V min	Y
Fall Time	$t_c-$	100 ns max	Z

VOLTAGE WAVEFORMS AND DEFINITIONS



INPUT PULSE CONDITIONS

SYMBOL	W	X	Y	Z	UNIT
PRF	35	5.0	5.0	1.0	MHz
PW	12	12	15	200	ns
$t_{c+}$	$\leq 2.0$	$\leq 2.0$	$\leq 5.0$	$\leq 50$	ns
$t_{c-}$	$\leq 2.0$	$\leq 2.0$	$\leq 5.0$	100	ns
$V_{IH}$	3.0	3.0	2.4	3.0	Volt

FIGURE 2 - J-K TERMINAL CHARACTERISTICS TEST CIRCUIT

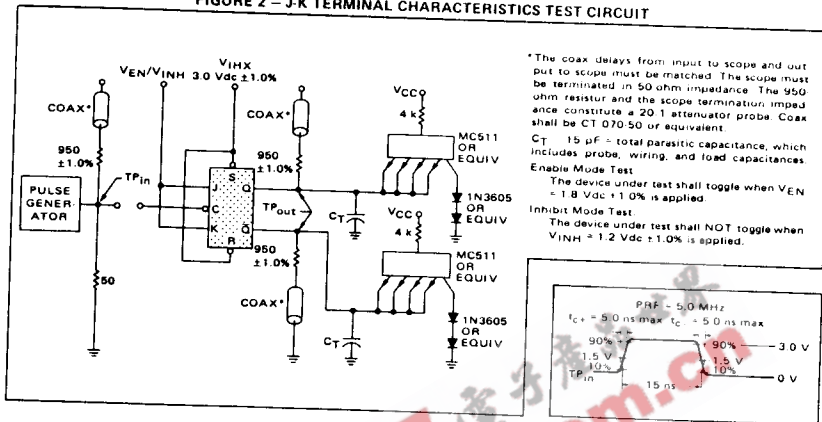
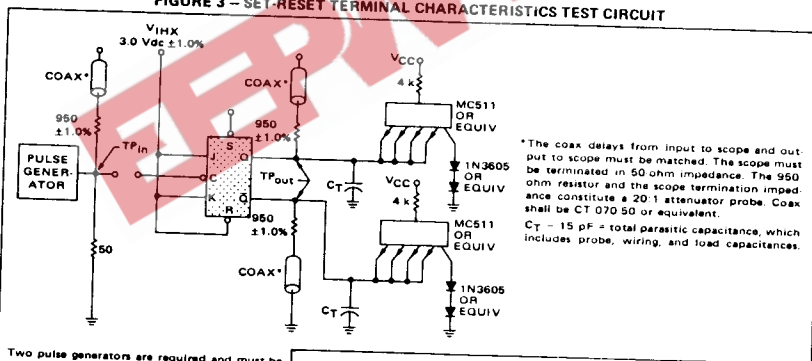


FIGURE 3 - SET-RESET TERMINAL CHARACTERISTICS TEST CIRCUIT



Two pulse generators are required and must be slaved together to provide the waveforms shown.

TEST PARAMETERS		
SYMBOL	VALUE	UNIT
$t_{sd}$	20	ns max
$t_{sd+}$	20	ns max

NOTE:

Connections shown for measuring times related to SET terminal only. To measure times at RESET terminals, apply the input pulse to Pin 13.

VOLTAGE WAVEFORMS AND DEFINITIONS

