

K4E171611D, K4E151611D K4E171612D, K4E151612D

CMOS DRAM

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

• Part Identification

- K4E171611D-J(T) (5V, 4K Ref.)
- K4E151611D-J(T) (5V, 1K Ref.)
- K4E171612D-J(T) (3.3V, 4K Ref.)
- K4E151612D-J(T) (3.3V, 1K Ref.)

• Active Power Dissipation

Unit : mW

| Speed | 3.3V | | 5V | |
|-------|------|-----|-----|-----|
| | 4K | 1K | 4K | 1K |
| -45 | 360 | 540 | 550 | 825 |
| -50 | 324 | 504 | 495 | 770 |
| -60 | 288 | 468 | 440 | 715 |

• Refresh Cycles

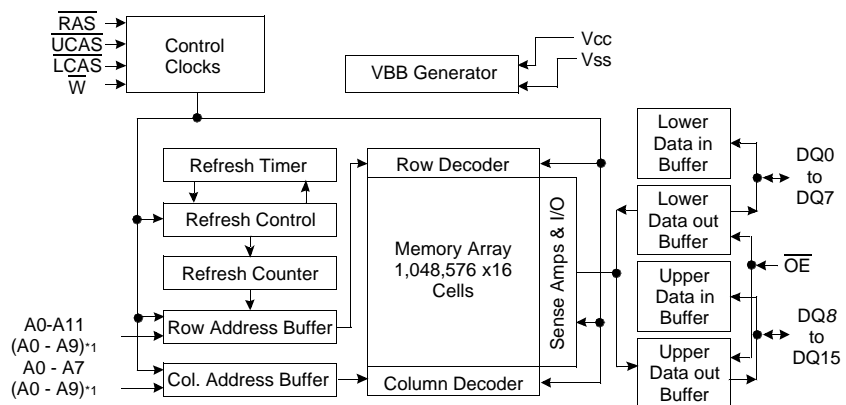
| Part NO. | V _{CC} | Refresh cycle | Refresh period | |
|------------|-----------------|---------------|----------------|-------|
| | | | Nor- | L-ver |
| K4E171611D | 5V | 4K | 64ms | 128ms |
| K4E171612D | 3.3V | | | |
| K4E151611D | 5V | 1K | 16ms | |
| K4E151612D | 3.3V | | | |

• Performance Range

| Speed | t _{RAC} | t _{CAC} | t _{RC} | t _{HPC} | Remark |
|-------|------------------|------------------|-----------------|------------------|---------|
| -45 | 45ns | 13ns | 69ns | 16ns | 5V/3.3V |
| -50 | 50ns | 15ns | 84ns | 20ns | 5V/3.3V |
| -60 | 60ns | 17ns | 104ns | 25ns | 5V/3.3V |

- Extended Data Out Mode operation (Fast Page Mode with Extended Data Out)
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in plastic SOJ 400mil and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

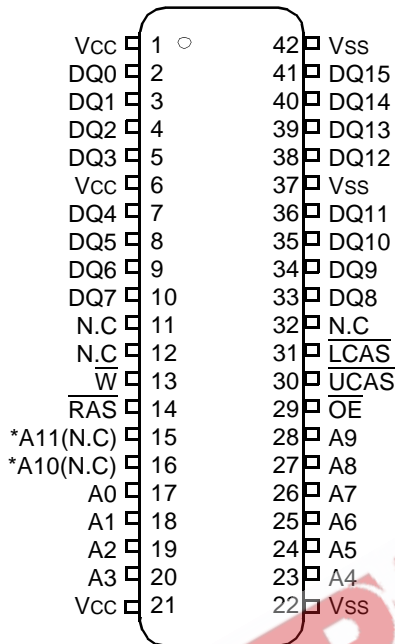


Note) *1: 1K Refresh

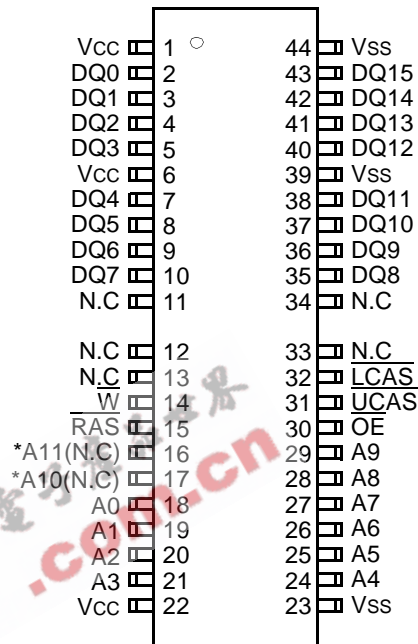
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PIN CONFIGURATION (Top Views)

• K4E17(5)1611(2)D-J



• K4E17(5)1611(2)D-T



*A10 and A11 are N.C for K4E151611(2)D(5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ

T : 400mil 50(44) TSOP II

| Pin Name | Pin Function |
|-------------------|-----------------------------|
| A0 - A11 | Address Inputs (4K Product) |
| A0 - A9 | Address Inputs (1K Product) |
| DQ0 - 15 | Data In/Out |
| Vss | Ground |
| \overline{RAS} | Row Address Strobe |
| \overline{UCAS} | Upper Column Address Strobe |
| \overline{LCAS} | Lower Column Address Strobe |
| \overline{W} | Read/Write Input |
| \overline{OE} | Data Output Enable |
| Vcc | Power(+5V) |
| | Power(+3.3V) |
| N.C | No Connection |

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ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Units |
|---------------------------------------|------------------------------------|--------------|--------------|-------|
| | | 3.3V | 5V | |
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -0.5 to +4.6 | -1.0 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | Vcc | -0.5 to +4.6 | -1.0 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +150 | -55 to +150 | °C |
| Power Dissipation | P _D | 1 | 1 | W |
| Short Circuit Output Current | I _{os} Address | 50 | 50 | mA |

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA= 0 to 70°C)

| Parameter | Symbol | 3.3V | | | 5V | | | Units |
|--------------------|-----------------|--------------------|-----|-----------------------|--------------------|-----|-----------------------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Voltage | Vcc | 3.0 | 3.3 | 3.6 | 4.5 | 5.0 | 5.5 | V |
| Ground | Vss | 0 | 0 | 0 | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.0 | - | Vcc+0.3* ¹ | 2.4 | - | Vcc+1.0* ¹ | V |
| Input Low Voltage | V _{IL} | -0.3* ² | - | 0.8 | -1.0* ² | - | 0.8 | V |

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

| Max | Parameter | Symbol | Min | Max | Units |
|------|--|-------------------|-----|-----|-------|
| 3.3V | Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.3V, all other input pins not under test=0 Volt) | I _{I(L)} | -5 | 5 | uA |
| | Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤Vcc) | I _{O(L)} | -5 | 5 | uA |
| | Output High Voltage Level(I _{OH} =-2mA) | V _{OH} | 2.4 | - | V |
| | Output Low Voltage Level(I _{OL} =2mA) | V _{OL} | - | 0.4 | V |
| 5V | Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt) | I _{I(L)} | -5 | 5 | uA |
| | Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤Vcc) | I _{O(L)} | -5 | 5 | uA |
| | Output High Voltage Level(I _{OH} =-5mA) | V _{OH} | 2.4 | - | V |
| | Output Low Voltage Level(I _{OL} =4.2mA) | V _{OL} | - | 0.4 | V |

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DC AND OPERATING CHARACTERISTICS (Continued)

| Symbol | Power | Speed | Max | | | | Units |
|------------------|-------------|------------|------------|------------|------------|------------|-------|
| | | | K4E171612D | K4E151612D | K4E171611D | K4E151611D | |
| I _{CC1} | Don't care | -45 | 100 | 150 | 100 | 150 | mA |
| | | -50 | 90 | 140 | 90 | 140 | mA |
| | | -60 | 80 | 130 | 80 | 130 | mA |
| I _{CC2} | Normal L | Don't care | 1 | 1 | 2 | 2 | mA |
| | | | 1 | 1 | 1 | 1 | mA |
| I _{CC3} | Don't care | -45 | 100 | 150 | 100 | 150 | mA |
| | | -50 | 90 | 140 | 90 | 140 | mA |
| | | -60 | 80 | 130 | 80 | 130 | mA |
| I _{CC4} | Don't care | -45 | 110 | 110 | 110 | 110 | mA |
| | | -50 | 100 | 100 | 100 | 100 | mA |
| | | -60 | 90 | 90 | 90 | 90 | mA |
| I _{CC5} | Normal L | Don't care | 0.5 | 0.5 | 1 | 1 | mA |
| | | | 200 | 200 | 200 | 200 | uA |
| I _{CC6} | Don't care | -45 | 100 | 150 | 110 | 150 | mA |
| | | -50 | 90 | 140 | 90 | 140 | mA |
| | | -60 | 80 | 130 | 80 | 130 | mA |
| I _{CC7} | L | Don't care | 300 | 200 | 350 | 250 | uA |
| I _{CC8} | L | Don't care | 150 | 150 | 200 | 200 | uA |

I_{CC1}* : Operating Current (\overline{RAS} and \overline{UCAS} , \overline{LCAS} , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address cycling @t_{RC}=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} , \overline{UCAS} or \overline{LCAS} cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, \overline{UCAS} , \overline{LCAS} =0.2V,

DQ=Don't care, T_{RC}=31.25us(4K/L-ver), 125us(1K/L-ver)

T_{RAS}=T_{ASmin}~300ns

I_{CC8} : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A11=V_{CC}-0.2V$ or 0.2V,

DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

*Note : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, t_{HPC}.

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CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

| Parameter | Symbol | Min | Max | Units |
|--|--------|-----|-----|-------|
| Input capacitance [A0 ~ A11] | CIN1 | - | 5 | pF |
| Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$] | CIN2 | - | 7 | pF |
| Output capacitance [DQ0 - DQ15] | CDQ | - | 7 | pF |

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V

Test condition (3.3V device) : VCC=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

| Parameter | Symbol | -45 | | -50 | | -60 | | Units | Notes |
|---|--------|----------|--------|-----|-----|-----|-----|-------|--------|
| | | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 79 | | 84 | | 104 | | ns | |
| Read-modify-write cycle time | tRWC | 105 | | 115 | | 140 | | ns | |
| Access time from $\overline{\text{RAS}}$ | tRAC | | 45 | | 50 | | 60 | ns | 3,4,10 |
| Access time from $\overline{\text{CAS}}$ | tCAC | | 14 | | 15 | | 17 | ns | 3,4,5 |
| Access time from column address | tAA | | 23/*20 | | 25 | | 30 | ns | 3,10 |
| $\overline{\text{CAS}}$ to output in Low-Z | tCLZ | 3 | | 3 | | 3 | | ns | 3 |
| Output buffer turn-off delay from $\overline{\text{CAS}}$ | tCEZ | 3 | 13 | 3 | 13 | 3 | 15 | ns | 6,19 |
| $\overline{\text{OE}}$ to output in Low-Z | tOLZ | 3 | | 3 | | 3 | | ns | 3 |
| Transition time (rise and fall) | tT | 2 | 50 | 2 | 50 | 2 | 50 | ns | 2 |
| $\overline{\text{RAS}}$ precharge time | tRP | 30 | | 30 | | 40 | | ns | |
| $\overline{\text{RAS}}$ pulse width | tRAS | 45 | 10K | 50 | 10K | 60 | 10K | ns | |
| $\overline{\text{RAS}}$ hold time | tRSH | 13 | | 13 | | 17 | | ns | |
| $\overline{\text{CAS}}$ hold time | tCSH | 36 | | 40 | | 50 | | ns | |
| $\overline{\text{CAS}}$ pulse width | tCAS | 7 / *6.5 | 10K | 8 | 10K | 10 | 10K | ns | 18 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | tRCD | 19 | 31 | 20 | 35 | 20 | 43 | ns | 4 |
| $\overline{\text{RAS}}$ to column address delay time | tRAD | 14 | 22 | 15 | 25 | 15 | 30 | ns | 10 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | tCRP | 5 | | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 9 | | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | 0 | | ns | 11 |
| Column address hold time | tCAH | 7 | | 8 | | 10 | | ns | 11 |
| Column address to $\overline{\text{RAS}}$ lead time | tRAL | 23 | | 25 | | 30 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{\text{CAS}}$ | tRCH | 0 | | 0 | | 0 | | ns | 8 |
| Read command hold time referenced to $\overline{\text{RAS}}$ | tRRH | 0 | | 0 | | 0 | | ns | 8 |
| Write command hold time | tWCH | 8 | | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 8 | | 10 | | 10 | | ns | |
| Write command to $\overline{\text{RAS}}$ lead time | tRWL | 10 | | 13 | | 15 | | ns | |
| Write command to $\overline{\text{CAS}}$ lead time | tCWL | 7 | | 8 | | 10 | | ns | 14 |

* KM416C1204DT-45 (5V, 1K Refresh) only

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AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -45 | | -50 | | -60 | | Units | Notes |
|--|--------|----------|------|-----|------|-----|------|-------|----------|
| | | Min | Max | Min | Max | Min | Max | | |
| Data set-up time | tDS | 0 | | 0 | | 0 | | ns | 9,17 |
| Data hold time | tDH | 7 | | 8 | | 10 | | ns | 9,17 |
| Refresh period (1K, Normal) | tREF | | 16 | | 16 | | 16 | ms | |
| Refresh period (4K, Normal) | tREF | | 64 | | 64 | | 64 | ms | |
| Refresh period (L-ver) | tREF | | 128 | | 128 | | 128 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | 0 | | ns | 7 |
| $\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time | tCWD | 28 | | 32 | | 36 | | ns | 7,13 |
| $\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time | tRWD | 59 | | 67 | | 79 | | ns | 7 |
| Column address $\overline{\text{W}}$ delay time | tAWD | 37 | | 42 | | 49 | | ns | 7 |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time | tCPWD | 39 | | 47 | | 54 | | ns | 7 |
| $\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | tCSR | 5 | | 5 | | 5 | | ns | 15 |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) | tCHR | 10 | | 10 | | 10 | | ns | 16 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time | tRPC | 5 | | 5 | | 5 | | ns | |
| Access time from $\overline{\text{CAS}}$ precharge | tCPA | | 25 | | 28 | | 35 | ns | 3 |
| Hyper Page mode cycle time | tHPC | 18 | | 20 | | 25 | | ns | 18 |
| Hyper Page read-modify-write cycle time | tHPRWC | 39 | | 47 | | 56 | | ns | 18 |
| $\overline{\text{CAS}}$ precharge time (Hyper Page cycle) | tCP | 7 / *6.5 | | 8 | | 10 | | ns | 12 |
| $\overline{\text{RAS}}$ pulse width (Hyper Page cycle) | tRASP | 45 | 200K | 50 | 200K | 60 | 200K | ns | |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge | tRHCP | 27 | | 30 | | 35 | | ns | |
| $\overline{\text{OE}}$ access time | tOEA | | 13 | | 13 | | 15 | ns | 3 |
| $\overline{\text{OE}}$ to data delay | tOED | 10 | | 13 | | 15 | | ns | |
| Output buffer turn off delay time from $\overline{\text{OE}}$ | tOEZ | 3 | 13 | 3 | 13 | 3 | 15 | ns | 6 |
| $\overline{\text{OE}}$ command hold time | tOEH | 10 | | 13 | | 15 | | ns | |
| Output data hold time | tDOH | 4 | | 5 | | 5 | | ns | |
| Output buffer turn off delay from $\overline{\text{RAS}}$ | tREZ | 3 | 13 | 3 | 13 | 3 | 15 | ns | 6,19 |
| Output buffer turn off delay from $\overline{\text{W}}$ | tWEZ | 3 | 13 | 3 | 13 | 3 | 15 | ns | 6 |
| $\overline{\text{W}}$ to data delay | tWED | 15 | | 15 | | 15 | | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time | tOCH | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$ | tCHO | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{OE}}$ precharge time | tOEP | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{W}}$ pulse width (Hyper Page Cycle) | tWPE | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh) | tRASS | 100 | | 100 | | 100 | | us | 20,21,22 |
| $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh) | tRPS | 79 | | 90 | | 110 | | ns | 20,21,22 |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh) | tCHS | -50 | | -50 | | -50 | | ns | 20,21,22 |

* KM416C1204DT-45 (5V, 1K Refresh) only

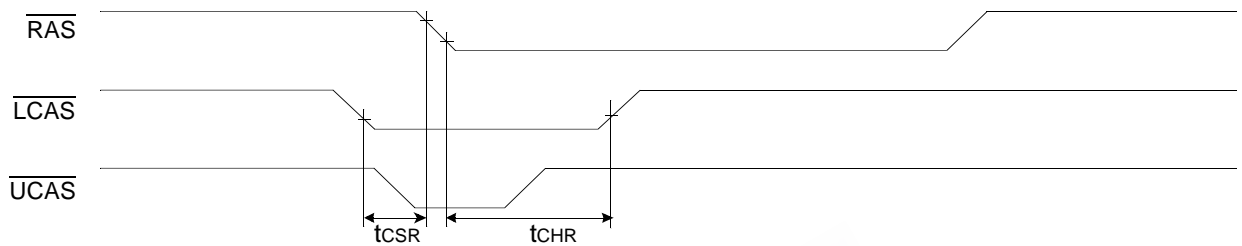
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{ih}(\text{min})$ and $V_{il}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

K4E17(5)1611(2)D Truth Table

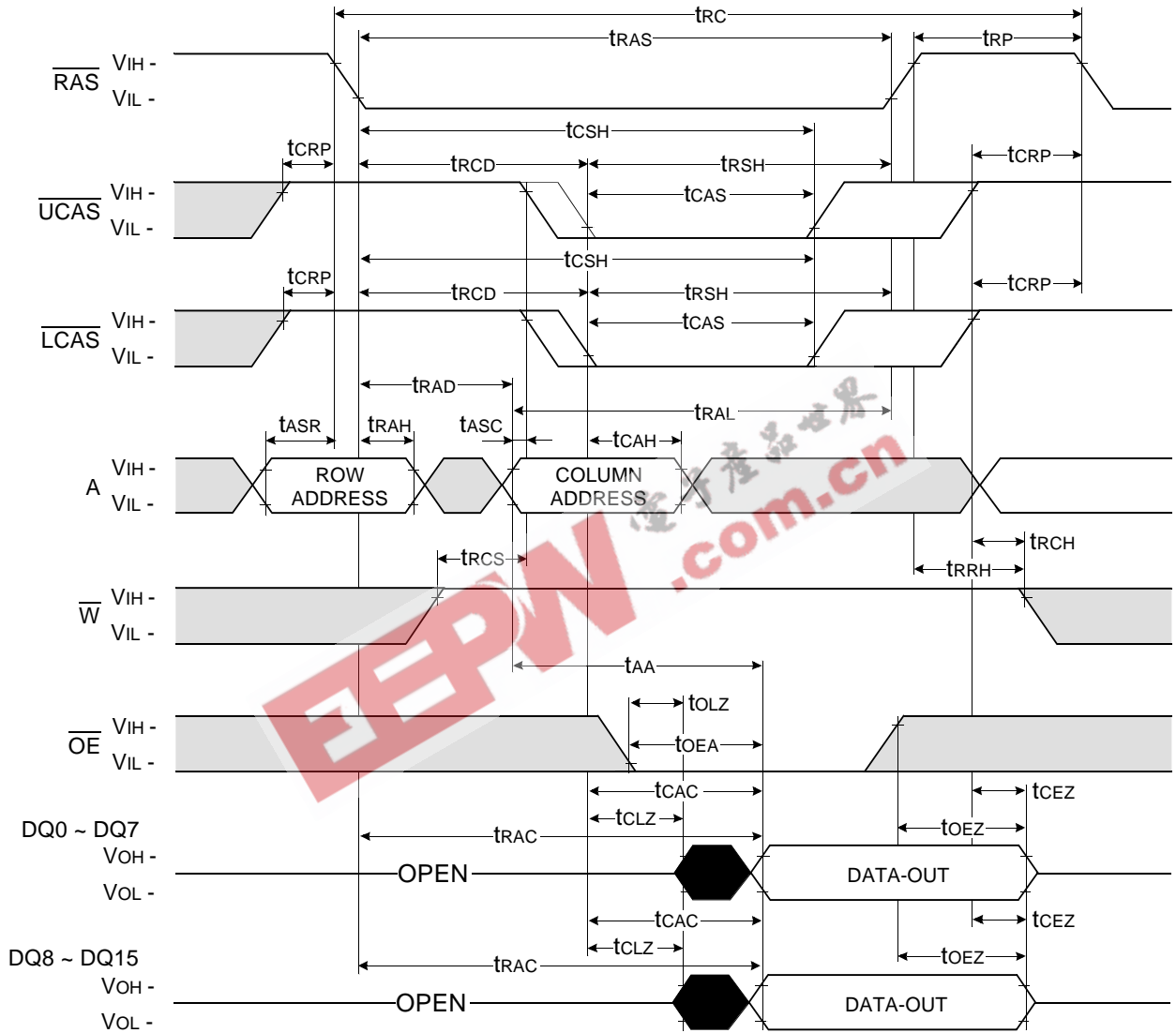
| RAS | LCAS | UCAS | W | OE | DQ0 - DQ7 | DQ8-DQ15 | STATE |
|------------|-------------|-------------|----------|-----------|------------------|-----------------|--------------|
| H | X | X | X | X | Hi-Z | Hi-Z | Standby |
| L | H | H | X | X | Hi-Z | Hi-Z | Refresh |
| L | L | H | H | L | DQ-OUT | Hi-Z | Byte Read |
| L | H | L | H | L | Hi-Z | DQ-OUT | Byte Read |
| L | L | L | H | L | DQ-OUT | DQ-OUT | Word Read |
| L | L | H | L | H | DQ-IN | - | Byte Write |
| L | H | L | L | H | - | DQ-IN | Byte Write |
| L | L | L | L | H | DQ-IN | DQ-IN | Word Write |
| L | L | L | H | H | Hi-Z | Hi-Z | - |

11. tASC, tCAH are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
12. tCP is specified from the later $\overline{\text{CAS}}$ rising edge in the previous cycle to the earlier $\overline{\text{CAS}}$ falling edge in the next cycle.
13. tCWD is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
14. tCWL is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.
15. tCSR is referenced to the earlier $\overline{\text{CAS}}$ falling edge before $\overline{\text{RAS}}$ transition low.
16. tCHR is referenced to the later $\overline{\text{CAS}}$ rising edge after $\overline{\text{RAS}}$ transition low.



17. tds, tDH is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).
18. tASC ≥ 6ns, assume tT = 2.0ns.
19. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going.
If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
20. If tRASS ≥ 100us, then $\overline{\text{RAS}}$ precharge time must use tRPS instead of tRP.
21. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 4096(4K)/1024(1K) cycles of burst refresh must be executed within 64ms/16ms before and after self refresh, in order to meet refresh specification.
22. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

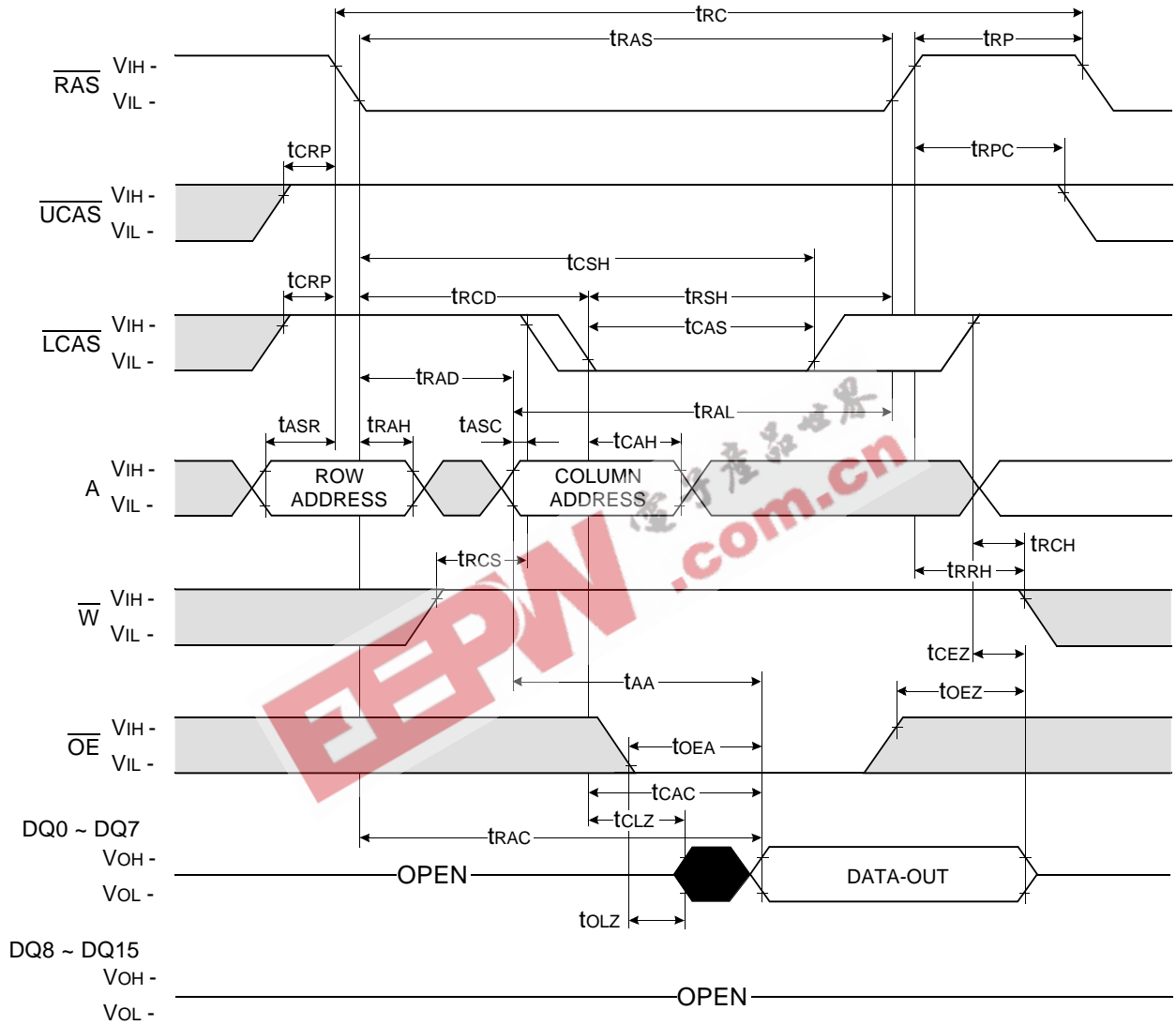
WORD READ CYCLE



Don't care
 Undefined

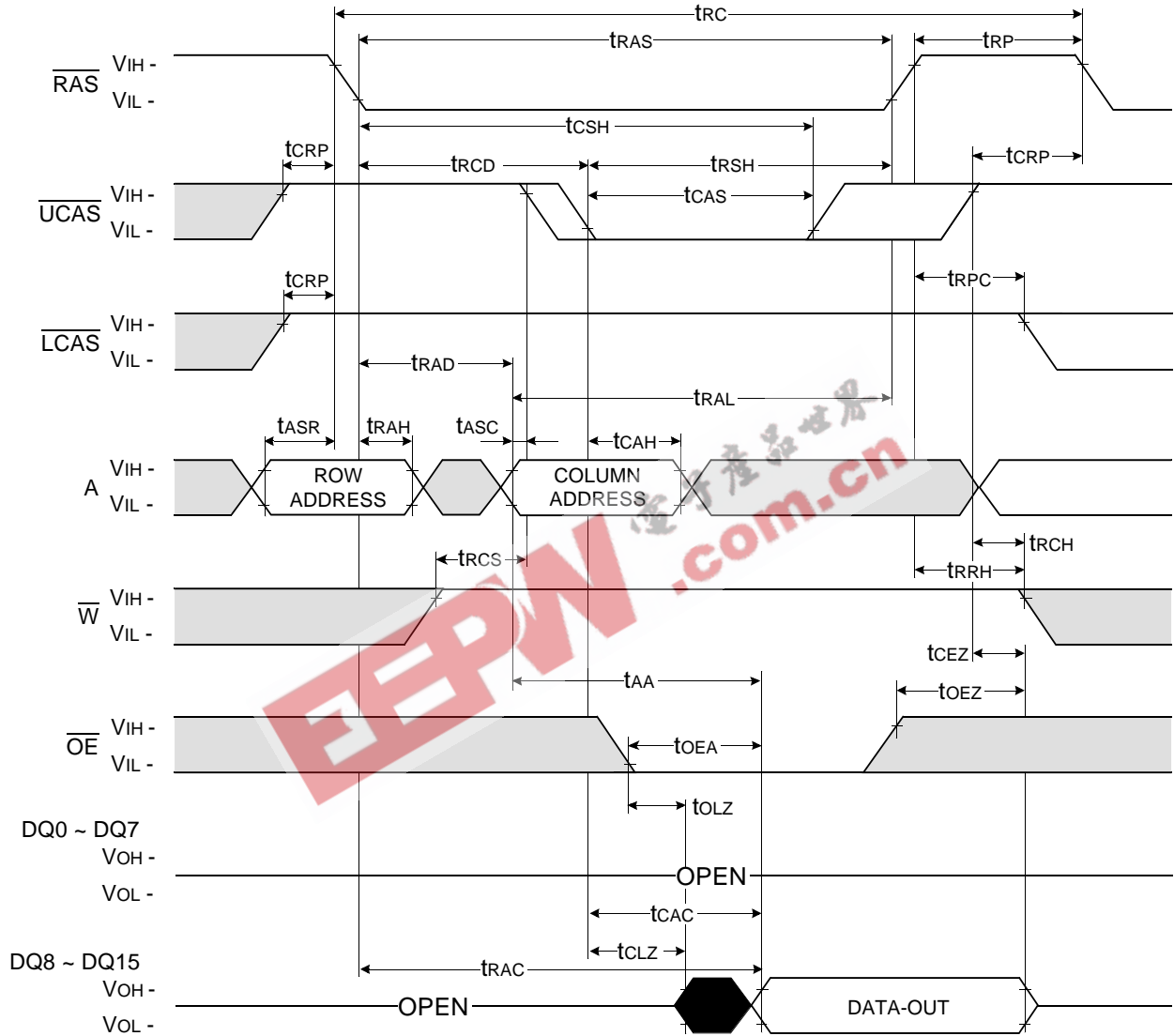
LOWER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN

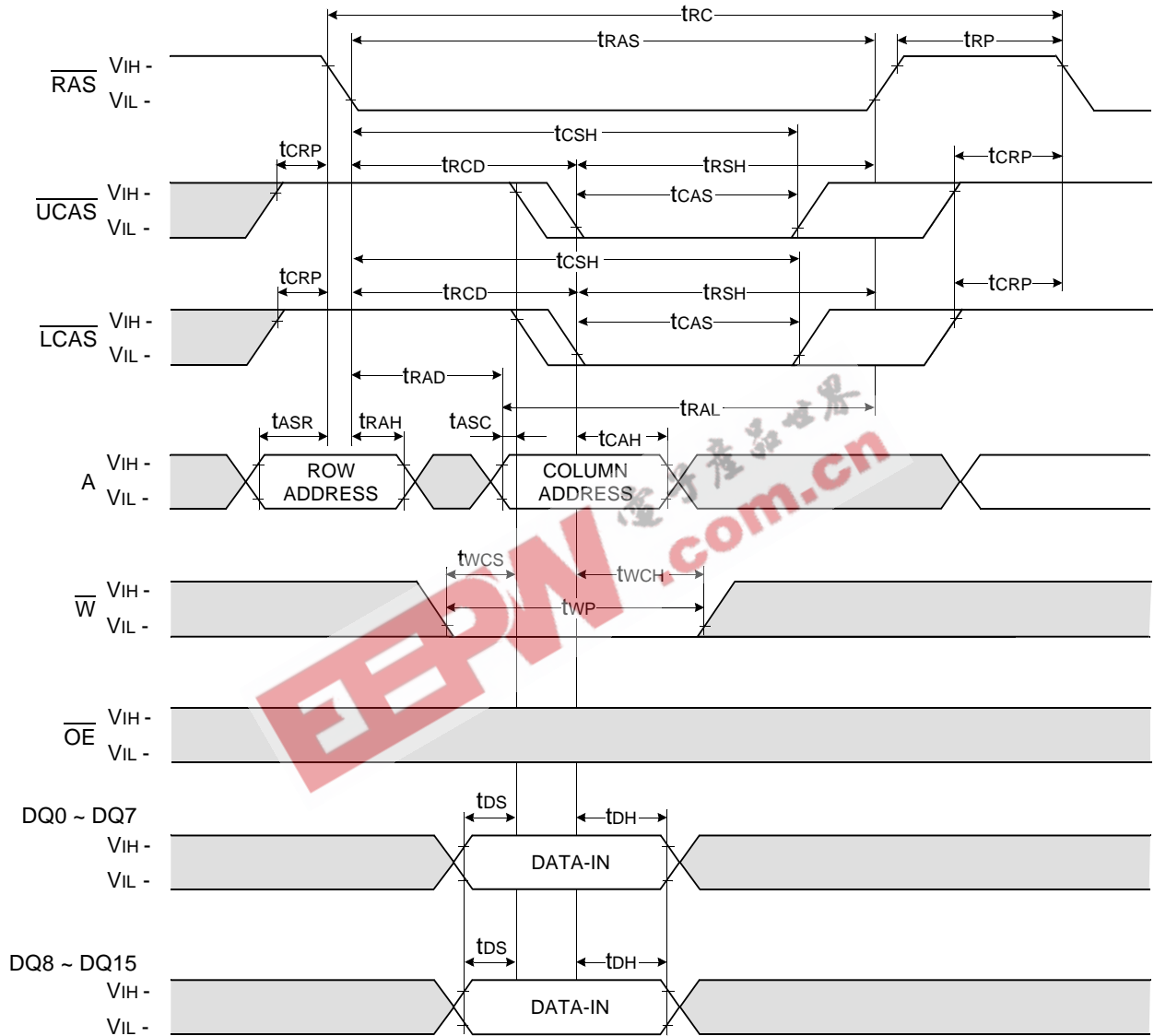


□ Don't care

■ Undefined

WORD WRITE CYCLE (EARLY WRITE)

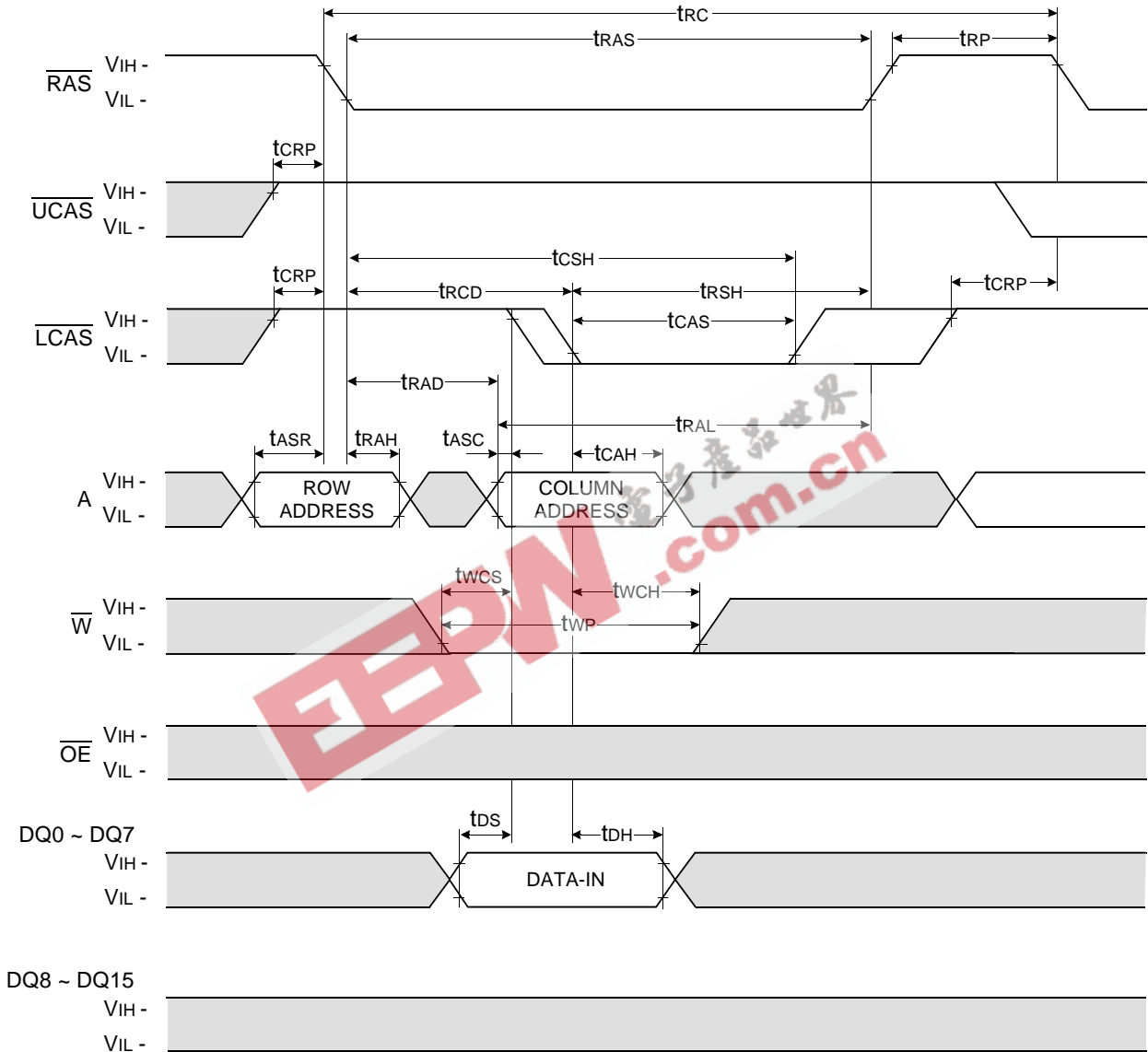
NOTE : DOUT = OPEN



□ Don't care
■ Undefined

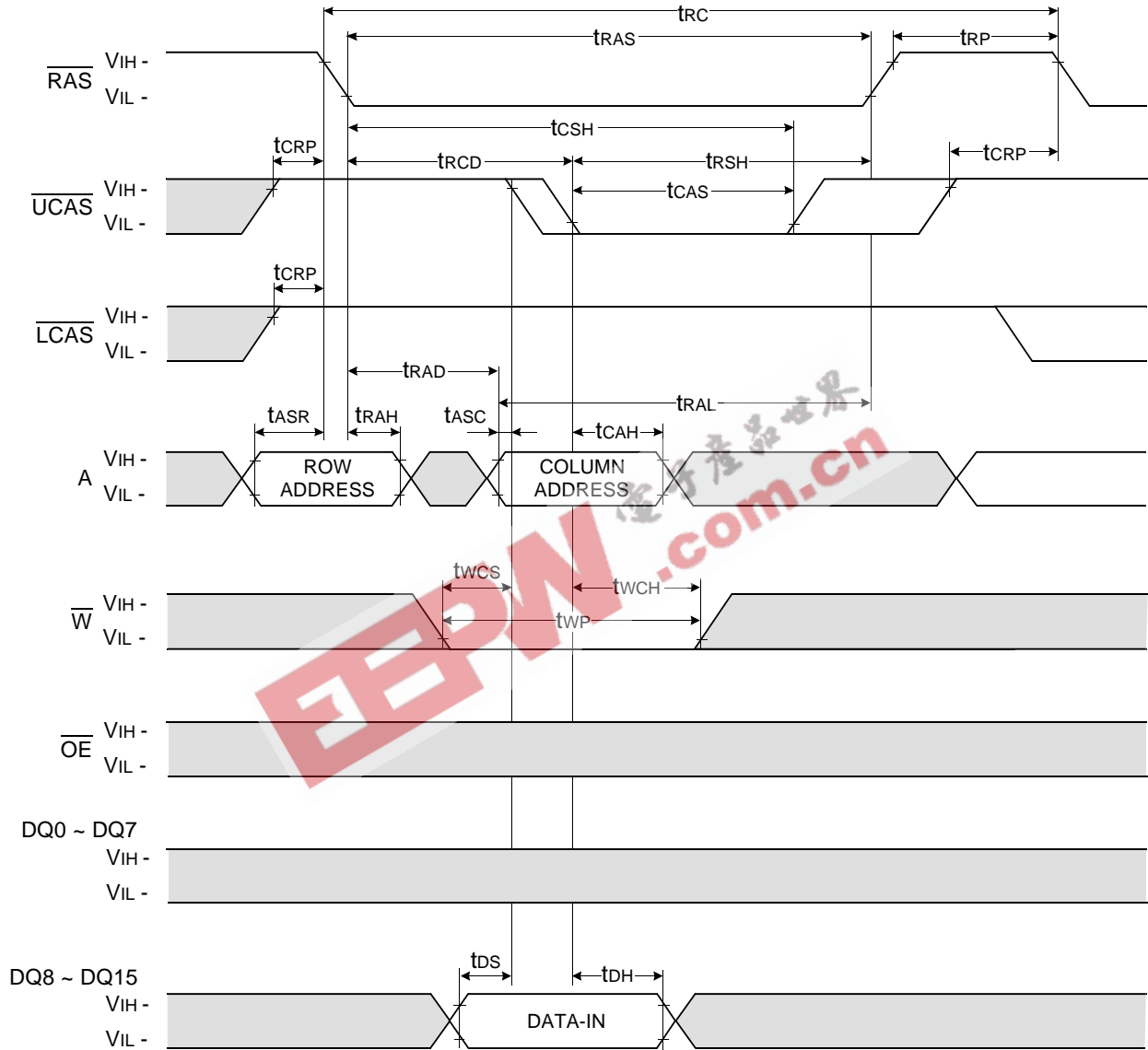
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



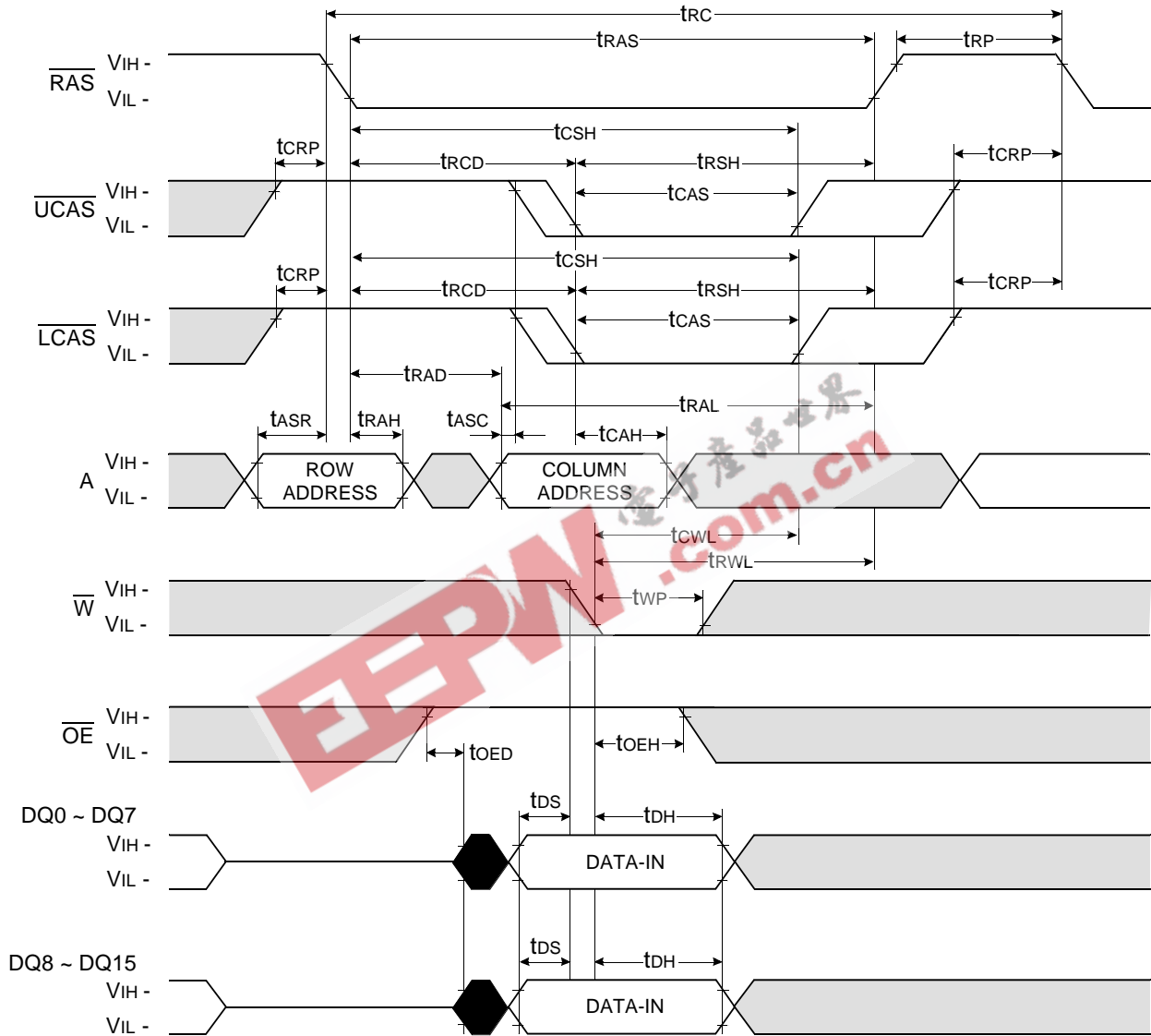
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



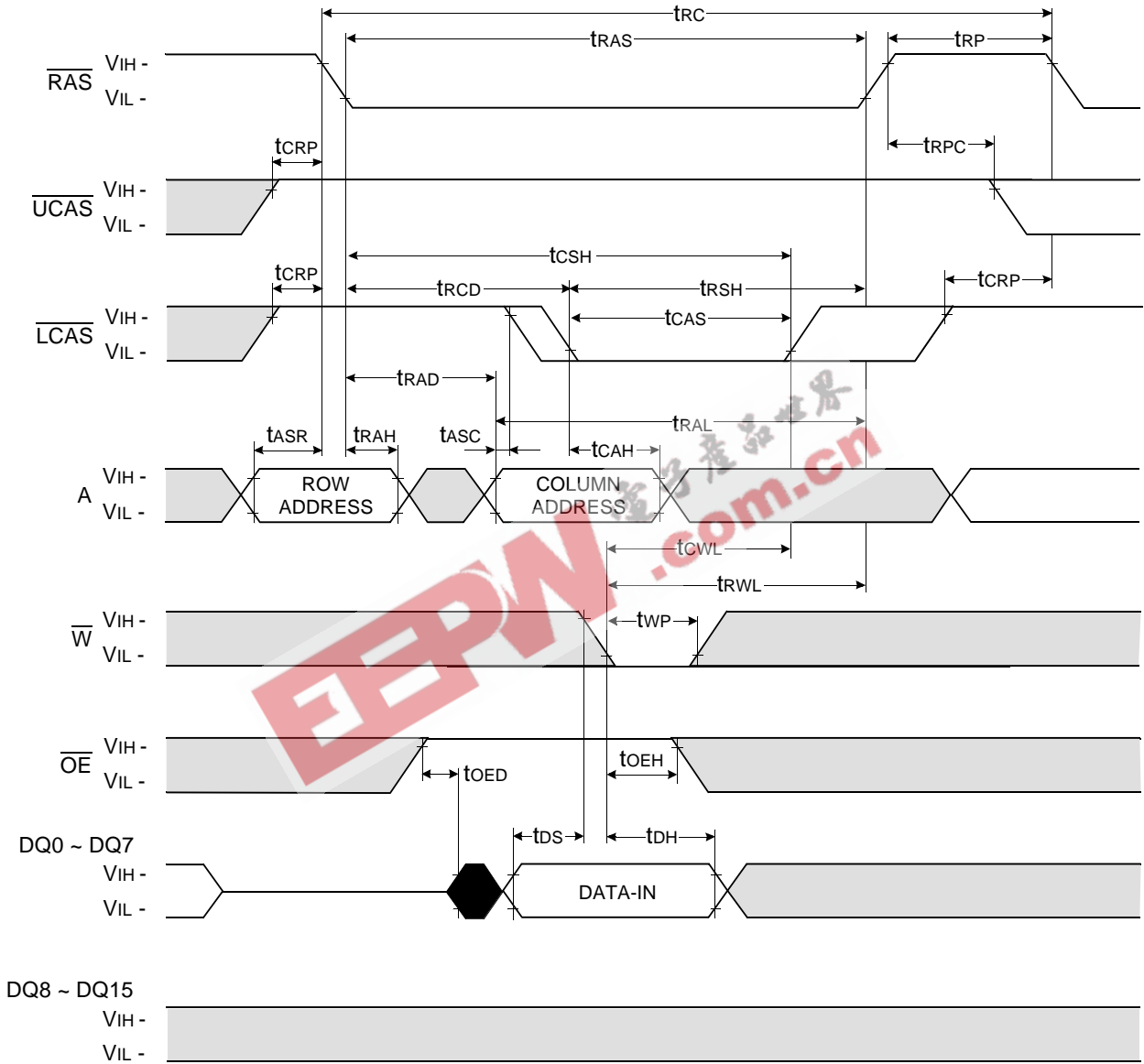
WORD WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

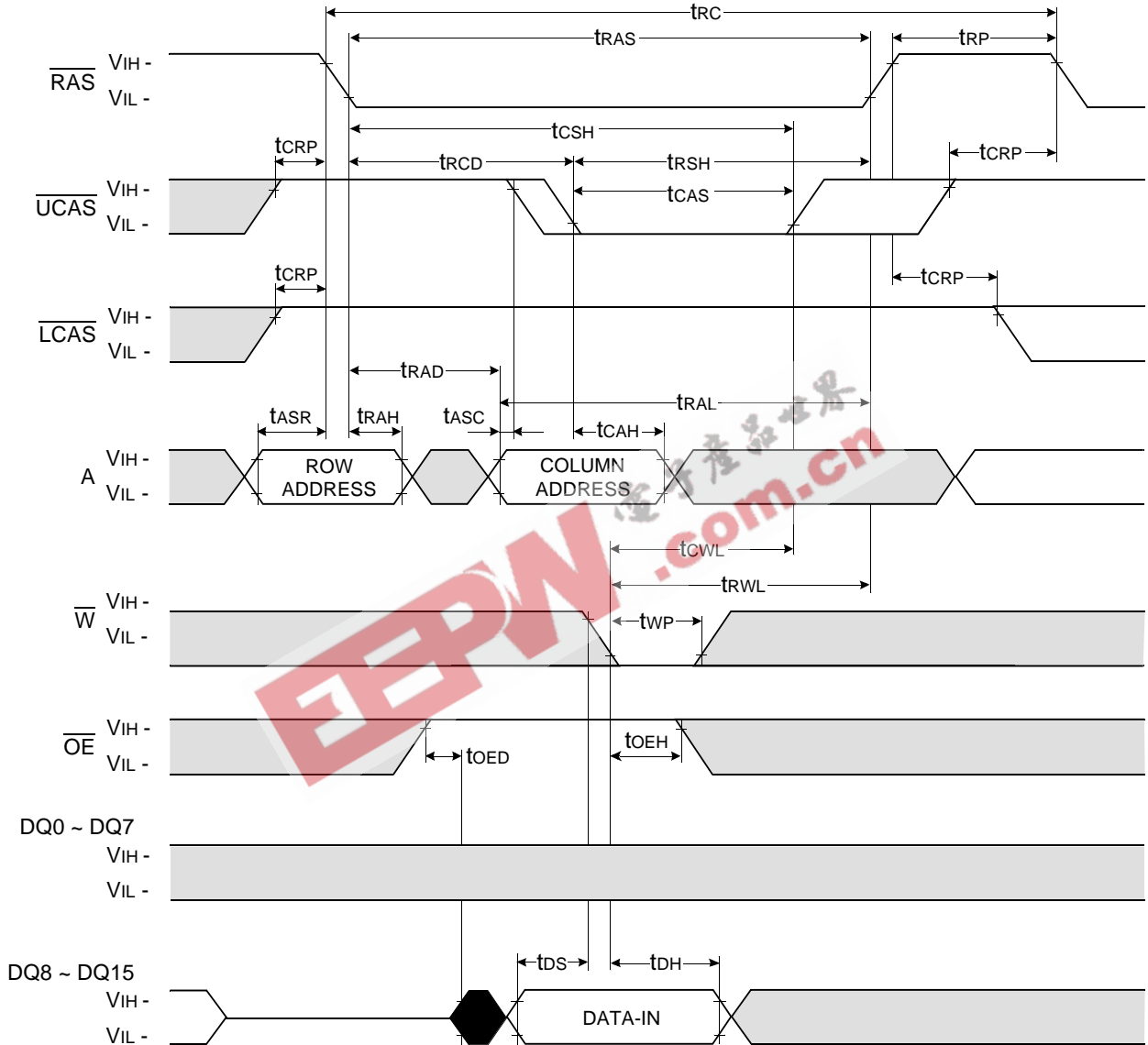
NOTE : DOUT = OPEN



□ Don't care
■ Undefined

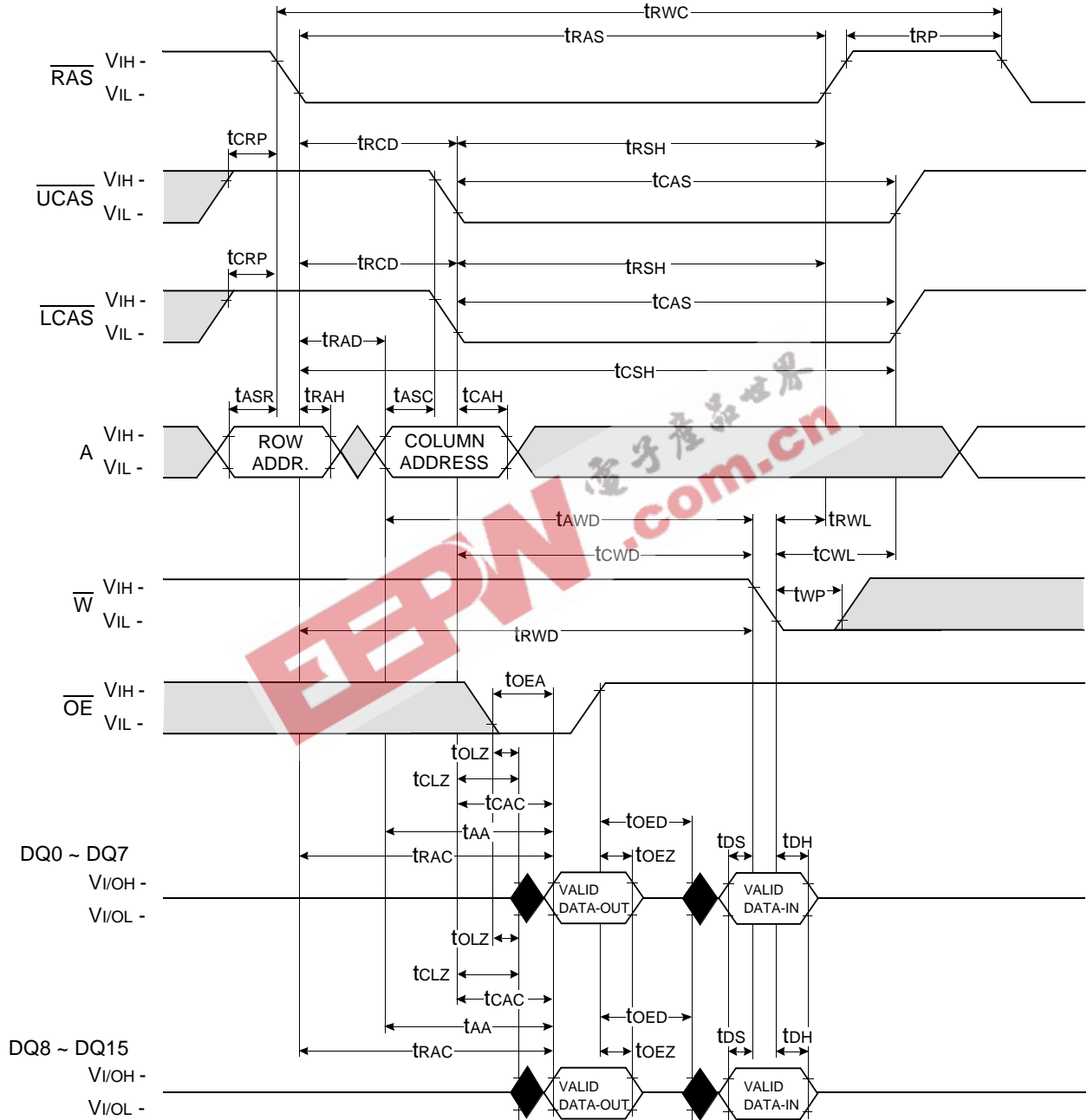
UPPER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



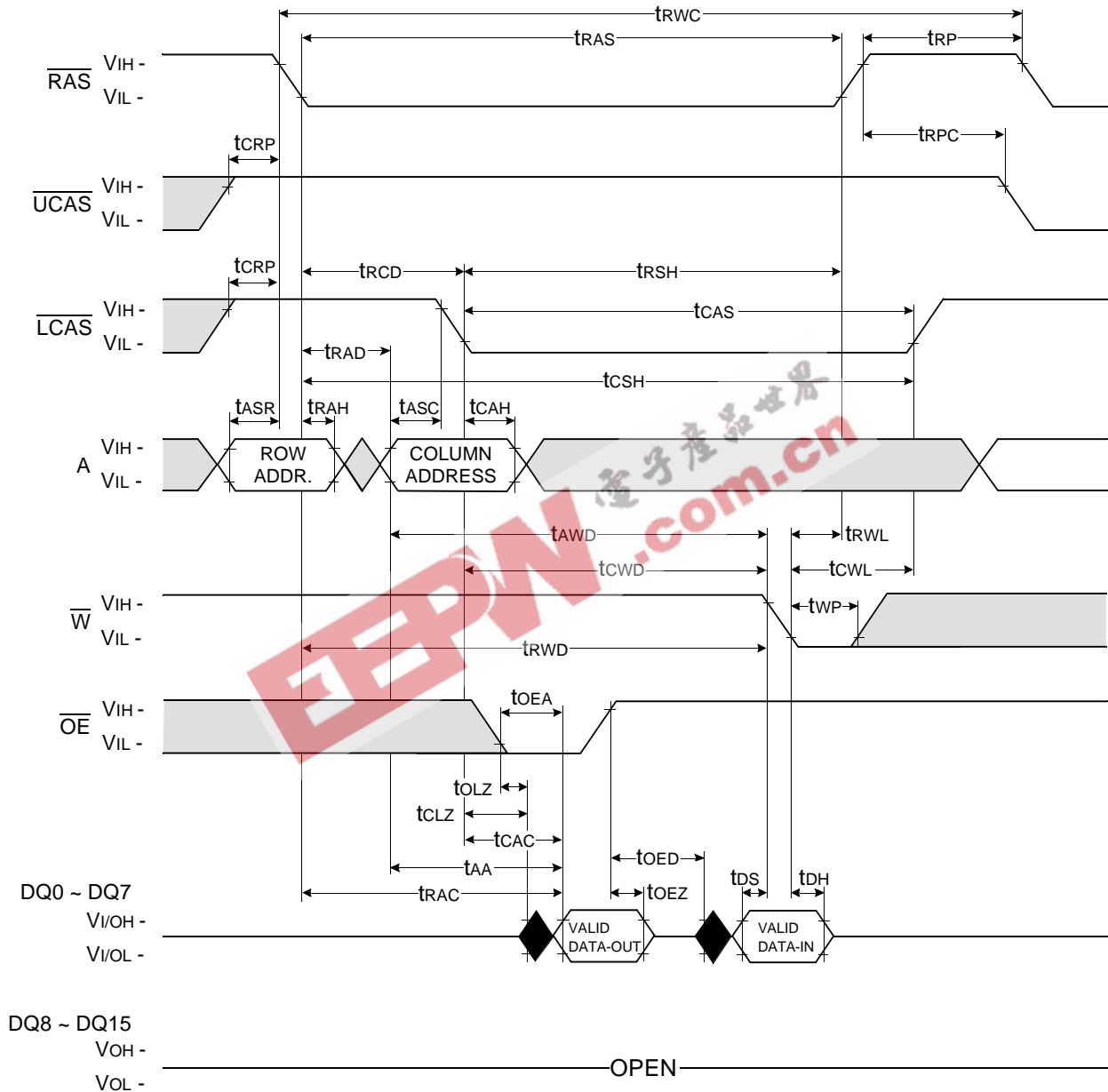
□ Don't care
 ■ Undefined

WORD READ - MODIFY - WRITE CYCLE



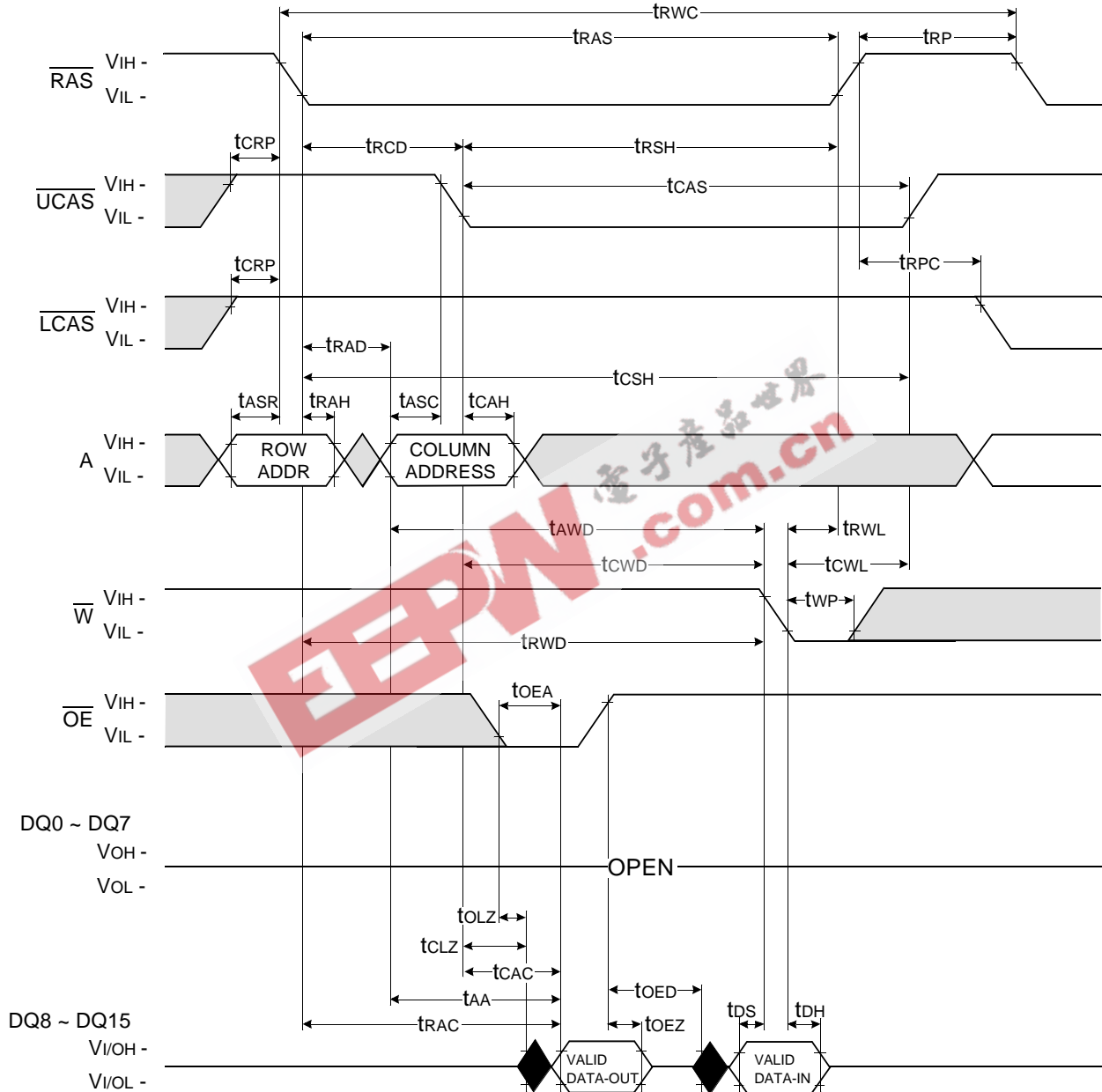
□ Don't care
■ Undefined

LOWER-BYTE READ - MODIFY - WRITE CYCLE



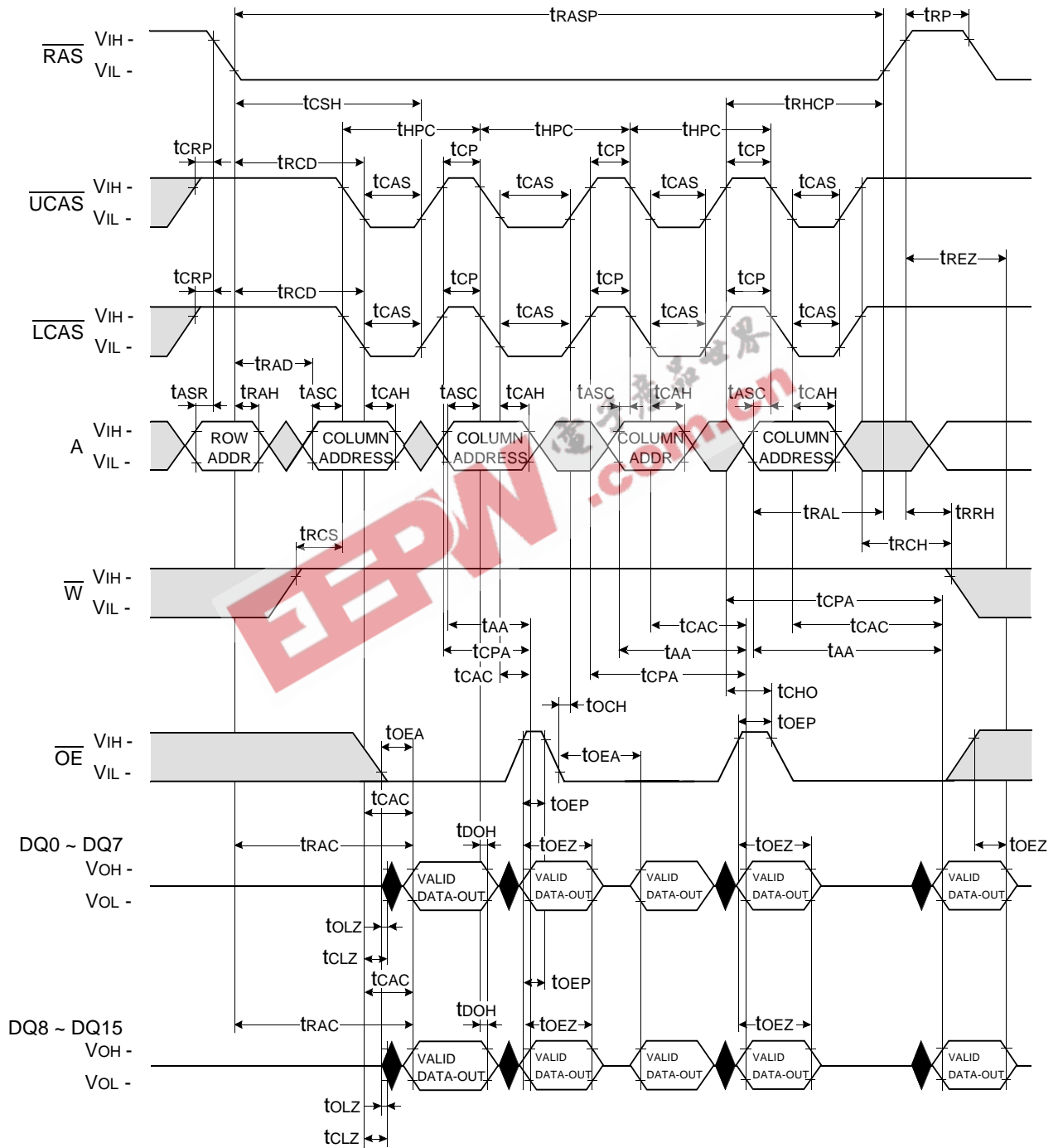
□ Don't care
■ Undefined

UPPER-BYTE READ - MODIFY - WRITE CYCLE



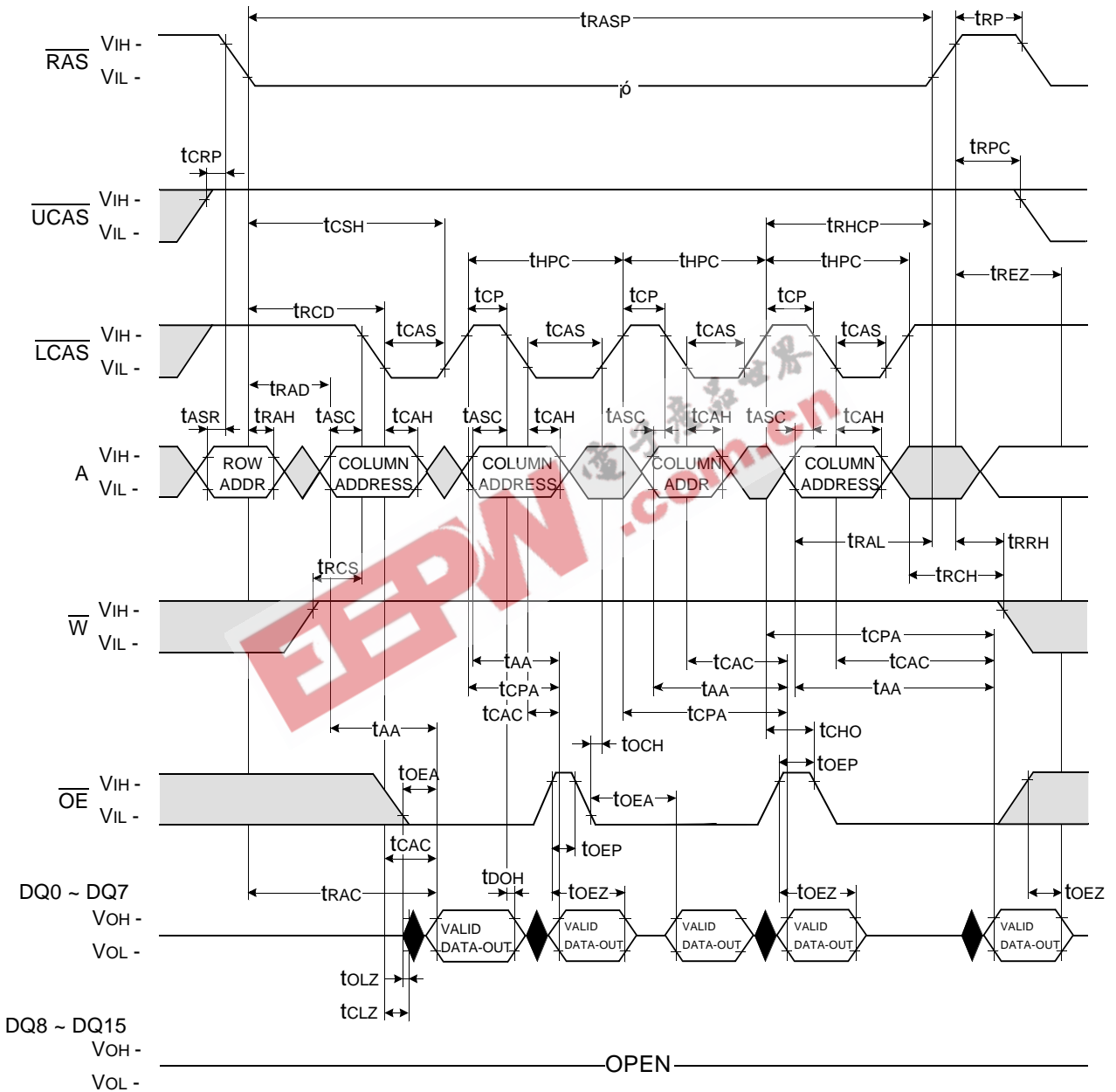
Don't care
 Undefined

HYPER PAGE MODE WORD READ CYCLE



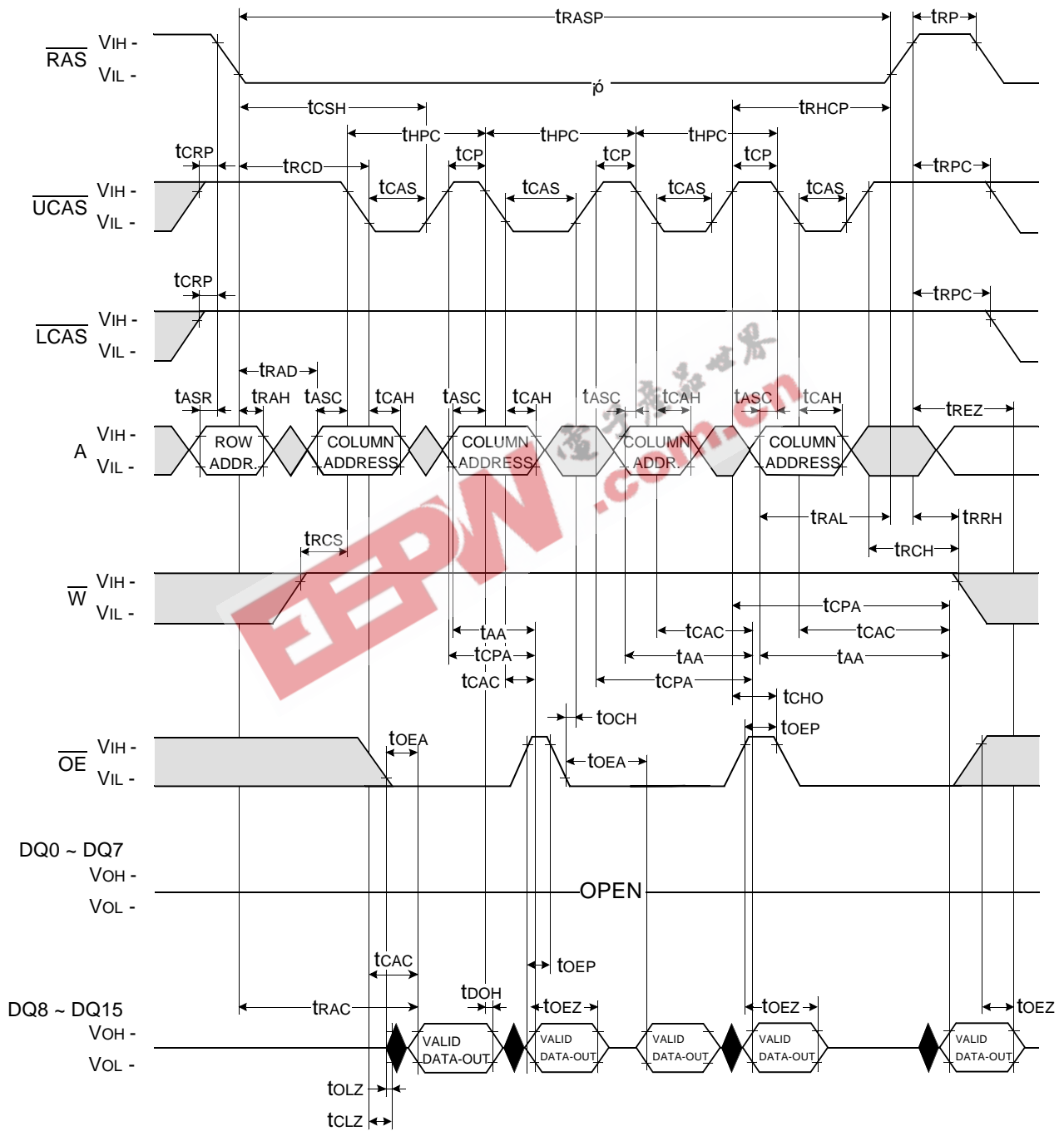
□ Don't care
 ■ Undefined

HYPER PAGE MODE LOWER BYTE READ CYCLE



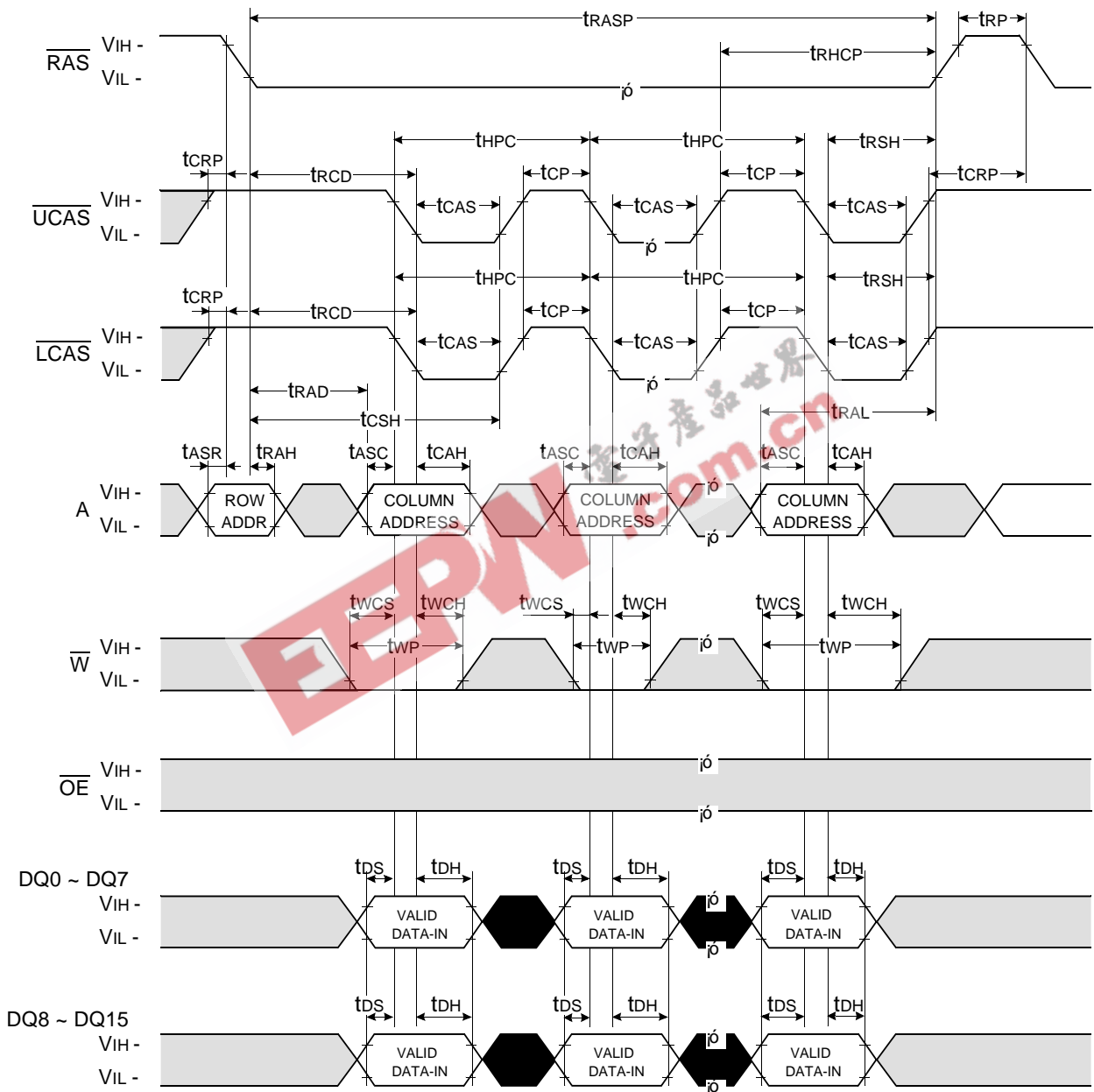
Don't care
 Undefined

HYPER PAGE MODE UPPER BYTE READ CYCLE



HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

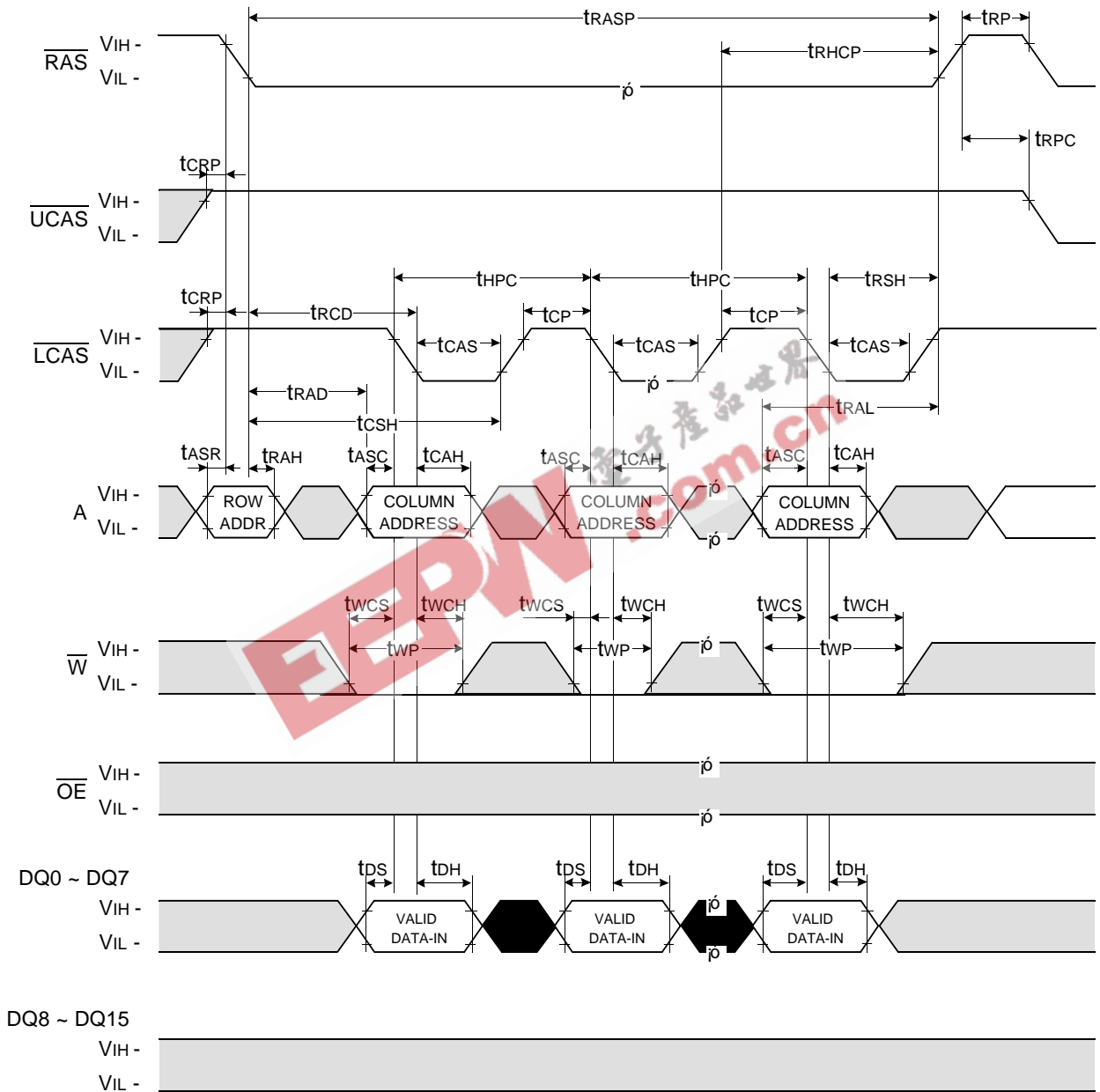
NOTE : DOUT = OPEN



□ Don't care
■ Undefined

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

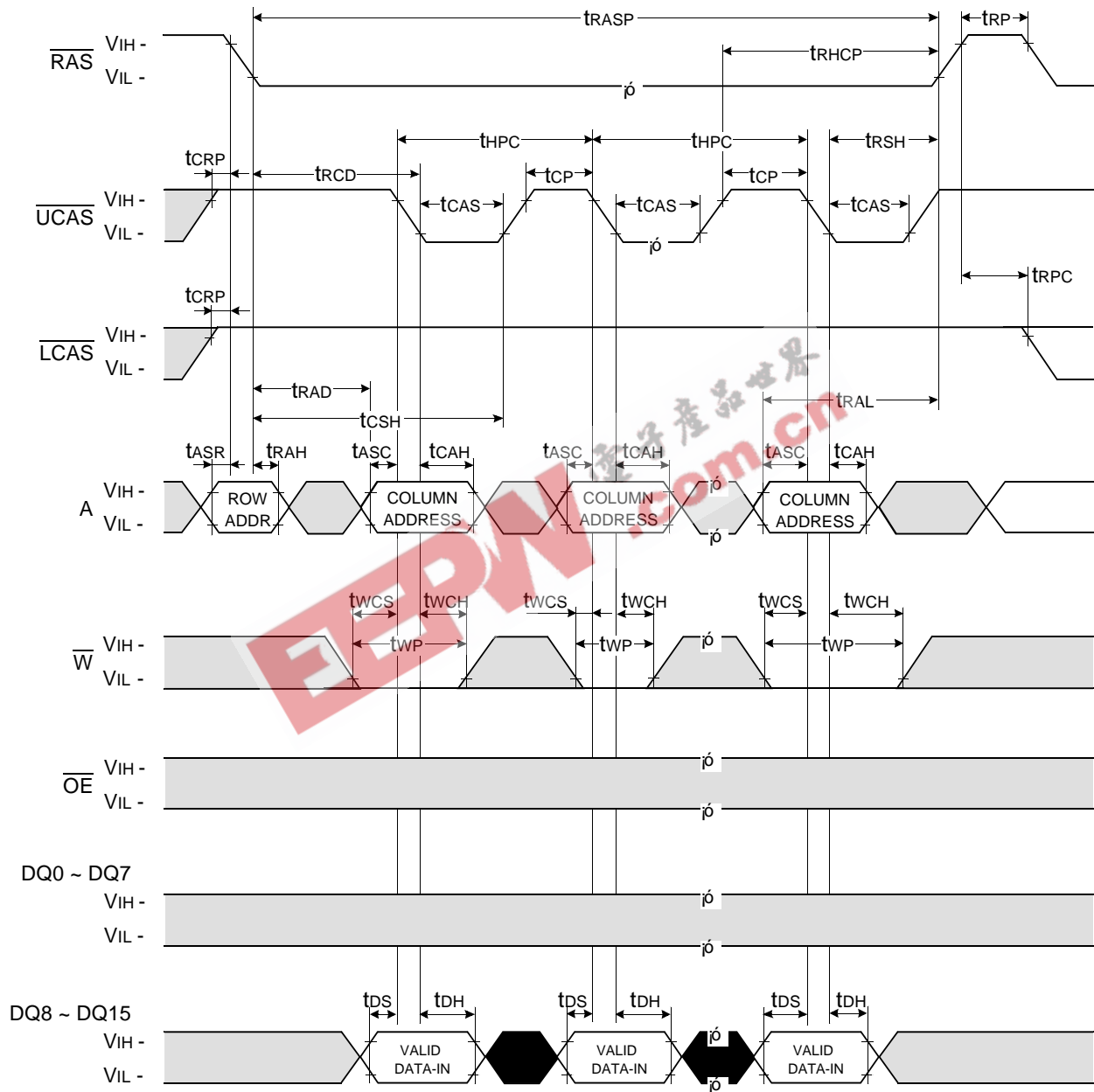


K4E171611D, K4E151611D K4E171612D, K4E151612D

CMOS DRAM

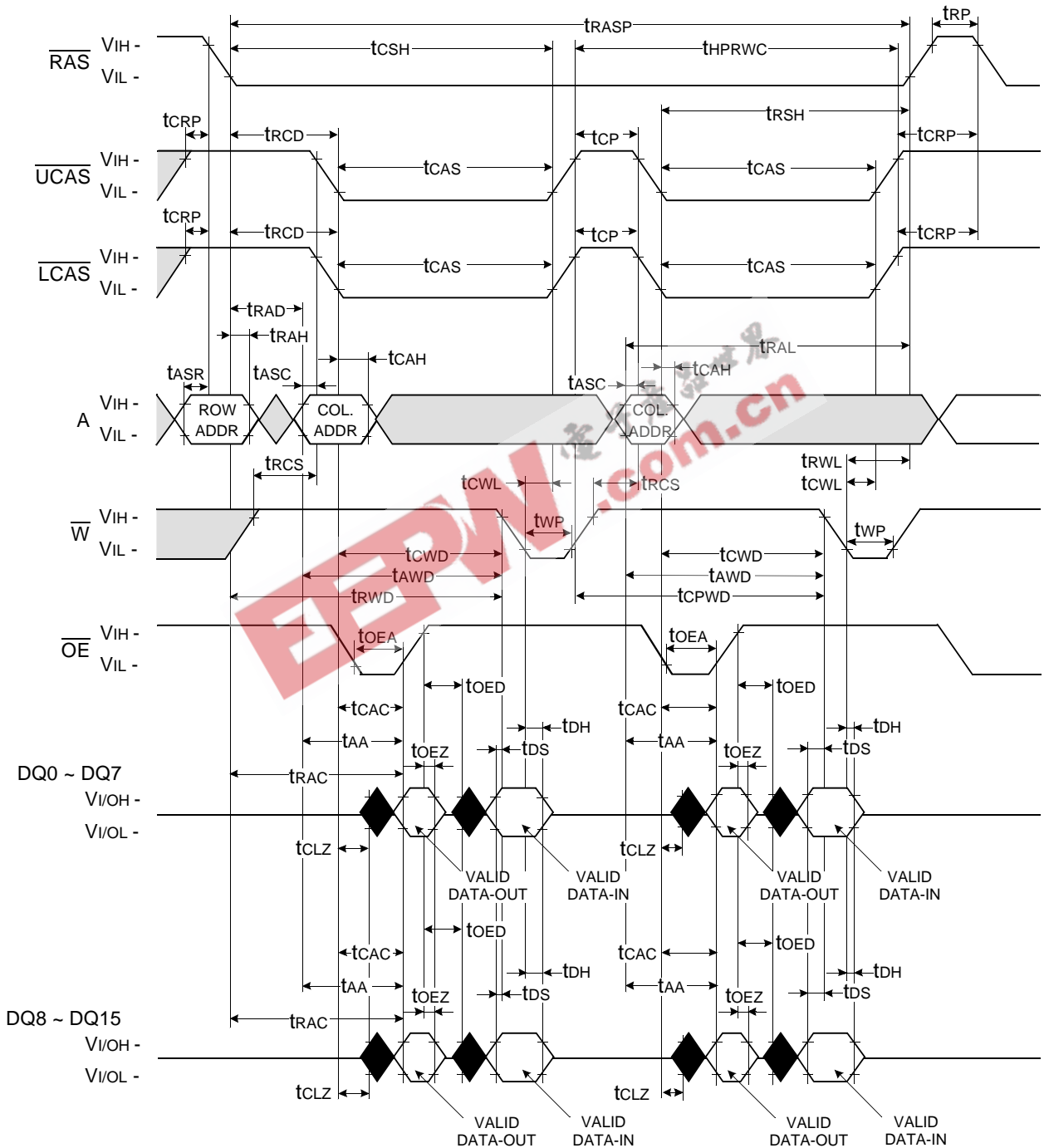
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



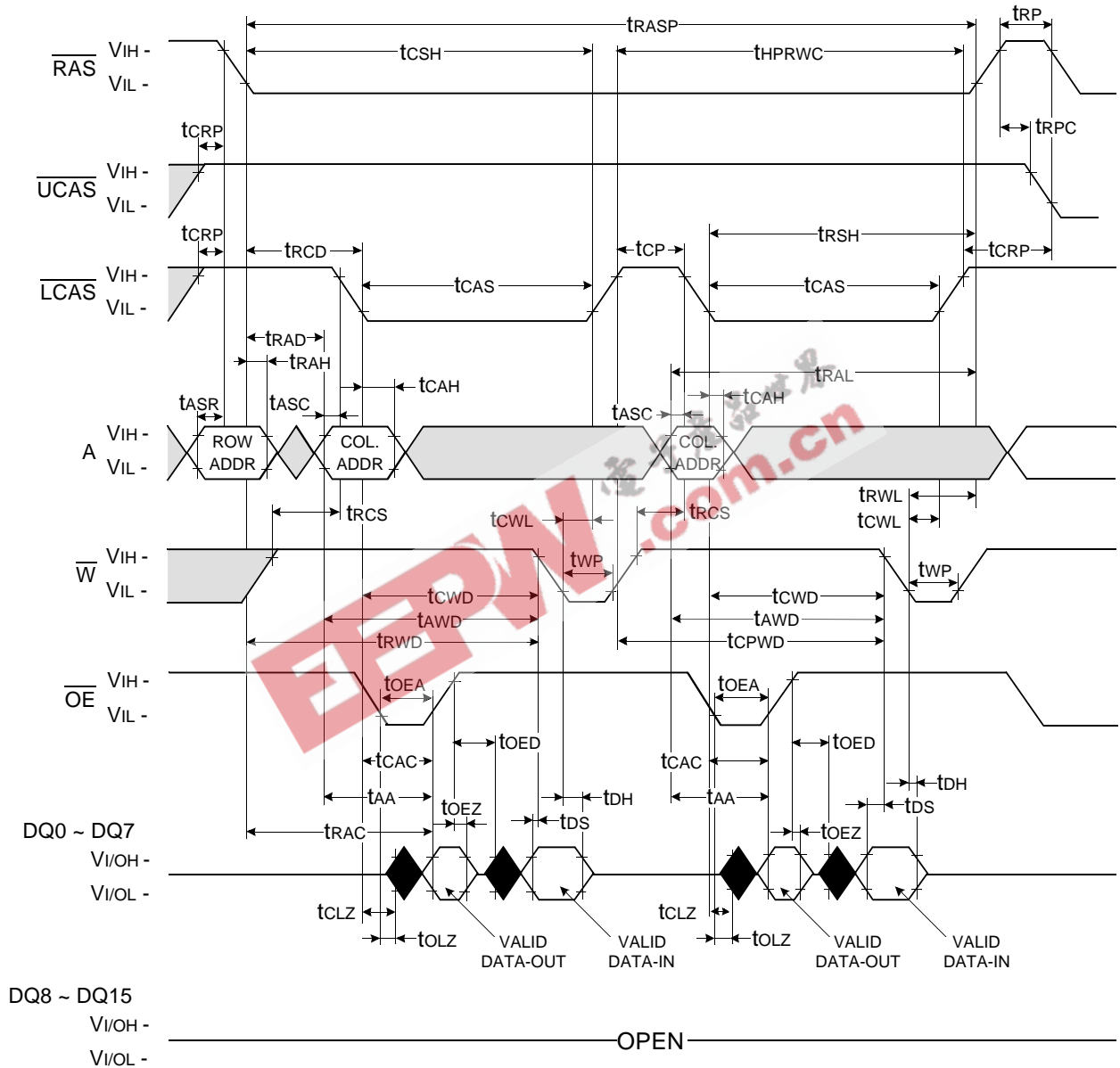
Don't care
 Undefined

HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE

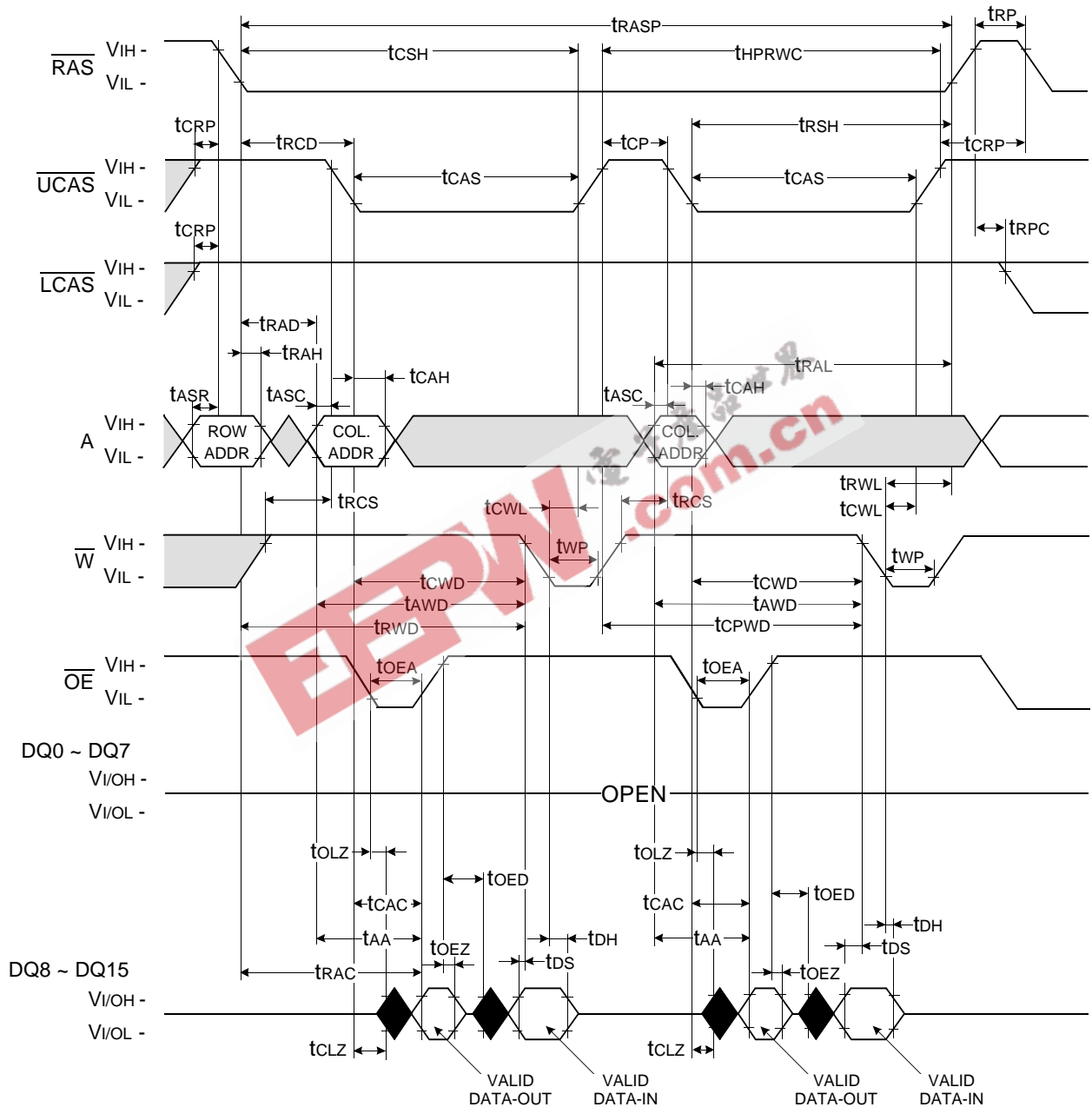


Don't care
Undefined

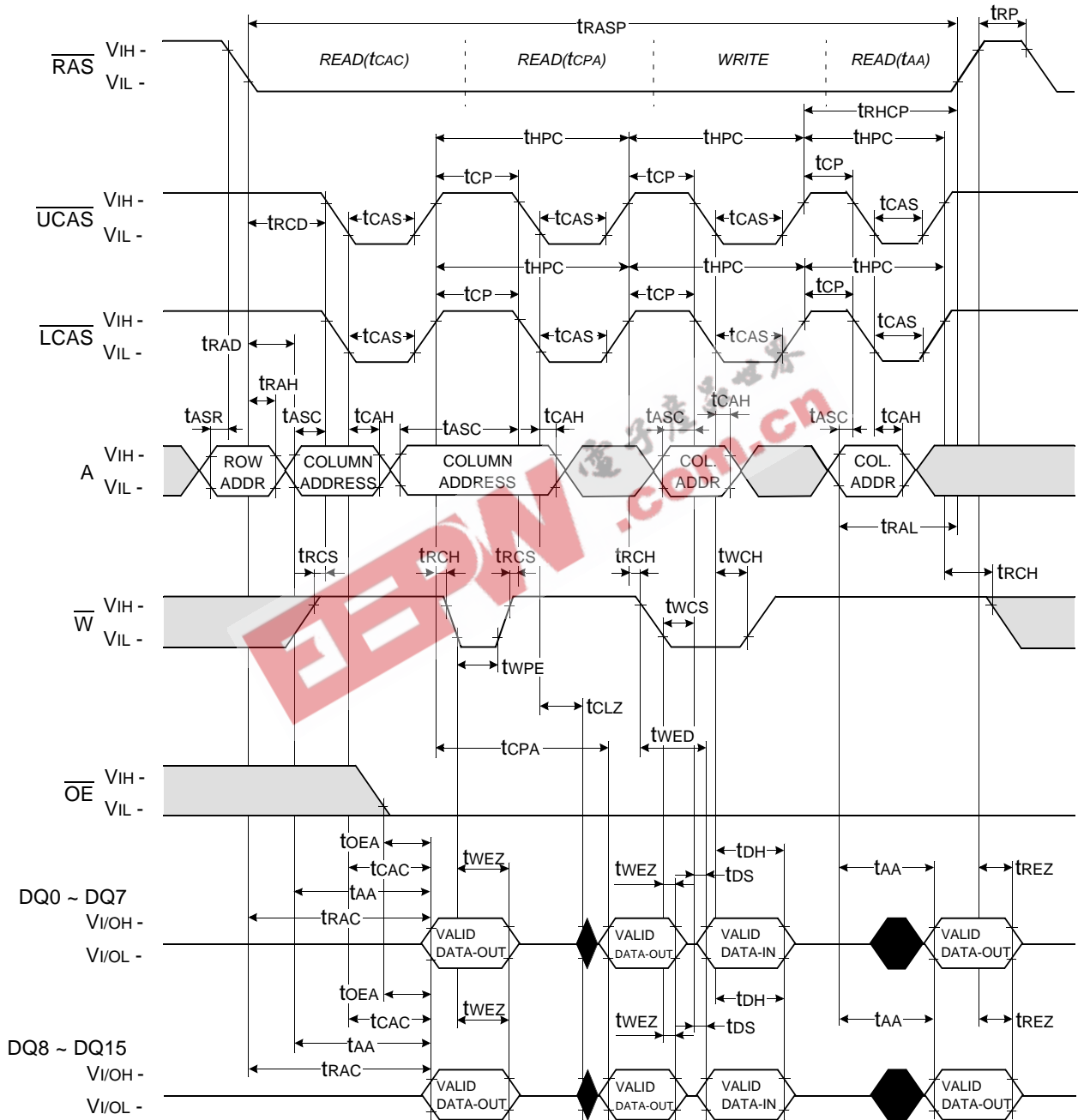
HYPER PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE



HYPER PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE



HYPER PAGE READ AND WRITE MIXED CYCLE



Don't care
 Undefined

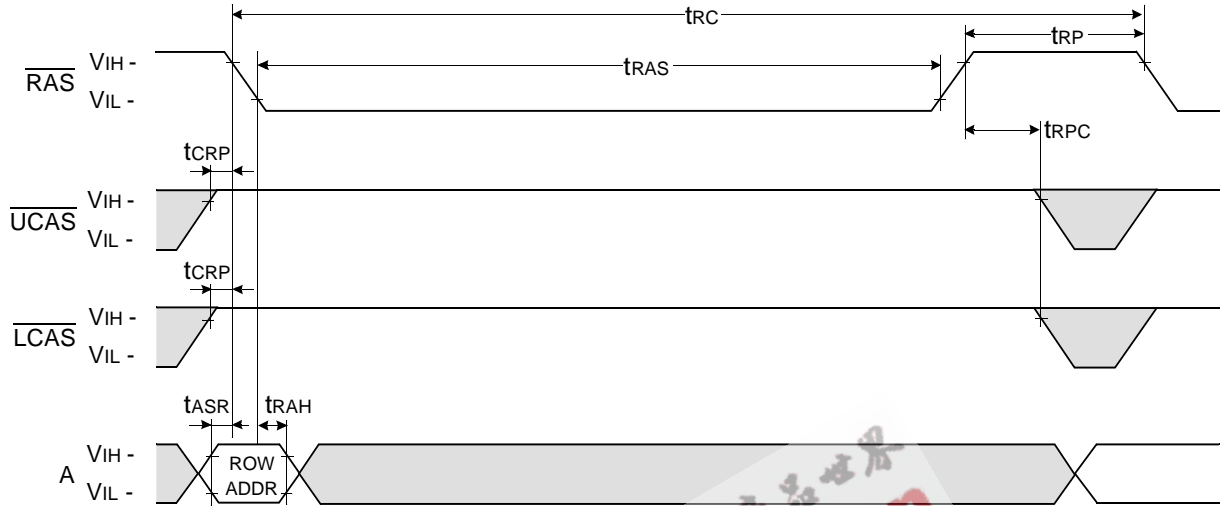
K4E171611D, K4E151611D K4E171612D, K4E151612D

CMOS DRAM

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

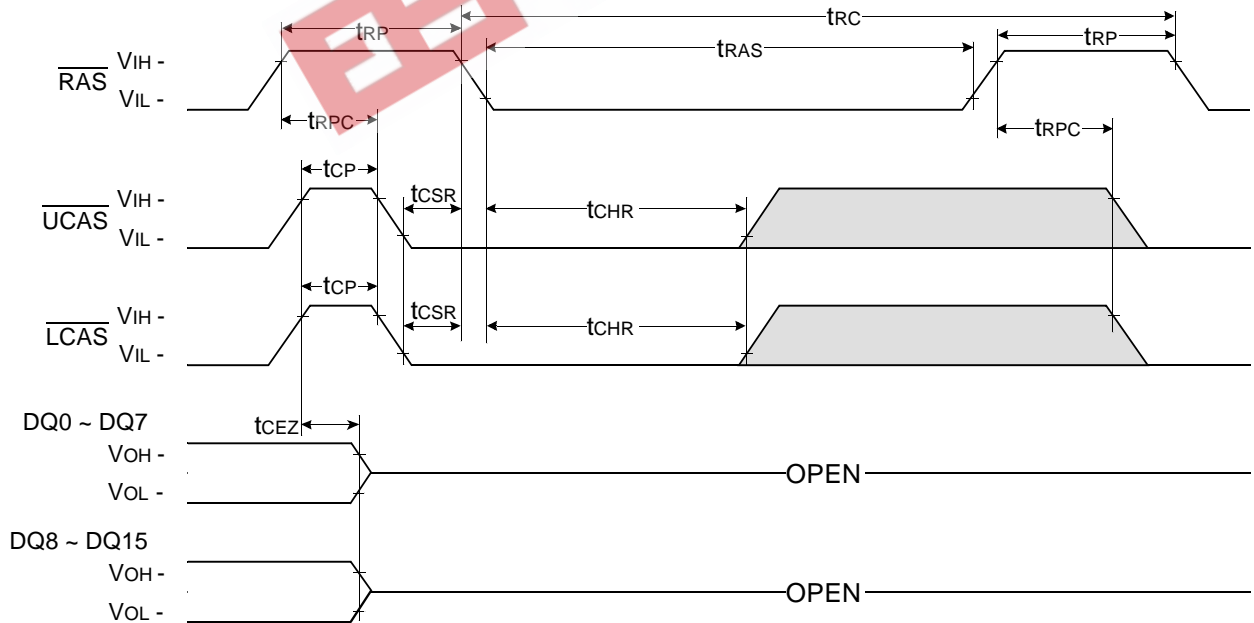
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



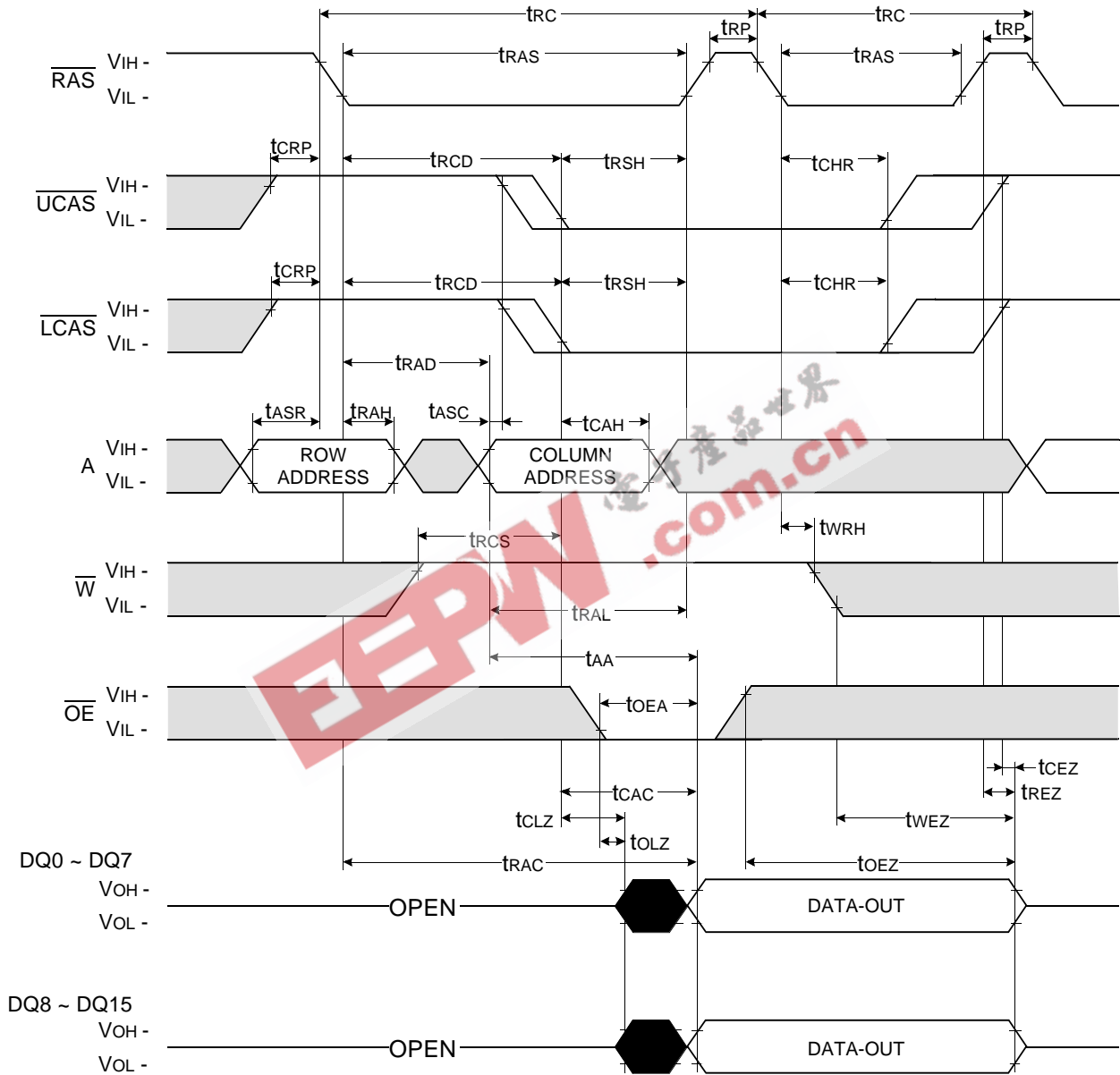
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

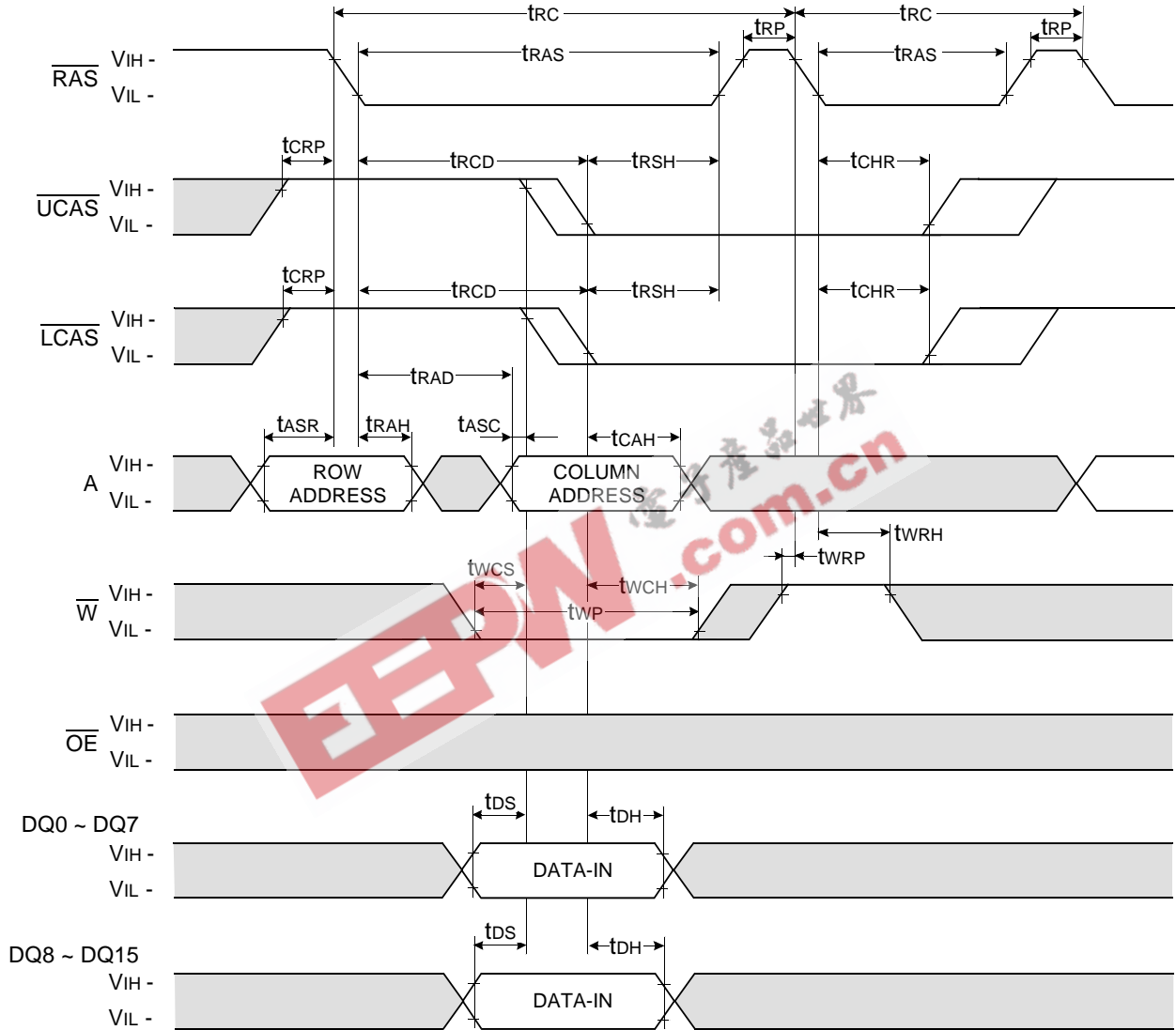
HIDDEN REFRESH CYCLE (READ)



Don't care
 Undefined

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



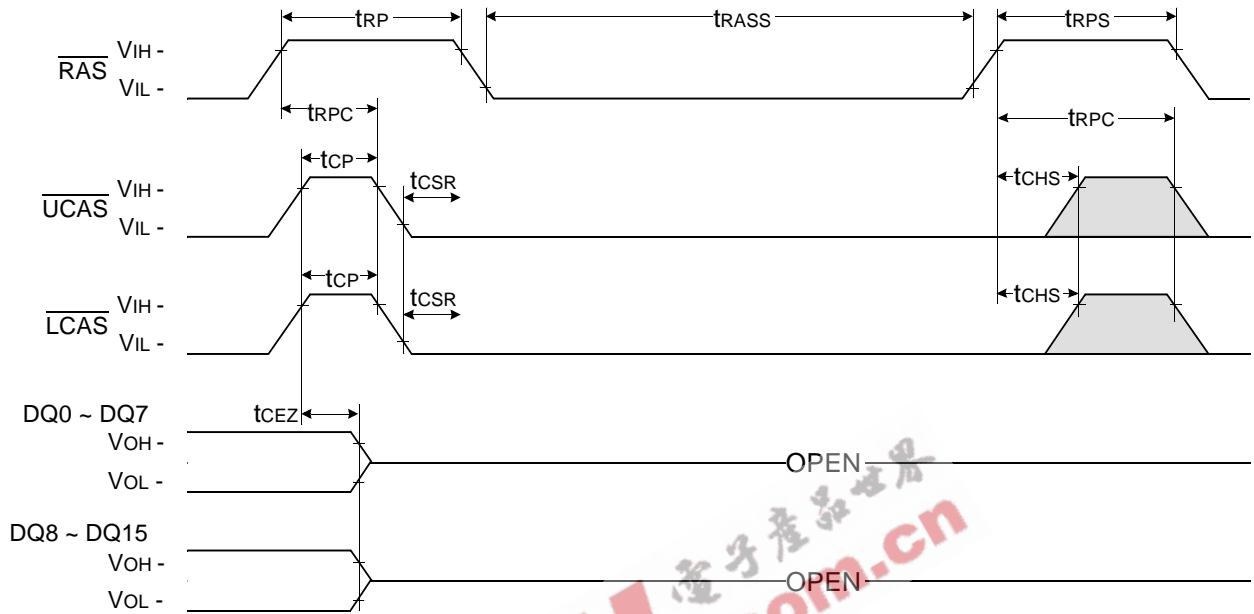
□ Don't care
 ■ Undefined

**K4E171611D, K4E151611D
K4E171612D, K4E151612D**

CMOS DRAM

$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



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Don't care
 Undefined

**K4E171611D, K4E151611D
K4E171612D, K4E151612D**

CMOS DRAM

PACKAGE DIMENSION

