

**Document Title**

**256Kx36 & 512Kx18-Bit Flow Through NtRAM™**

**Revision History**

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial document.	May. 18. 2001	Preliminary
0.1	1. Add x32 org part and industrial temperature part	Aug. 11. 2001	Preliminary
0.2	1. change scan order(1) form 4T to 6T at 119BGA(x18)	Aug. 28. 2001	Preliminary
1.0	1. Final spec release 2. Change ISB2 form 50mA to 60mA	Nov. 16. 2001	Final
2.0	Change ordering information( remove 225MHz at Nt-Pipelined)	April. 01. 2002	Final
2.1	1. Delete 119BGA package	April. 04. 2003	Final
3.0	1. Remove x32 organization 2. Remove -85 speed bin	Nov. 17. 2003	Final



The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

**K7M803625B  
K7M801825B**

**256Kx36 & 512Kx18 Flow-Through NtRAM™**

**8Mb NtRAM(Flow Through / Pipelined) Ordering Information**

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
512Kx18	K7M801825B-QC(I)65/75	FlowThrough	3.3	6.5/7.5 ns	Q: 100TQFP	C: Commercial Temperature Range I: Industrial Temperature Range
	K7N801801B-QC(I)16/13	Pipelined	3.3	167/133 MHz		
	K7N801809B-QC(I)25	Pipelined	3.3	250 MHz		
	K7N801845B-QC(I)16/13	Pipelined	2.5	167/133 MHz		
	K7N801849B-QC(I)25	Pipelined	2.5	250MHz		
256Kx36	K7M803625B-QC(I)65/75	FlowThrough	3.3	6.5/7.5 ns		
	K7N803601B-QC(I)16/13	Pipelined	3.3	167/133 MHz		
	K7N803609B-QC(I)25	Pipelined	3.3	250 MHz		
	K7N803645B-QC(I)16/13	Pipelined	2.5	167/133 MHz		
	K7N803649B-QC(I)25	Pipelined	2.5	250 MHz		



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## 256Kx36 & 512Kx18 Flow-Through NtRAM™

### 256Kx36 & 512Kx18-Bit Flow Through NtRAM™

#### FEATURES

- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention.
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A
- Operating in commercial and industrial temperature range.

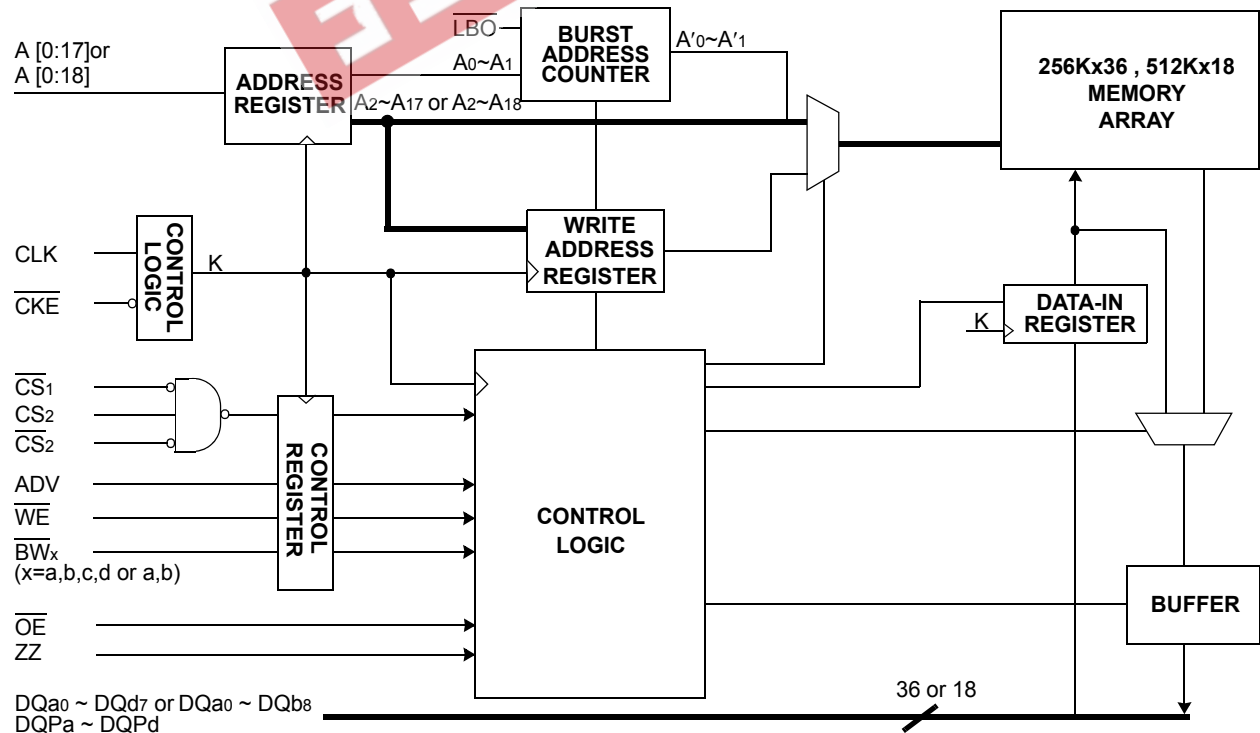
#### FAST ACCESS TIMES

Parameter	Symbol	-65	-75	Unit
Cycle Time	t <sub>CYC</sub>	7.5	8.5	ns
Clock Access Time	t <sub>CD</sub>	6.5	7.5	ns
Output Enable Access Time	t <sub>OE</sub>	3.5	3.5	ns

#### GENERAL DESCRIPTION

The K7M803625B and K7M801825B are 9,437,184-bit Synchronous Static SRAMs. The NtRAM™, or No Turnaround Random Access Memory utilizes all bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, Flow-Through SRAM allows output data to simply flow freely from the memory array. The K7M803625B and K7M801825B are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP and Multiple power and ground pins minimize ground bounce.

#### LOGIC BLOCK DIAGRAM



NtRAM™ and No Turnaround Random Access Memory are trademarks of Samsung, and its architecture and functionalities are supported by NEC and Toshiba.

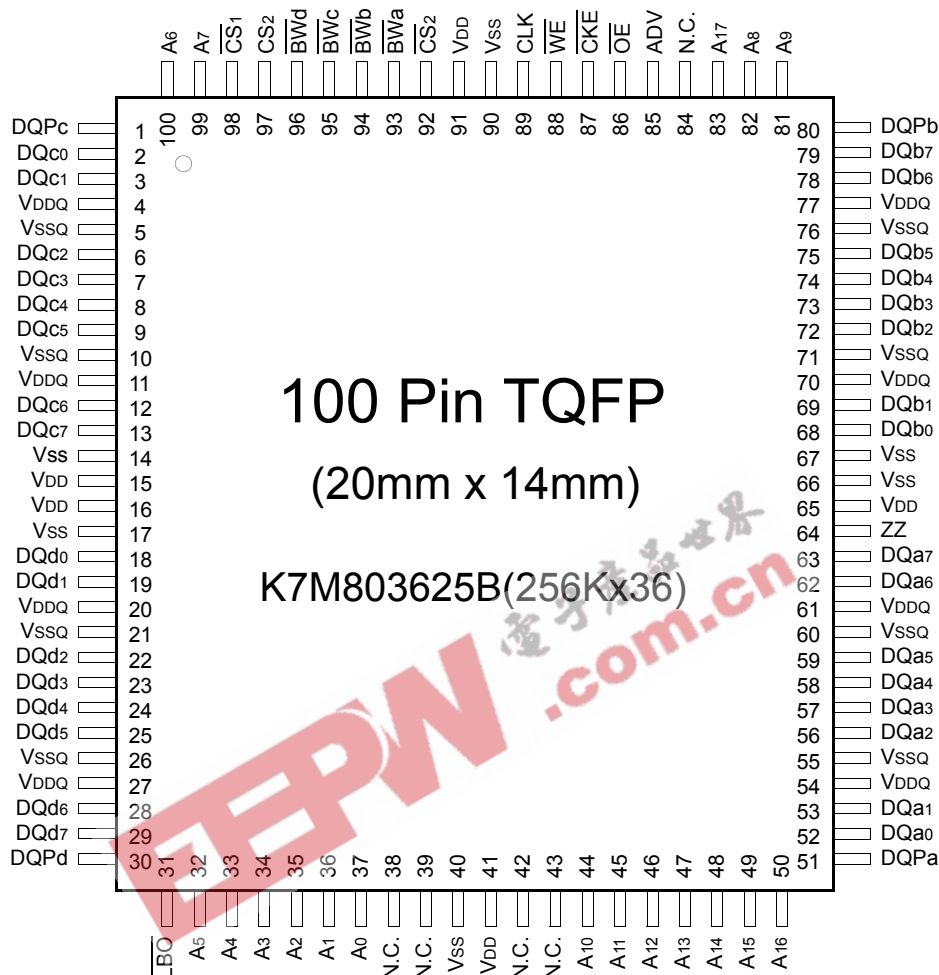


ELECTRONICS

# K7M803625B K7M801825B

## 256Kx36 & 512Kx18 Flow-Through NtRAM™

### PIN CONFIGURATION(TOP VIEW)



### PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,81 82,83,99,100	VDD	Power Supply(+3.3V)	15,16,41,65,91
			VSS	Ground	14,17,40,66,67,90
			N.C.	No Connect	38,39,42,43,84
ADV	Address Advance/Load	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
WE	Read/Write Control Input	88	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CKE	Clock Enable	87	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

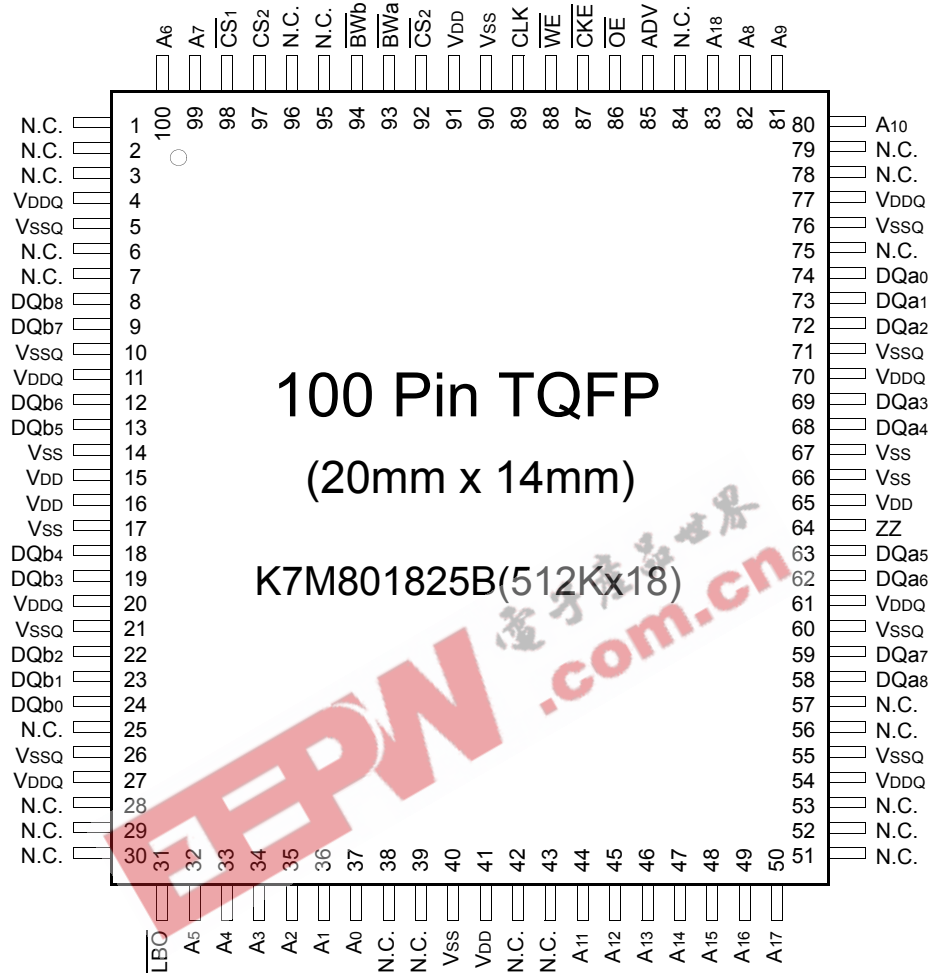
Notes : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.

2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,80 81,82,83,99,100	VDD	Power Supply(+3.3V)	15,16,41,65,91
			VSS	Ground	14,17,40,66,67,90
			N.C.	No Connect	1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,84,95,96
ADV	Address Advance/Load	85			
WE	Read/Write Control Input	88	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
CLK	Clock	89	DQb0~b8		8,9,12,13,18,19,22,23,24
CKE	Clock Enable	87			
CS1	Chip Select	98	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	97	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS2	Chip Select	92			
BW(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

**Notes :** 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.  
 2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

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## 256Kx36 & 512Kx18 Flow-Through NtRAM™

### FUNCTION DESCRIPTION

The K7M803625B and K7M801825B are NtRAM™ designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of  $\overline{OE}$ ,  $\overline{LBO}$  and  $\overline{ZZ}$ ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable ( $\overline{CKE}$ ) pin allows the operation of the chip to be suspended as long as necessary. When  $\overline{CKE}$  is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NtRAM™ latches external address and initiates a cycle, when  $\overline{CKE}$ , ADV are driven to low and all three chip enables ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{CS2}$ ) are active.

Output Enable ( $\overline{OE}$ ) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register,  $\overline{CKE}$  is driven low, all three chip enables ( $\overline{CS1}$ ,  $CS2$ ,  $\overline{CS2}$ ) are active, the write enable input signals  $\overline{WE}$  are driven high, and ADV driven low. Data appears at the outputs within the same clock cycle as the address for the data. Also during read operation  $\overline{OE}$  must be driven low for the device to drive out the requested data.

Write operation occurs when  $\overline{WE}$  is driven low at the rising edge of the clock.  $\overline{BW}[d:a]$  can be used for byte write operation. The Flow Through NtRAM™ uses a late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock,  $\overline{WE}$  and address are registered, and the data associated with that address is required one cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the  $\overline{LBO}$  pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation,  $\overline{ZZ}$  must be driven low. When  $\overline{ZZ}$  is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles.

At this time, internal state of the SRAM is preserved. When  $\overline{ZZ}$  returns to low, the SRAM normally operates after 2 cycles of wake up time.

### BURST SEQUENCE TABLE

(Interleaved Burst,  $\overline{LBO}$ =High)

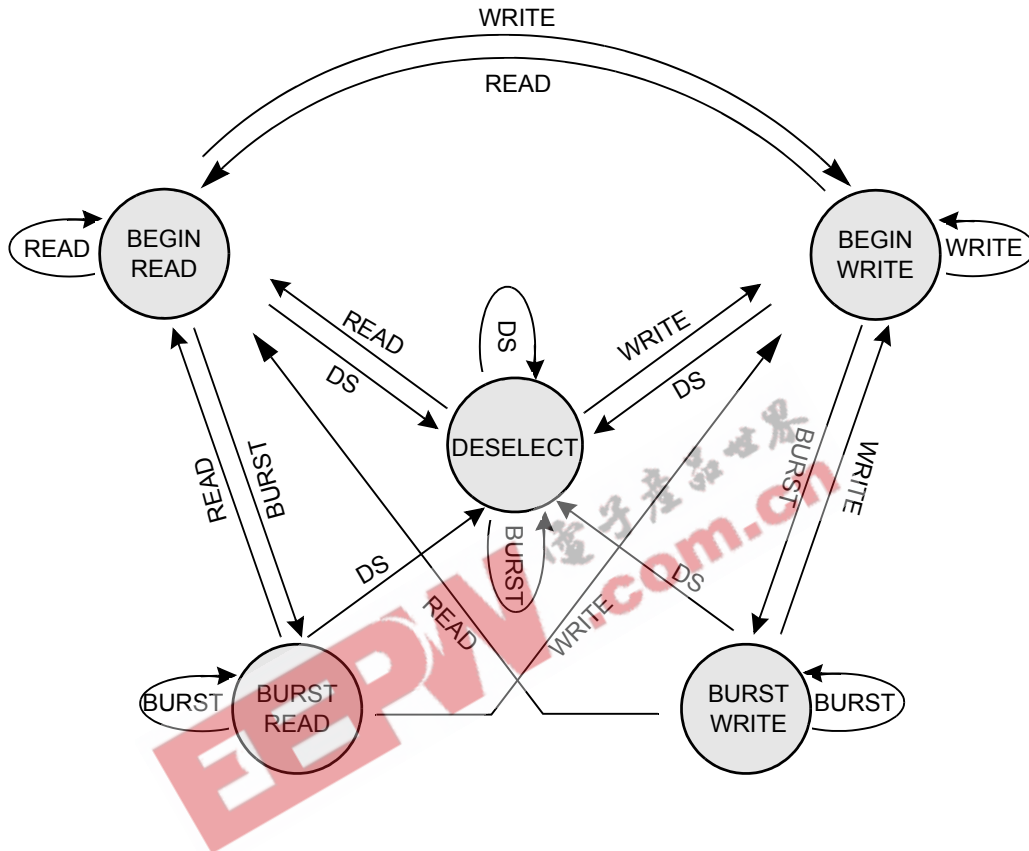
$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst,  $\overline{LBO}$ =Low)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.  
2. States change on the rising edge of the clock(CLK)

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## TRUTH TABLES

### SYNCHRONOUS TRUTH TABLE

CS <sub>1</sub>	CS <sub>2</sub>	CS <sub>2</sub>	ADV	WE	BW <sub>x</sub>	OE	CKE	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).

3. A continue deselect cycle can only be entered if a deselect cycle is executed first.

4.  $\overline{\text{WRITE}} = \text{L}$  means Write operation in WRITE TRUTH TABLE.

$\overline{\text{WRITE}} = \text{H}$  means Read operation in WRITE TRUTH TABLE.

5. Operation finally depends on status of asynchronous input pins(ZZ and OE).

### WRITE TRUTH TABLE<sub>(x36)</sub>

WE	BW <sub>a</sub>	BW <sub>b</sub>	BW <sub>c</sub>	BW <sub>d</sub>	Operation
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

### WRITE TRUTH TABLE<sub>(x18)</sub>

WE	BW <sub>a</sub>	BW <sub>b</sub>	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).



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**ASYNCHRONOUS TRUTH TABLE**

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**Notes**

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT	
Voltage on VDD Supply Relative to Vss	VDD	-0.3 to 4.6	V	
Voltage on Any Other Pin Relative to Vss	VIN	-0.3 to VDD+0.3	V	
Power Dissipation	PD	1.4	W	
Storage Temperature	TSTG	-65 to 150	°C	
Operating Temperature	Commercial	TOPR	0 to 70	°C
	Industrial	TOPR	-40 to 85	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C	

\*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)**

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

\* The above parameters are also guaranteed at industrial temperature range.

**OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)**

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

\* The above parameters are also guaranteed at industrial temperature range.

**CAPACITANCE\* (TA=25°C, f=1MHz)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	7	pF

\*Note : Sampled not 100% tested.

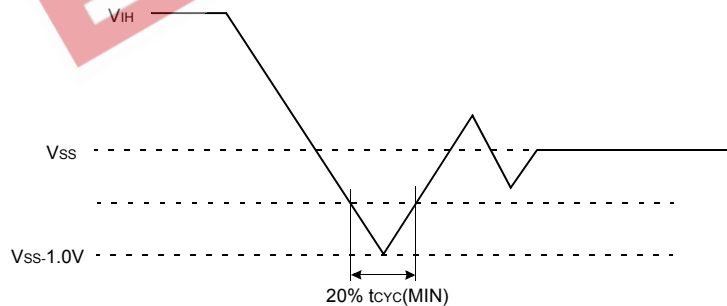
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## DC ELECTRICAL CHARACTERISTICS (V<sub>DD</sub>=3.3V+0.165V/-0.165V, T<sub>A</sub>=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES	
Input Leakage Current(except ZZ)	I <sub>IL</sub>	V <sub>DD</sub> =Max ; V <sub>IN</sub> =V <sub>SS</sub> to V <sub>DD</sub>	-2	+2	μA		
Output Leakage Current	I <sub>OL</sub>	Output Disabled,	-2	+2	μA		
Operating Current	I <sub>CC</sub>	Device Selected , I <sub>OUT</sub> =0mA, ZZ≤V <sub>IL</sub> . Cycle Time ≥ t <sub>CYC</sub> Min	-65	-	300	mA	1,2
			-75	-	280		
Standby Current	I <sub>SB</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≤V <sub>IL</sub> , f=Max, All Inputs≤0.2V or ≥V <sub>DD</sub> -0.2V	-65	-	140	mA	
			-75	-	130		
	I <sub>SB1</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V <sub>DD</sub> -0.2V or 0.2V)	-	-	100	mA	
	I <sub>SB2</sub>	Device deselected, I <sub>OUT</sub> =0mA, ZZ≥V <sub>DD</sub> -0.2V, f=Max, All Inputs≤V <sub>IL</sub> or ≥V <sub>IH</sub>	-	-	60	mA	
Output Low Voltage(3.3V I/O)	V <sub>OL</sub>	I <sub>OL</sub> =8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	V <sub>OH</sub>	I <sub>OH</sub> =-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	V <sub>OL</sub>	I <sub>OL</sub> =1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	V <sub>IL</sub>		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	V <sub>IH</sub>		2.0	V <sub>DD</sub> +0.3**	V	3	
Input Low Voltage(2.5V I/O)	V <sub>IL</sub>		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	V <sub>IH</sub>		1.7	V <sub>DD</sub> +0.3**	V	3	

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
  2. Reference AC Operating Conditions and Characteristics for input and timing.
  3. Data states are all zero.
  4. In Case of I/O Pins, the Max. V<sub>IH</sub>=V<sub>DDQ</sub>+0.3V.



## TEST CONDITIONS

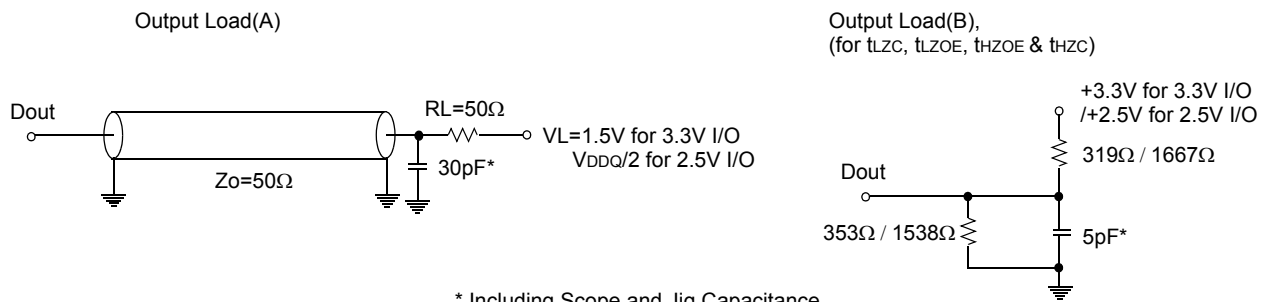
(V<sub>DD</sub>=3.3V+0.165V/-0.165V, V<sub>DDQ</sub>=3.3V+0.165V/-0.165V or V<sub>DD</sub>=3.3V+0.165V/-0.165V, V<sub>DDQ</sub>=2.5V+0.4V/-0.125V, T<sub>A</sub>=0to70°C)

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V <sub>DDQ</sub> /2
Output Load	See Fig. 1

\* The above parameters are also guaranteed at industrial temperature range.

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\* Including Scope and Jig Capacitance

Fig. 1

### AC TIMING CHARACTERISTICS (VDD=3.3V+0.165V/-0.165V, TA=0°C to +70°C)

PARAMETER	SYMBOL	-65		-75		UNIT
		MIN	MAX	MIN	MAX	
Cycle Time	t <sub>cy</sub>	7.5	-	8.5	-	ns
Clock Access Time	t <sub>cd</sub>	-	6.5	-	7.5	ns
Output Enable to Data Valid	t <sub>oe</sub>	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t <sub>LZC</sub>	2.5	-	2.5	-	ns
Output Hold from Clock High	t <sub>oh</sub>	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t <sub>LZOE</sub>	0	-	0	-	ns
Output Enable High to Output High-Z	t <sub>HZOE</sub>	-	3.5	-	3.5	ns
Clock High to Output High-Z	t <sub>HZC</sub>	-	3.8	-	4.0	ns
Clock High Pulse Width	t <sub>ch</sub>	2.5	-	2.8	-	ns
Clock Low Pulse Width	t <sub>cl</sub>	2.5	-	2.8	-	ns
Address Setup to Clock High	t <sub>as</sub>	1.5	-	2.0	-	ns
$\overline{\text{CKE}}$ Setup to Clock High	t <sub>ces</sub>	1.5	-	2.0	-	ns
Data Setup to Clock High	t <sub>ds</sub>	1.5	-	2.0	-	ns
Write Setup to Clock High ( $\overline{\text{WE}}$ , $\overline{\text{BWx}}$ )	t <sub>ws</sub>	1.5	-	2.0	-	ns
Address Advance Setup to Clock High	t <sub>adv<sub>s</sub></sub>	1.5	-	2.0	-	ns
Chip Select Setup to Clock High	t <sub>css</sub>	1.5	-	2.0	-	ns
Address Hold from Clock High	t <sub>ah</sub>	0.5	-	0.5	-	ns
$\overline{\text{CKE}}$ Hold from Clock High	t <sub>ceh</sub>	0.5	-	0.5	-	ns
Data Hold from Clock High	t <sub>dh</sub>	0.5	-	0.5	-	ns
Write Hold from Clock High ( $\overline{\text{WE}}$ , $\overline{\text{BWx}}$ )	t <sub>wh</sub>	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t <sub>adv<sub>h</sub></sub>	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t <sub>cs<sub>h</sub></sub>	0.5	-	0.5	-	ns
ZZ High to Power Down	t <sub>pds</sub>	2	-	2	-	cycle
ZZ Low to Power Up	t <sub>p<sub>us</sub></sub>	2	-	2	-	cycle

- Notes :**
- The above parameters are also guaranteed at industrial temperature range.
  - All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and  $\overline{\text{CS}}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  - Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
  - A write cycle is defined by  $\overline{\text{WE}}$  low having been registered into the device at ADV Low, A Read cycle is defined by  $\overline{\text{WE}}$  High with ADV Low, Both cases must meet setup and hold times.
  - To avoid bus contention, At a given voltage and temperature t<sub>LZC</sub> is more than t<sub>HZC</sub>.  
The specs as shown do not imply bus contention because t<sub>LZC</sub> is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than t<sub>HZC</sub>, which is a Max. parameter(worst case at 70°C,3.135V)  
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

**SLEEP MODE**

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to  $I_{SB2}$ . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

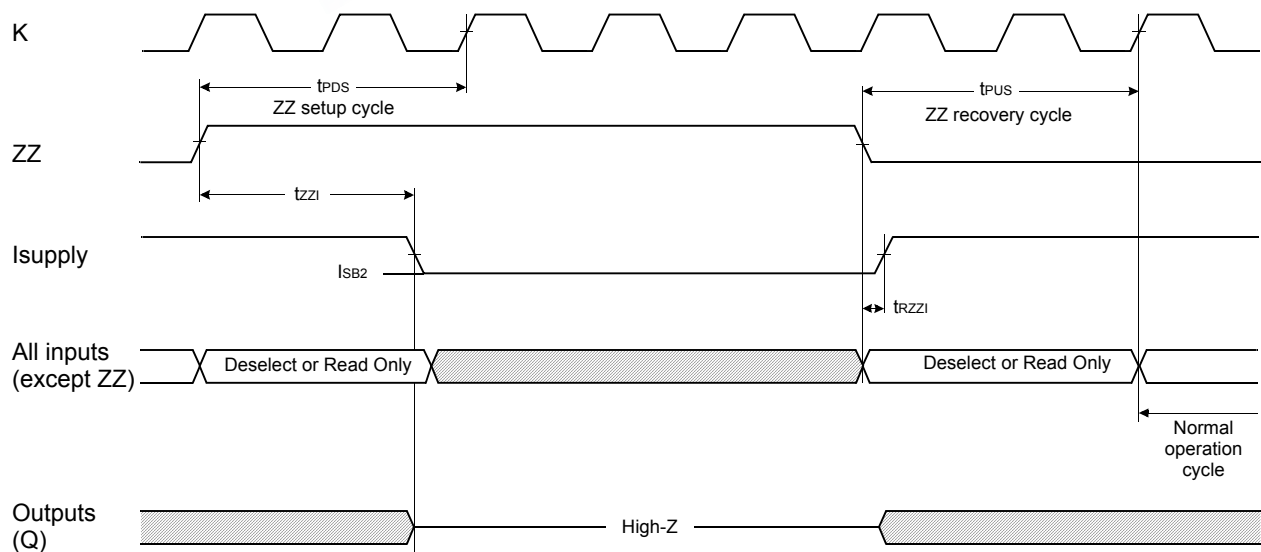
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High,  $I_{SB2}$  is guaranteed after the time  $t_{ZZ1}$  is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during  $t_{PUS}$ , only a Deselect or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

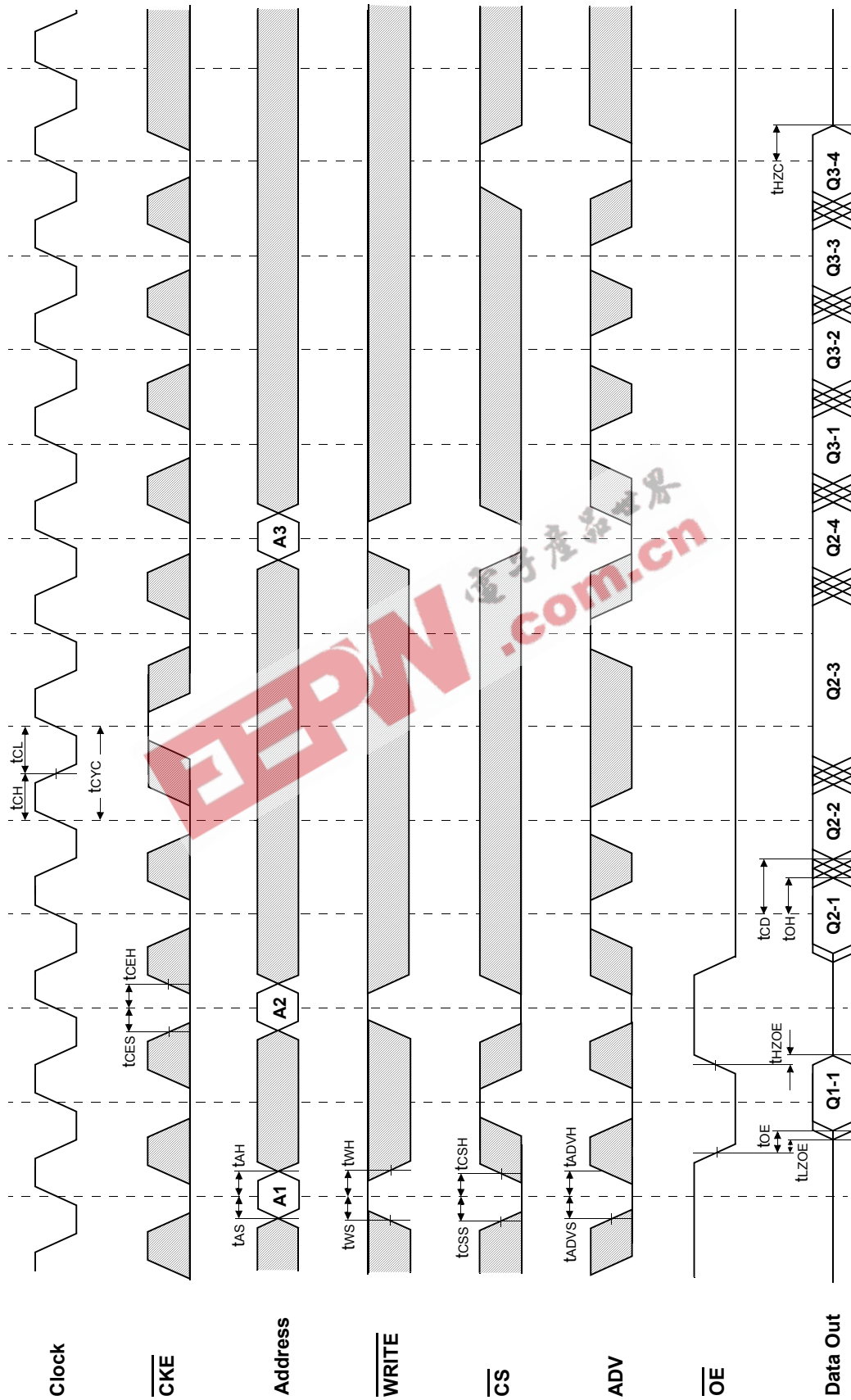
**SLEEP MODE ELECTRICAL CHARACTERISTICS**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	$I_{SB2}$		60	mA
ZZ active to input ignored		$t_{PDS}$	2		cycle
ZZ inactive to input sampled		$t_{PUS}$	2		cycle
ZZ active to SLEEP current		$t_{ZZ1}$		2	cycle
ZZ inactive to exit SLEEP current		$t_{RZZ1}$	0		

**SLEEP MODE WAVEFORM**



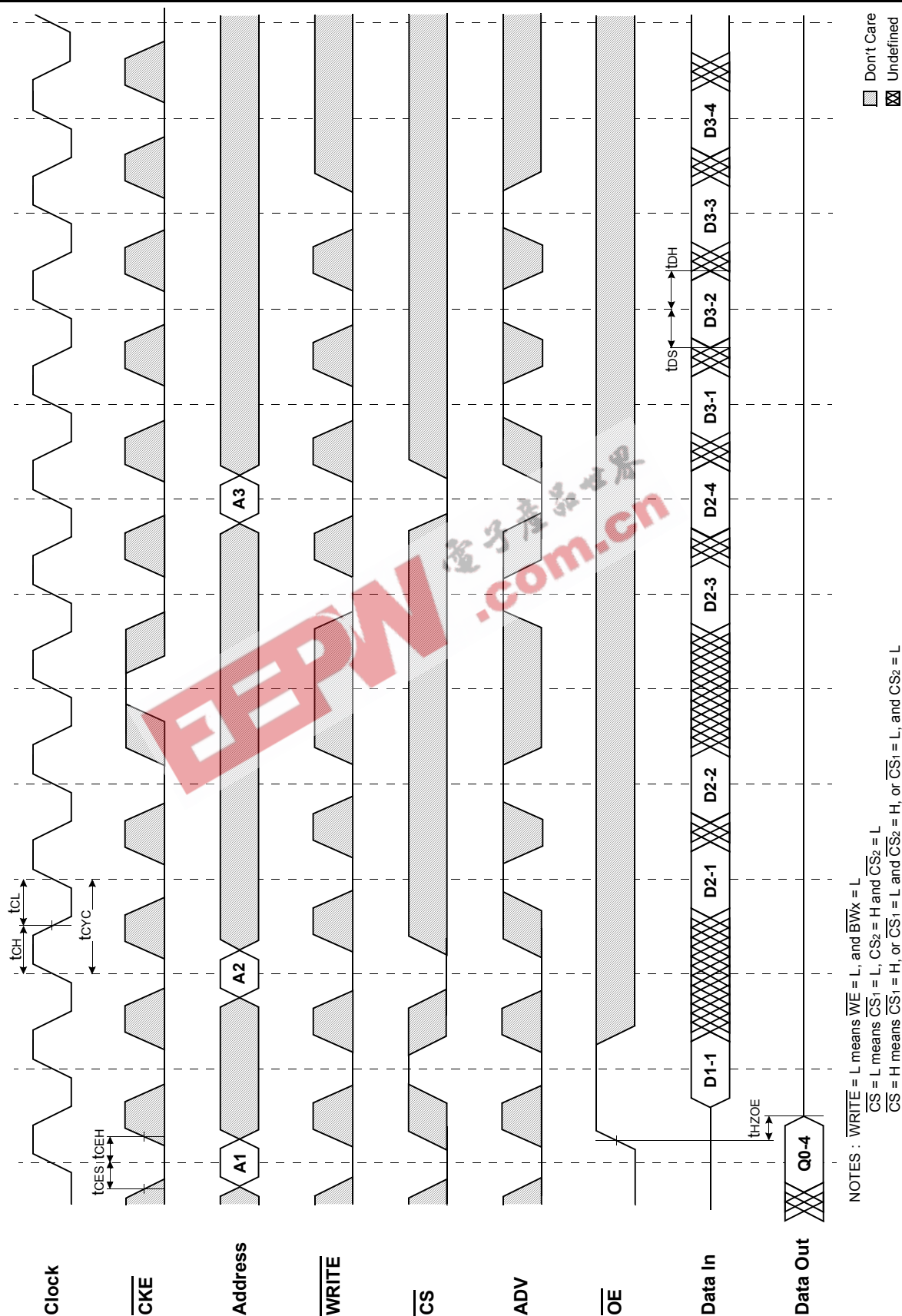
TIMING WAVEFORM OF READ CYCLE



□ Don't Care  
▨ Undefined

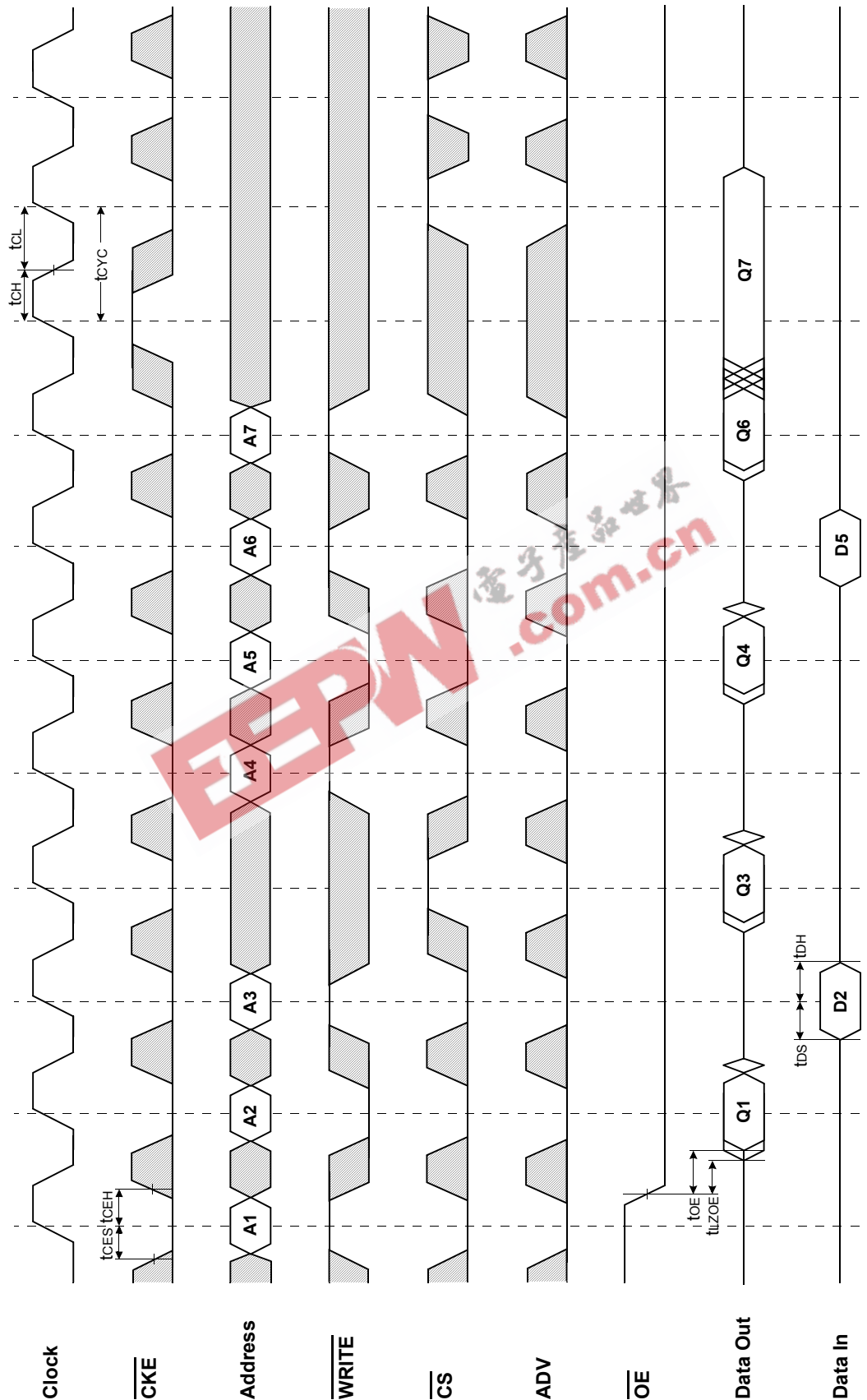
NOTES :  $\overline{WRITE} = L$  means  $\overline{WE} = L$ , and  $\overline{BWx} = L$   
 $\overline{CS} = L$  means  $\overline{CS}_1 = L$ ,  $\overline{CS}_2 = H$  and  $\overline{CS}_2 = L$   
 $\overline{CS} = H$  means  $\overline{CS}_1 = H$ , or  $\overline{CS}_1 = L$  and  $\overline{CS}_2 = H$ , or  $\overline{CS}_1 = L$ , and  $\overline{CS}_2 = L$

TIMING WAVEFORM OF WRTE CYCLE



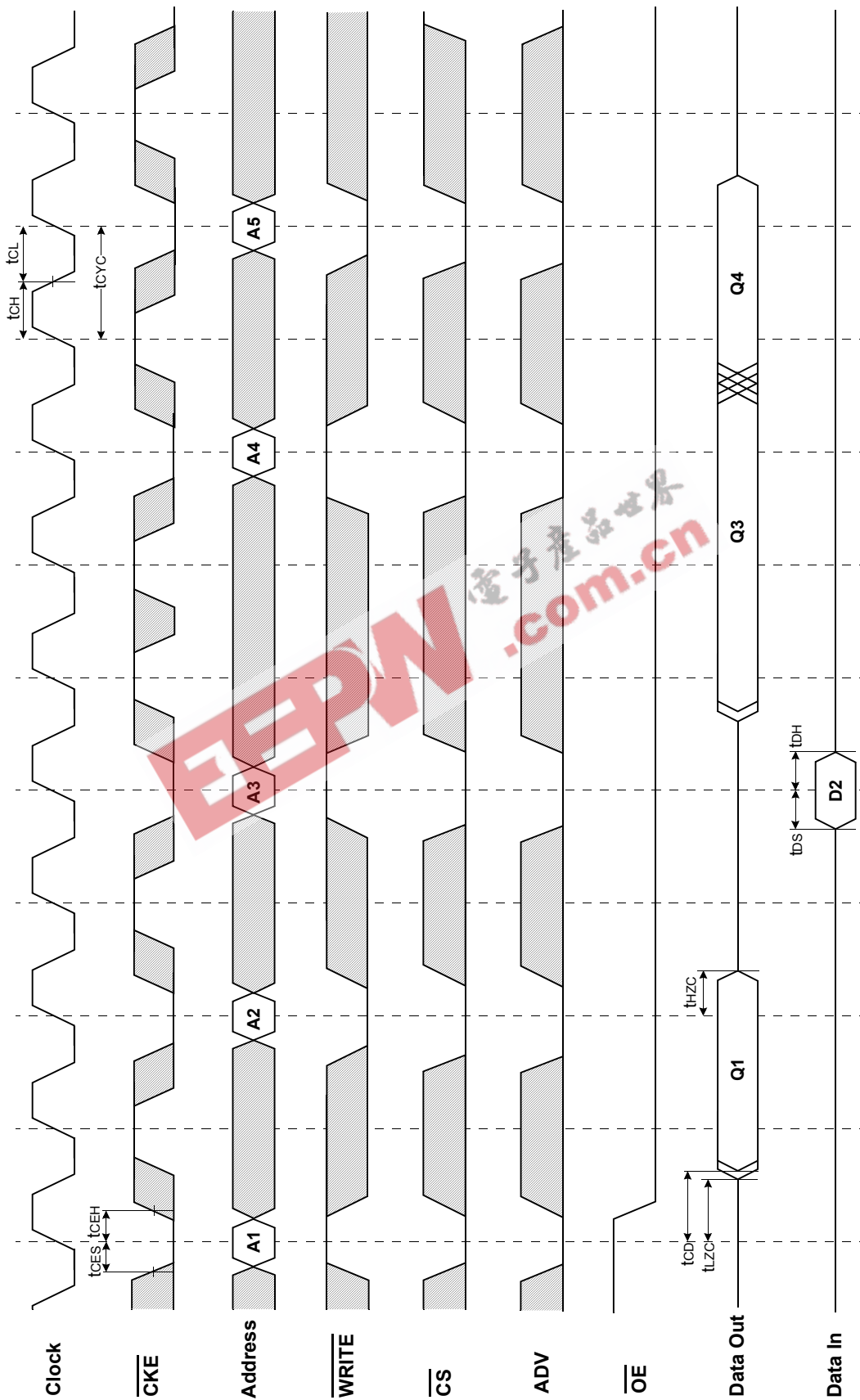
NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BWx}} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\overline{\text{CS}}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\overline{\text{CS}}_2 = \text{L}$

TIMING WAVEFORM OF SINGLE READ/WRITE



NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BWx}} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\overline{\text{CS}}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\overline{\text{CS}}_2 = \text{L}$

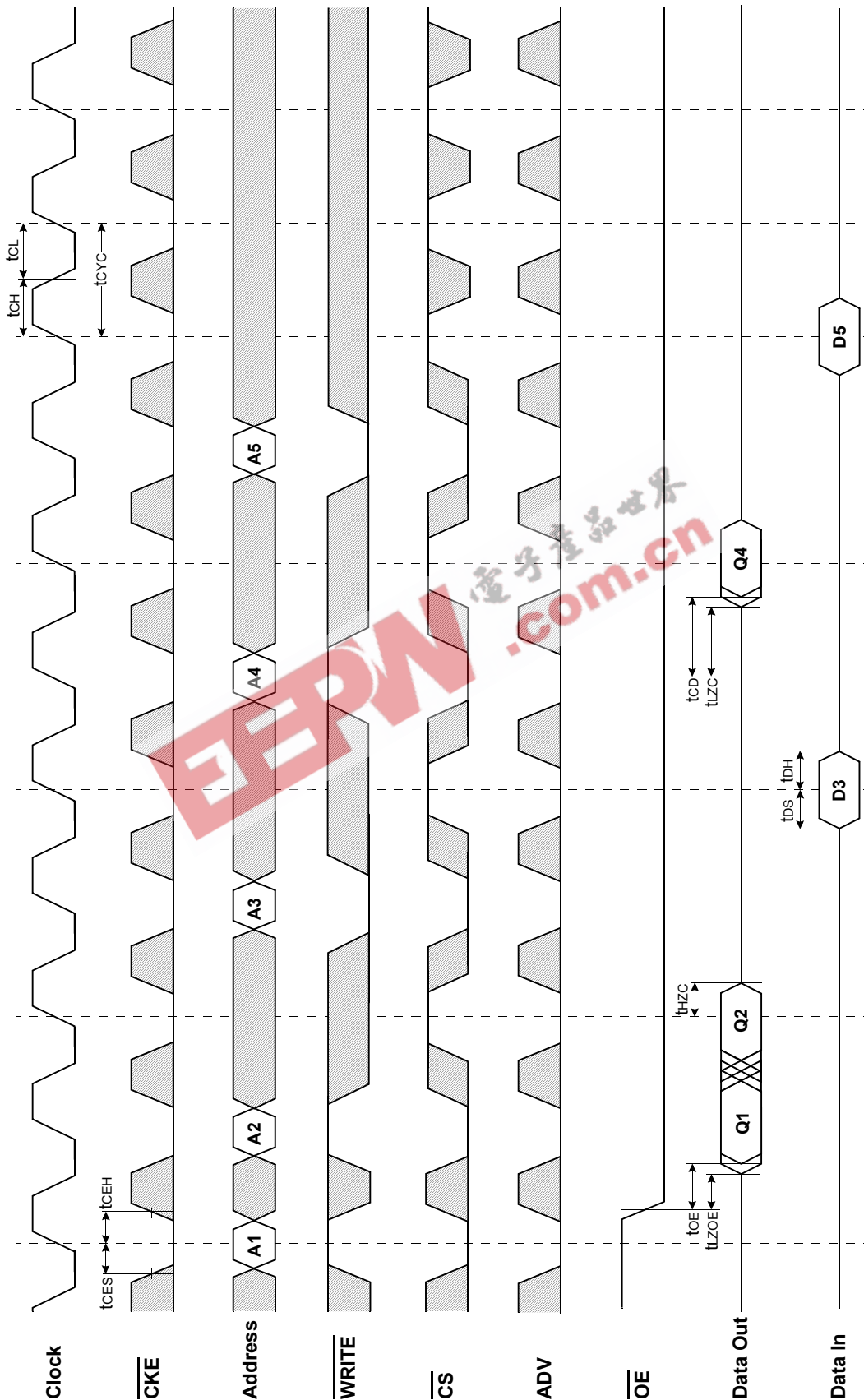
TIMING WAVEFORM OF CKE OPERATION



NOTES : WRITE = L means WE = L, and BWx = L  
CS = L means CS<sub>1</sub> = L, CS<sub>2</sub> = H and CS<sub>2</sub> = L  
CS = H means CS<sub>1</sub> = H, or CS<sub>1</sub> = L and CS<sub>2</sub> = H, or CS<sub>1</sub> = L, and CS<sub>2</sub> = L



TIMING WAVEFORM OF  $\overline{\text{CS}}$  OPERATION



Don't Care  
 Undefined

NOTES :  $\overline{\text{WRITE}} = \text{L}$  means  $\overline{\text{WE}} = \text{L}$ , and  $\overline{\text{BWx}} = \text{L}$   
 $\overline{\text{CS}} = \text{L}$  means  $\overline{\text{CS}}_1 = \text{L}$ ,  $\overline{\text{CS}}_2 = \text{H}$  and  $\overline{\text{CS}}_2 = \text{L}$   
 $\overline{\text{CS}} = \text{H}$  means  $\overline{\text{CS}}_1 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$  and  $\overline{\text{CS}}_2 = \text{H}$ , or  $\overline{\text{CS}}_1 = \text{L}$ , and  $\overline{\text{CS}}_2 = \text{L}$

