

16Mx16  
SDRAM 54CSP  
(VDD/VDDQ 3.0V/3.0V or 3.3V/3.3V)

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## 4M x 16Bit x 4 Banks Synchronous DRAM in 54CSP

### FEATURES

- 3.0V & 3.3V power supply.
- LVCMOS compatible with multiplexed address.
- Four banks operation.
- MRS cycle with address key programs.
  - CAS latency (1 & 2 & 3).
  - Burst length (1, 2, 4, 8 & Full page).
  - Burst type (Sequential & Interleave).
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation.
- DQM for masking
- Auto refresh.
- 64ms refresh period (8K cycle).
- Commercial Temperature Operation (-25°C ~ 70°C).  
Extended Temperature Operation (-25°C ~ 85°C).  
Industrial Temperature Operation (-40°C ~ 85°C).
- 54balls CSP (-RXXX - Pb, -BXXX - Pb Free)

### GENERAL DESCRIPTION

The K4S561633C is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### ORDERING INFORMATION

| Part No.               | Max Freq.                    | Interface | Package                   |
|------------------------|------------------------------|-----------|---------------------------|
| K4S561633C-R(B)L/N/P75 | 133MHz(CL=3)<br>105MHz(CL=2) | LVCMOS    | 54 CSP<br>Pb<br>(Pb Free) |
| K4S561633C-R(B)L/N/P1H | 105MHz(CL=2)                 |           |                           |
| K4S561633C-R(B)L/N/P1L | 105MHz(CL=3)*1               |           |                           |

-R(B)L ; Low Power, Operating Temp : -25°C ~ 70°C.

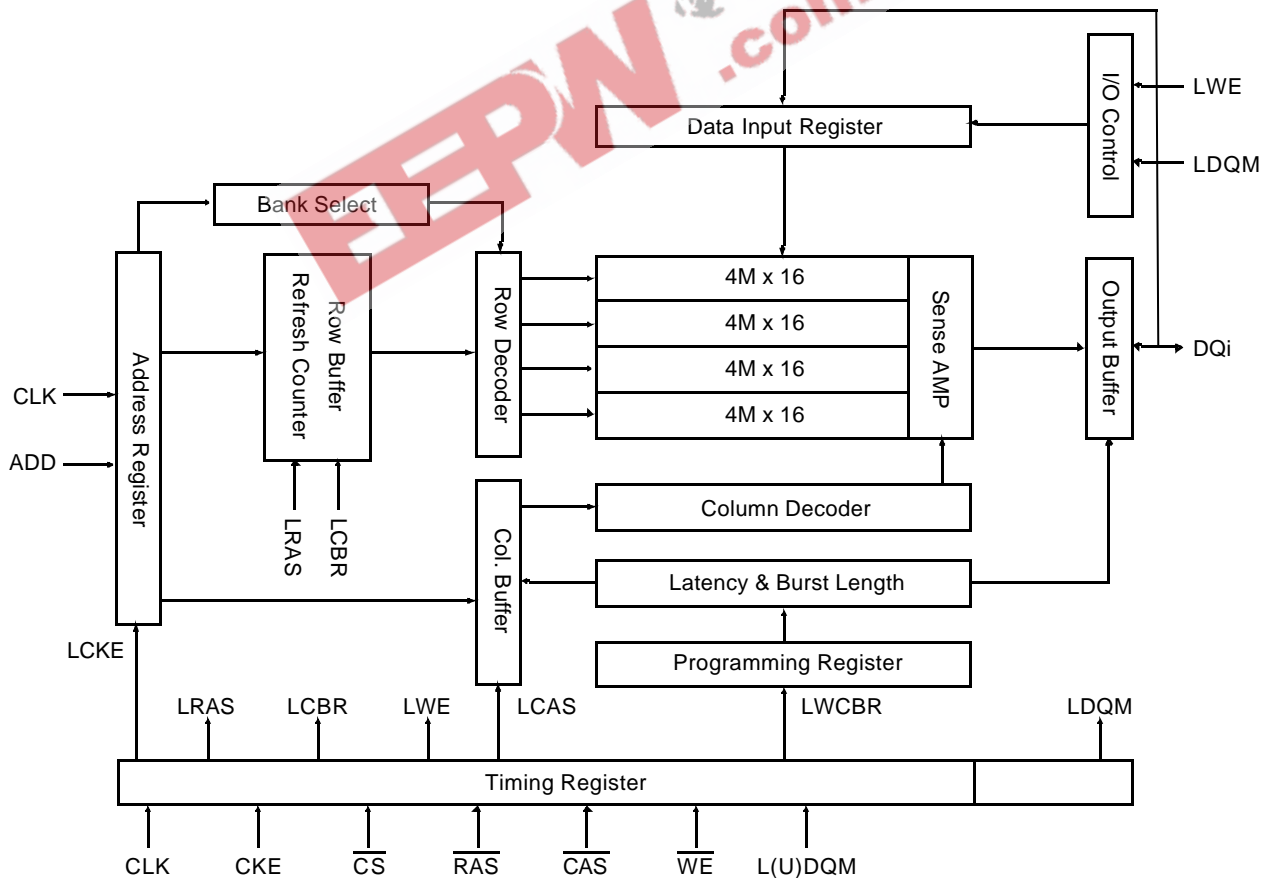
-R(B)N ; Low Power, Operating Temp : -25°C ~ 85°C.

-R(B)P : Low Power, Operating Temp : -40°C ~ 85°C.

**Note :**

1. In case of 40MHz Frequency, CL1 can be supported.

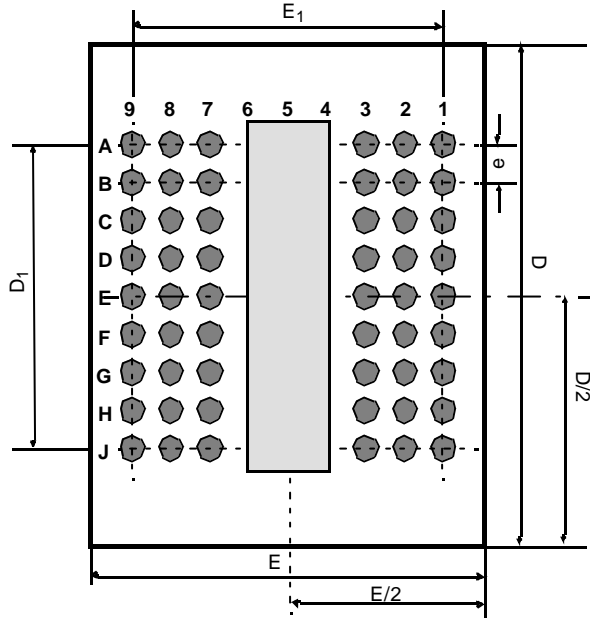
### FUNCTIONAL BLOCK DIAGRAM



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Package Dimension and Pin Configuration

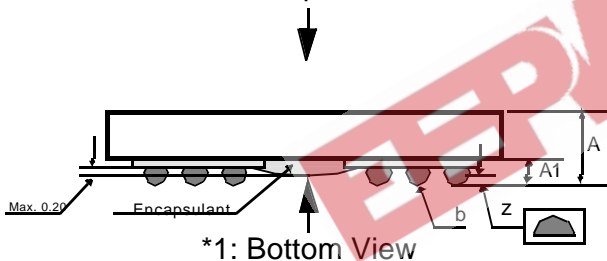
< Bottom View \*1 >



< Top View \*2 >

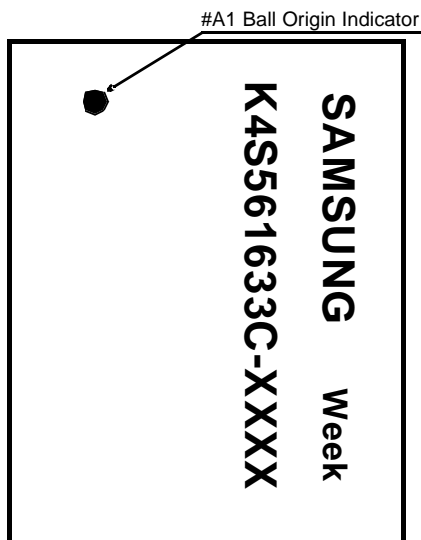
| 54Ball(6x9) CSP |                 |      |                  |                  |      |                 |
|-----------------|-----------------|------|------------------|------------------|------|-----------------|
|                 | 1               | 2    | 3                | 7                | 8    | 9               |
| A               | V <sub>SS</sub> | DQ15 | V <sub>SSQ</sub> | V <sub>DDQ</sub> | DQ0  | V <sub>DD</sub> |
| B               | DQ14            | DQ13 | V <sub>DDQ</sub> | V <sub>SSQ</sub> | DQ2  | DQ1             |
| C               | DQ12            | DQ11 | V <sub>SSQ</sub> | V <sub>DDQ</sub> | DQ4  | DQ3             |
| D               | DQ10            | DQ9  | V <sub>DDQ</sub> | V <sub>SSQ</sub> | DQ6  | DQ5             |
| E               | DQ8             | NC   | V <sub>SS</sub>  | V <sub>DD</sub>  | LDQM | DQ7             |
| F               | UDQM            | CLK  | CKE              | CAS              | RAS  | WE              |
| G               | A12             | A11  | A9               | BA0              | BA1  | CS              |
| H               | A8              | A7   | A6               | A0               | A1   | A10             |
| J               | V <sub>SS</sub> | A5   | A4               | A3               | A2   | V <sub>DD</sub> |

\*2: Top View



\*1: Bottom View

< Top View \*2 >



| Pin Name                           | Pin Function             |
|------------------------------------|--------------------------|
| CLK                                | System Clock             |
| CS                                 | Chip Select              |
| CKE                                | Clock Enable             |
| A <sub>0</sub> ~ A <sub>12</sub>   | Address                  |
| BA <sub>0</sub> ~ BA <sub>1</sub>  | Bank Select Address      |
| RAS                                | Row Address Strobe       |
| CAS                                | Column Address Strobe    |
| WE                                 | Write Enable             |
| L(U)DQM                            | Data Input/Output Mask   |
| DQ <sub>0</sub> ~ 15               | Data Input/Output        |
| V <sub>DD</sub> /V <sub>SS</sub>   | Power Supply/Ground      |
| V <sub>DDQ</sub> /V <sub>SSQ</sub> | Data Output Power/Ground |

[Unit:mm]

| Symbol         | Min  | Typ   | Max  |
|----------------|------|-------|------|
| A              | 0.90 | 0.95  | 1.00 |
| A <sub>1</sub> | 0.30 | 0.35  | 0.40 |
| E              | -    | 8.10  | -    |
| E <sub>1</sub> | -    | 6.40  | -    |
| D              | -    | 15.10 | -    |
| D <sub>1</sub> | -    | 6.40  | -    |
| e              | -    | 0.80  | -    |
| b              | 0.40 | 0.45  | 0.50 |
| z              | -    | -     | 0.10 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter   | Symbol                             | Value      | Unit |
|---|------------------------------------|------------|------|
| Voltage on any pin relative to V <sub>SS</sub>                | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 ~ 4.6 | V    |
| Voltage on V <sub>DD</sub> supply relative to V <sub>SS</sub> | V <sub>DD</sub> , V <sub>DDQ</sub> | -1.0 ~ 4.6 | V    |
| Storage temperature   | T <sub>STG</sub>                   | -55 ~ +150 | °C   |
| Power dissipation   | P <sub>D</sub>                     | 1          | W    |
| Short circuit current   | I <sub>OS</sub>                    | 50         | mA   |

## Notes :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>A</sub> = Commercial, Extended, Industrial Temperature)

| Parameter                 | Symbol           | Min  | Typ | Max                   | Unit | Note                   |
|---------------------------|------------------|------|-----|-----------------------|------|------------------------|
| Supply voltage            | V <sub>DD</sub>  | 2.7  | 3.0 | 3.6                   | V    |                        |
|                           | V <sub>DDQ</sub> | 2.7  | 3.0 | 3.6                   | V    |                        |
| Input logic high voltage  | V <sub>IH</sub>  | 2.2  | 3.0 | V <sub>DDQ</sub> +0.3 | V    | 1                      |
| Input logic low voltage   | V <sub>IL</sub>  | -0.3 | 0   | 0.5                   | V    | 2                      |
| Output logic high voltage | V <sub>OH</sub>  | 2.4  | -   | -                     | V    | I <sub>OH</sub> = -2mA |
| Output logic low voltage  | V <sub>OL</sub>  | -    | -   | 0.4                   | V    | I <sub>OL</sub> = 2mA  |
| Input leakage current     | I <sub>LI</sub>  | -10  | -   | 10                    | uA   | 3                      |

## Notes:

1. V<sub>IH</sub> (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.

2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.

Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.

4. Dout is disabled, 0V ≤ V<sub>OUT</sub> ≤ V<sub>DDQ</sub>.

CAPACITANCE (V<sub>DD</sub> = 3.0V & 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 0.9V ± 50 mV)

| Pin  | Symbol           | Min | Max | Unit | Note |
|--|------------------|-----|-----|------|------|
| Clock  | C <sub>CLK</sub> | 2.0 | 4.0 | pF   |      |
| $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{CS}}$ , CKE, DQM | C <sub>IN</sub>  | 2.0 | 4.0 | pF   |      |
| Address  | C <sub>ADD</sub> | 2.0 | 4.0 | pF   |      |
| DQ <sub>0</sub> ~ DQ <sub>15</sub>   | C <sub>OUT</sub> | 3.5 | 6.0 | pF   |      |

## DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to  $V_{SS} = 0V$ ,  $T_A = \text{Commercial, Extended, Industrial Temperature}$ )

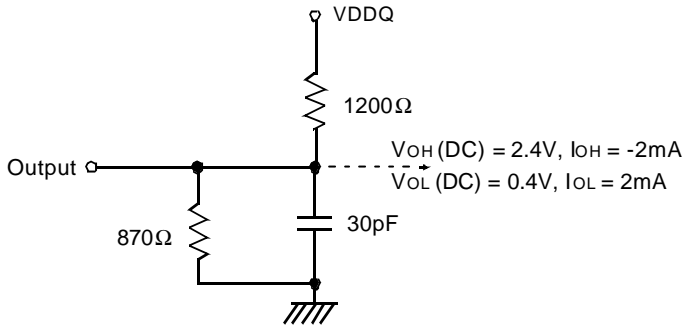
| Parameter   | Symbol             | Test Condition   | Version |     |     | Unit | Note   |   |
|---|--------------------|--|---------|-----|-----|------|--------|---|
|   |                    |  | -75     | -1H | -1L |      |        |   |
| Operating Current<br>(One Bank Active)                                | I <sub>CC1</sub>   | Burst length = 1<br>$t_{RC} \geq t_{RC}(\text{min})$<br>$I_o = 0 \text{ mA}$   | 90      | 85  | 85  | mA   | 1      |   |
| Precharge Standby Current<br>in power-down mode                       | I <sub>CC2P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 0.5     |     |     | mA   |        |   |
|   | I <sub>CC2PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 0.5     |     |     |      |        |   |
| Precharge Standby Current<br>in non power-down mode                   | I <sub>CC2N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 15      |     |     | mA   |        |   |
|   | I <sub>CC2NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 10      |     |     |      |        |   |
| Active Standby Current<br>in power-down mode                          | I <sub>CC3P</sub>  | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 10\text{ns}$  | 6       |     |     | mA   |        |   |
|   | I <sub>CC3PS</sub> | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$   | 6       |     |     |      |        |   |
| Active Standby Current<br>in non power-down mode<br>(One Bank Active) | I <sub>CC3N</sub>  | $\text{CKE} \geq V_{IH}(\text{min})$ , $\overline{\text{CS}} \geq V_{IH}(\text{min})$ , $t_{CC} = 10\text{ns}$<br>Input signals are changed one time during 20ns | 25      |     |     | mA   |        |   |
|   | I <sub>CC3NS</sub> | $\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$<br>Input signals are stable                                      | 25      |     |     |      |        |   |
| Operating Current<br>(Burst Mode)                                     | I <sub>CC4</sub>   | $I_o = 0 \text{ mA}$<br>Page burst<br>4Banks Activated<br>$t_{CCD} = 2\text{CLKs}$   | 130     | 130 | 105 | mA   | 1      |   |
| Refresh Current   | I <sub>CC5</sub>   | $t_{RC} \geq t_{RC}(\text{min})$   | 185     | 185 | 165 | mA   | 2      |   |
| Self Refresh Current  | I <sub>CC6</sub>   | $\text{CKE} \leq 0.2V$   | 800     |     |     | uA   | -R(B)L | 3 |
|   |                    |  |         |     |     |      | -R(B)N | 4 |
|   |                    |  |         |     |     |      | -R(B)P |   |

## Notes :

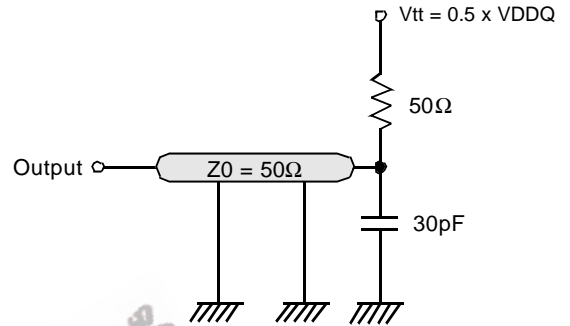
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S561633C-R(B)L\*\*
4. K4S561633C-R(B)N\*\*
5. K4S561633C-R(B)P\*\*
6. Unless otherwise noted, input swing level is CMOS( $V_{IH} / V_{IL} = V_{DDQ} / V_{SSQ}$ )

AC OPERATING TEST CONDITIONS (V<sub>DD</sub> = 2.7V ~ 3.6V, T<sub>A</sub> = Commercial, Extended, Industrial Temperature)

| Parameter   | Value                  | Unit |
|---|------------------------|------|
| AC input levels (V <sub>ih</sub> /V <sub>il</sub> ) | 2.4 / 0.4              | V    |
| Input timing measurement reference level            | 0.5 x V <sub>DDQ</sub> | V    |
| Input rise and fall time                            | tr/ff = 1/1            | ns   |
| Output timing measurement reference level           | 0.5 x V <sub>DDQ</sub> | V    |
| Output load condition                               | See Fig. 2             |      |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

| Parameter  | Symbol                 | Version                            |     |     | Unit | Note |
|--|------------------------|------------------------------------|-----|-----|------|------|
|  |                        | - 75                               | -1H | -1L |      |      |
| Row active to row active delay                           | t <sub>RRD</sub> (min) | 15                                 | 19  | 19  | ns   | 1    |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay | t <sub>RCD</sub> (min) | 19                                 | 19  | 24  | ns   | 1    |
| Row precharge time                                       | t <sub>RP</sub> (min)  | 19                                 | 19  | 24  | ns   | 1    |
| Row active time  | t <sub>RAS</sub> (min) | 45                                 | 50  | 60  | ns   | 1    |
|  | t <sub>RAS</sub> (max) | 100                                |     |     | us   |      |
| Row cycle time   | t <sub>RC</sub> (min)  | 65                                 | 70  | 84  | ns   | 1    |
| Last data in to row precharge                            | t <sub>RDL</sub> (min) | 2                                  |     |     | CLK  | 2,3  |
| Last data in to Active delay                             | t <sub>DAL</sub> (min) | t <sub>RDL</sub> + t <sub>RP</sub> |     |     | -    | 3    |
| Last data in to new col. address delay                   | t <sub>CDL</sub> (min) | 1                                  |     |     | CLK  | 2    |
| Last data in to burst stop                               | t <sub>BDL</sub> (min) | 1                                  |     |     | CLK  | 2    |
| Col. address to col. address delay                       | t <sub>CCD</sub> (min) | 1                                  |     |     | CLK  | 4    |
| Number of valid output data                              | CAS latency=3          | 2                                  |     |     | ea   | 5    |
|  | CAS latency=2          | 1                                  |     |     |      |      |
|  | CAS latency=1          | -                                  | 0   |     |      |      |

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum t<sub>RDL</sub>=2CLK and t<sub>DAL</sub>(=t<sub>RDL</sub> + t<sub>RP</sub>) is required to complete both of last data write command(t<sub>RDL</sub>) and precharge command(t<sub>RP</sub>). t<sub>RDL</sub>=1CLK can be supported only in the case under 100MHz with manual precharge mode.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

**AC CHARACTERISTICS**(AC operating conditions unless otherwise noted)

| Parameter                 |               | Symbol | - 75 |      | -1H |      | -1L |      | Unit | Note |
|---------------------------|---------------|--------|------|------|-----|------|-----|------|------|------|
|                           |               |        | Min  | Max  | Min | Max  | Min | Max  |      |      |
| CLK cycle time            | CAS latency=3 | tCC    | 7.5  | 1000 | 9.5 | 1000 | 9.5 | 1000 | ns   | 1    |
|                           | CAS latency=2 |        | 9.5  |      | 12  |      |     |      |      |      |
|                           | CAS latency=1 |        | -    |      | 25  |      |     |      |      |      |
| CLK to valid output delay | CAS latency=3 | tSAC   |      | 5.4  |     | 7    |     | 7    | ns   | 1,2  |
|                           | CAS latency=2 |        |      | 7    |     | 7    |     | 8    |      |      |
|                           | CAS latency=1 |        |      | -    |     | -    |     | 20   |      |      |
| Output data hold time     | CAS latency=3 | tOH    | 2.5  |      | 2.5 |      | 2.5 |      | ns   | 2    |
|                           | CAS latency=2 |        | 2.5  |      | 2.5 |      | 2.5 |      |      |      |
|                           | CAS latency=1 |        | -    |      | -   |      | 2.5 |      |      |      |
| CLK high pulse width      |               | tCH    | 2.5  |      | 3   |      | 3   |      | ns   | 3    |
| CLK low pulse width       |               | tCL    | 2.5  |      | 3   |      | 3   |      | ns   | 3    |
| Input setup time          |               | tSS    | 2.0  |      | 2.5 |      | 2.5 |      | ns   | 3    |
| Input hold time           |               | tSH    | 1.0  |      | 1.5 |      | 1.5 |      | ns   | 3    |
| CLK to output in Low-Z    |               | tSLZ   | 1    |      | 1   |      | 1   |      | ns   | 2    |
| CLK to output in Hi-Z     | CAS latency=3 | tSHZ   |      | 5.4  |     | 7    |     | 7    | ns   |      |
|                           | CAS latency=2 |        |      | 7    |     | 7    |     | 8    |      |      |
|                           | CAS latency=1 |        |      | -    |     | -    |     | 20   |      |      |

**Notes :**

- Parameters depend on programmed CAS latency.
- If clock rising time is longer than 1ns,  $(tr/2-0.5)$ ns should be added to the parameter.
- Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]$ ns should be added to the parameter.

**Note :**

- Samsung are not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in samsung electronics when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

## SIMPLIFIED TRUTH TABLE (V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

| COMMAND                            |                        | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | BA <sub>0,1</sub> | A <sub>10/AP</sub> | A <sub>11, A12, A9 ~ A0</sub>                    | Note |   |
|------------------------------------|------------------------|--------|------|-----------------|------------------|------------------|-----------------|-----|-------------------|--------------------|--|------|---|
| Register                           | Mode Register Set      | H      | X    | L               | L                | L                | L               | X   | OP CODE           |                    |  | 1, 2 |   |
| Refresh                            | Auto Refresh           | H      | H    | L               | L                | L                | H               | X   | X                 |                    |  | 3    |   |
|                                    | Entry                  |        | L    |                 |                  |                  |                 |     |                   |                    |  | 3    |   |
|                                    | Self Refresh           | Exit   | L    | H               | L                | H                | H               | H   | X                 | X                  |  |      | 3 |
|                                    |                        |        |      |                 | H                | X                | X               | X   |                   |                    |  |      | 3 |
| Bank Active & Row Addr.            |                        | H      | X    | L               | L                | H                | H               | X   | V                 | Row Address        |  |      |   |
| Read & Column Address              | Auto Precharge Disable | H      | X    | L               | H                | L                | H               | X   | V                 | L                  | Column Address (A <sub>0</sub> ~A <sub>8</sub> ) | 4    |   |
|                                    | Auto Precharge Enable  |        |      |                 |                  |                  |                 |     |                   | H                  |  | 4, 5 |   |
| Write & Column Address             | Auto Precharge Disable | H      | X    | L               | H                | L                | L               | X   | V                 | L                  | Column Address (A <sub>0</sub> ~A <sub>8</sub> ) | 4    |   |
|                                    | Auto Precharge Enable  |        |      |                 |                  |                  |                 |     |                   | H                  |  | 4, 5 |   |
| Burst Stop                         |                        | H      | X    | L               | H                | H                | L               | X   | X                 |                    |  | 6    |   |
| Precharge                          | Bank Selection         | H      | X    | L               | L                | H                | L               | X   | V                 | L                  | X  |      |   |
|                                    | All Banks              |        |      |                 |                  |                  |                 |     | X                 | H                  |  |      |   |
| Clock Suspend or Active Power Down | Entry                  | H      | L    | H               | X                | X                | X               | X   | X                 |                    |  |      |   |
|                                    |                        |        |      | L               | V                | V                | V               |     |                   |                    |  |      |   |
| Precharge Power Down Mode          | Entry                  | H      | L    | H               | X                | X                | X               | X   | X                 |                    |  |      |   |
|                                    |                        |        |      | L               | H                | H                | H               |     |                   |                    |  |      |   |
|                                    | Exit                   | L      | H    | H               | X                | X                | X               | X   | X                 |                    |  |      |   |
|                                    |                        |        |      | L               | V                | V                | V               |     |                   |                    |  |      |   |
| DQM                                |                        | H      | X    | X               |                  |                  |                 | V   | X                 |                    | 7  |      |   |
| No Operation Command               |                        | H      | X    | H               | X                | X                | X               | X   | X                 |                    |  |      |   |
|                                    |                        |        |      | L               | H                | H                | H               |     |                   |                    |  |      |   |

## Notes :

- OP Code : Operand Code  
A<sub>0</sub> ~ A<sub>12</sub> & BA<sub>0</sub> ~ BA<sub>1</sub> : Program keys. (@MRS)
- MRS can be issued only at all banks precharge state.  
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are the same as CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA<sub>0</sub> ~ BA<sub>1</sub> : Bank select addresses.  
If both BA<sub>0</sub> and BA<sub>1</sub> are "Low" at read, write, row active and precharge, bank A is selected.  
If BA<sub>0</sub> is "Low" and BA<sub>1</sub> is "High" at read, write, row active and precharge, bank B is selected.  
If BA<sub>0</sub> is "High" and BA<sub>1</sub> is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA<sub>0</sub> and BA<sub>1</sub> are "High" at read, write, row active and precharge, bank D is selected.  
If A<sub>10/AP</sub> is "High" at row precharge, BA<sub>0</sub> and BA<sub>1</sub> are ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at t<sub>RP</sub> after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).