

Document Title**2Mx16 bit Uni-Transistor Random Access Memory**Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|---------------------|---|-------------------|---------------|
| 0.0 | Initial Draft - Design target | September 4, 2000 | Advance |
| 0.1 | Revised - Change package type from FBGA to TBGA. - Improve operating current from 30mA to 25mA. - Change input and output reference voltage from 1.1V to 1.5V at AC test condition. - Expand max operating voltage from 3.0V to 3.3V. - Expand max operating temperature from 70°C to 85°C. - Release speed from 70/85ns to 100ns. - Release standby current form 170μA to 200μA. - Add Power up timing diagram. - Add AC characteristics for continuous write. | February 9, 2001 | Preliminary |
| 1.0 | Finalize - Release standby current form 200μA to 250μA. - Release deep power down current form 10μA to 20μA. - Release t _{wc} for continuous write operation from 100ns to 110ns. - Release t _{cw} for continuous write operation from 90ns to 100ns. - Release t _{aw} for continuous write operation from 90ns to 100ns. - Release t _{bw} for continuous write operation from 90ns to 100ns. - Release t _{wP} for continuous write operation from 90ns to 100ns. | March 30, 2001 | Final |
| 2.0 | Revised - Add product list | April 16, 2001 | Final |
| 3.0 | Revised - Improve standby current from 250μA to 150μA. | May 28, 2001 | Final |

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2M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 2M x16 bit
- Power Supply Voltage: 2.7~3.3V
- Three state output status
- Deep Power Down: Memory cell data hold invalid
- Package Type: 48-TBGA-9.00x12.00
- Compatible with Low Power SRAM

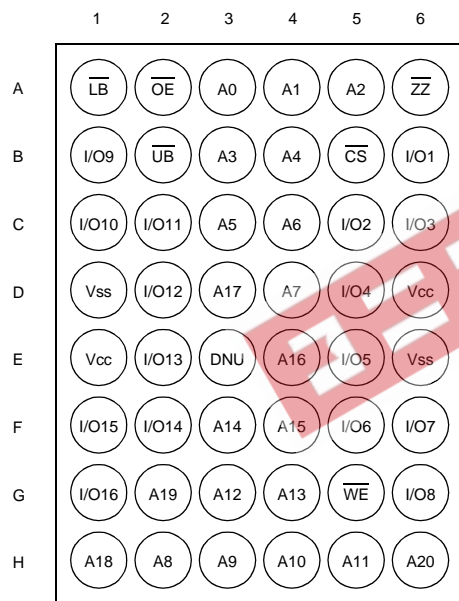
GENERAL DESCRIPTION

The K1S321615M is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device support, extended temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports deep power down mode for low standby current.

PRODUCT FAMILY

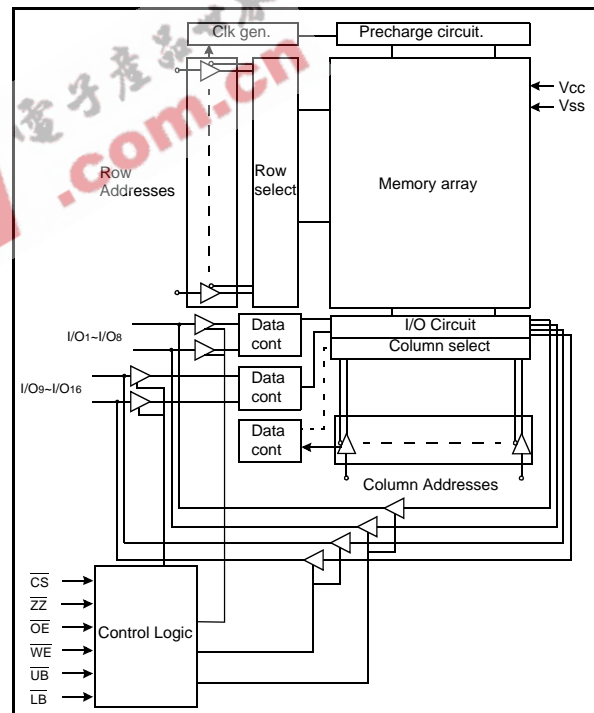
| Product Family | Operating Temp. | Vcc Range | Speed (trc) | Power Dissipation | | | PKG Type |
|----------------|--------------------|-----------|-------------|-----------------------------------|---|-------------------------------------|--------------------|
| | | | | Standby (I _{SB1} , Max.) | Deep power down(I _{SD} , Max.) | Operating (I _{CC2} , Max.) | |
| K1S321615M-E | Extended(-25~85°C) | 2.7~3.3V | 100ns | 150µA | 20µA | 25mA | 48-TBGA-9.00x12.00 |

PIN DESCRIPTION



48-TBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



| Name | Function | Name | Function |
|-------------------------------------|---------------------|-----------------|----------------------------------|
| \overline{CS} | Chip Select Input | Vcc | Power |
| \overline{ZZ} | Deep Power Down | Vss | Ground |
| \overline{OE} | Output Enable Input | \overline{UB} | Upper Byte(I/O ₉ ~16) |
| \overline{WE} | Write Enable Input | \overline{LB} | Lower Byte(I/O ₁ ~8) |
| A ₀ ~A ₂₀ | Address Inputs | DNU | Do Not Use ¹⁾ |
| I/O ₁ ~I/O ₁₆ | Data Inputs/Outputs | | |

1) Reserved for future user

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POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(V_{cc} min.=2.7V) for a minium 200μs with \overline{CS} =high.
3. Issue read operation at least twice.

FUNCTIONAL DESCRIPTION

| \overline{CS} | \overline{ZZ} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{UB} | I/O1-8 | I/O9-16 | Mode | Power |
|------------------|-----------------|------------------|------------------|------------------|------------------|--------|---------|------------------|-----------------|
| H | H | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | High-Z | High-Z | Deselected | Standby |
| X ⁽¹⁾ | L | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | High-Z | High-Z | Deselected | Deep Power Down |
| L | H | X ⁽¹⁾ | X ⁽¹⁾ | H | H | High-Z | High-Z | Deselected | Standby |
| L | H | H | H | L | X ⁽¹⁾ | High-Z | High-Z | Output Disabled | Active |
| L | H | H | H | X ⁽¹⁾ | L | High-Z | High-Z | Output Disabled | Active |
| L | H | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | Word Read | Active |
| L | H | X ⁽¹⁾ | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | H | X ⁽¹⁾ | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | H | X ⁽¹⁾ | L | L | L | Din | Din | Word Write | Active |

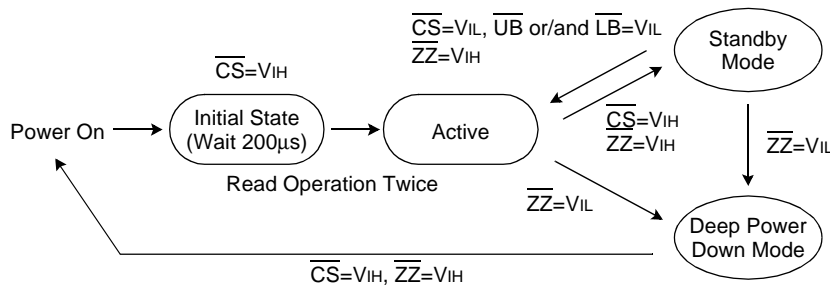
1. X means dont care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Item | Symbol | Ratings | Unit |
|---|------------------------------------|-------------------------------|------|
| Voltage on any pin relative to V _{ss} | V _{IN} , V _{OUT} | -0.2 to V _{cc} +0.3V | V |
| Voltage on V _{cc} supply relative to V _{ss} | V _{cc} | -0.2 to 3.6V | V |
| Power Dissipation | P _D | 1.0 | W |
| Storage temperature | T _{STG} | -65 to 150 | °C |
| Operating Temperature | T _A | -25 to 85 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions longer than 1seconds may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

| Power Mode | Memory Cell Data | Standby Current(mA) | Wait Time(μs) |
|-----------------|------------------|---------------------|---------------|
| Standby | Valid | 150 | 0 |
| Deep Power Down | Invaield | 20 | 200 |

PRODUCT LIST

| Extended Temperature Products(-25~85°C) | |
|---|-----------------------------------|
| Part Name | Function |
| K1S321615M-EE10 | 48-TBGA with 48 ball, 100ns, 3.0V |

RECOMMENDED DC OPERATING CONDITIONS¹⁾

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|------------------------------------|------|
| Supply voltage | V _{CC} | 2.7 | 3.0 | 3.3 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input high voltage | V _{IH} | 2.2 | - | V _{CC} +0.2 ²⁾ | V |
| Input low voltage | V _{IL} | -0.2 ³⁾ | - | 0.6 | V |

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance | C _{IN} | V _{IN} =0V | - | 8 | pF |
| Input/Output capacitance | C _{IO} | V _{IO} =0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

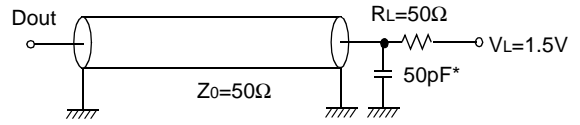
| Item | Symbol | Test Conditions | Min | Typ ¹⁾ | Max | Unit |
|---------------------------|------------------|---|-----|-------------------|-----|------|
| Input leakage current | I _{LI} | V _{IN} =V _{SS} to V _{CC} | -1 | - | 1 | μA |
| Output leakage current | I _{LO} | $\overline{CS}=V_{IH}, \overline{ZZ}=V_{IH}, \overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}, V_{IO}=V_{SS}$ to V _{CC} | -1 | - | 1 | μA |
| Average operating current | I _{CC1} | Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS} \leq 0.2V$, $\overline{ZZ} \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V | - | 2 | 5 | mA |
| | I _{CC2} | Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}=V_{IL}, \overline{ZZ}=V_{IH}, V_{IN}=V_{IL}$ or V _{IH} | - | 18 | 25 | mA |
| Output low voltage | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | V |
| Output high voltage | V _{OH} | I _{OH} =-1.0mA | 2.4 | - | - | V |
| Standby Current(CMOS) | I _{SB1} | $\overline{CS} \geq V_{CC}-0.2V, \overline{ZZ} \geq V_{CC}-0.2V$, Other inputs=V _{SS} to V _{CC} | - | 120 | 150 | μA |
| Deep Power Down | I _{SD} | $\overline{ZZ} \leq 0.2V$, Other inputs=V _{SS} to V _{CC} | - | 5 | 20 | μA |

1. Typical values are tested at V_{CC}=3.0V, T_A=25°C and not guaranteed.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load(See right): CL=50pF



* Include scope and jig capacitance

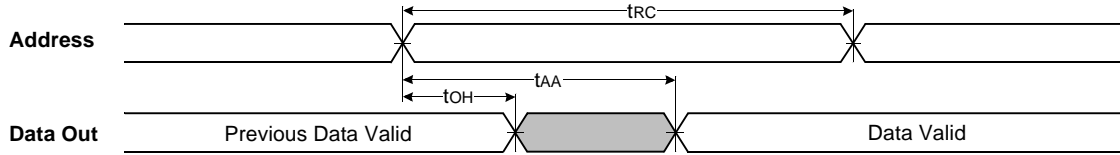
AC CHARACTERISTICS(V_{CC}=2.7~3.3V, T_A=-25 to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | Units |
|----------------|--|------------------|---------------------|-----|---------------------|-----|-------|
| | | | 100ns ¹⁾ | | 100ns ²⁾ | | |
| | | | Min | Max | Min | Max | |
| Read | Read Cycle Time | t _{RC} | 100 | - | 100 | - | ns |
| | Address Access Time | t _{AA} | - | 100 | - | 100 | ns |
| | Chip Select to Output | t _{CO} | - | 100 | - | 100 | ns |
| | Output Enable to Valid Output | t _{OE} | - | 50 | - | 50 | ns |
| | \overline{UB} , \overline{LB} Access Time | t _{BA} | - | 100 | - | 100 | ns |
| | Chip Select to Low-Z Output | t _{LZ} | 10 | - | 10 | - | ns |
| | \overline{UB} , \overline{LB} Enable to Low-Z Output | t _{BLZ} | 10 | - | 10 | - | ns |
| | Output Enable to Low-Z Output | t _{OLZ} | 5 | - | 5 | - | ns |
| | Chip Disable to High-Z Output | t _{HZ} | 0 | 25 | 0 | 25 | ns |
| | \overline{UB} , \overline{LB} Disable to High-Z Output | t _{BHZ} | 0 | 25 | 0 | 25 | ns |
| | Output Disable to High-Z Output | t _{OHZ} | 0 | 25 | 0 | 25 | ns |
| | Output Hold from Address Change | t _{OH} | 5 | - | 5 | - | ns |
| Write | Write Cycle Time | t _{WC} | 100 | - | 110 | - | ns |
| | Chip Select to End of Write | t _{CW} | 80 | - | 100 | - | ns |
| | Address Set-up Time | t _{AS} | 0 | - | 0 | - | ns |
| | Address Valid to End of Write | t _{AW} | 80 | - | 100 | - | ns |
| | \overline{UB} , \overline{LB} Valid to End of Write | t _{BW} | 80 | - | 100 | - | ns |
| | Write Pulse Width | t _{WP} | 70 | - | 100 | - | ns |
| | Write Recovery Time | t _{WR} | 0 | - | 0 | - | ns |
| | Write to Output High-Z | t _{WHZ} | 0 | 30 | 0 | 30 | ns |
| | Data to Write Time Overlap | t _{DW} | 40 | - | 40 | - | ns |
| | Data Hold from Write Time | t _{DH} | 0 | - | 0 | - | ns |
| | End Write to Output Low-Z | t _{OW} | 5 | - | 5 | - | ns |

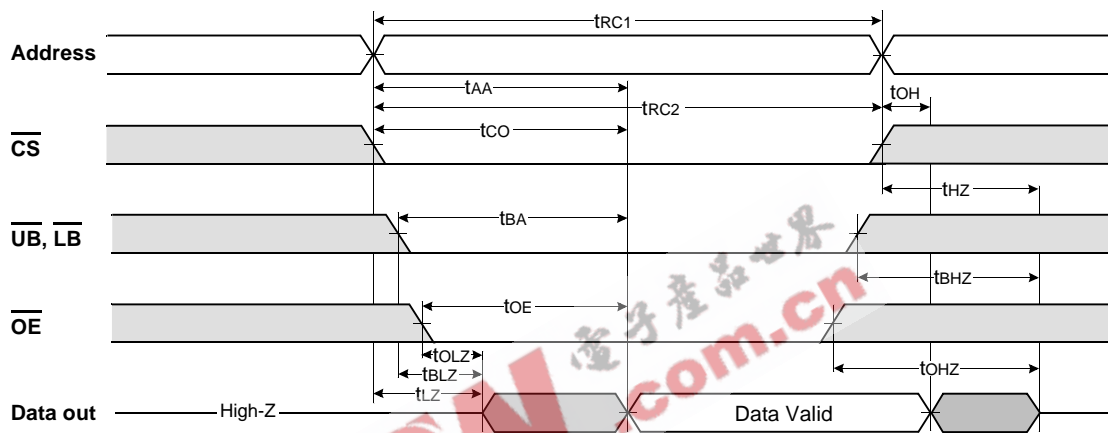
1. The characteristics which is restricted for continuous write operation over 20 times, please refer to technical note.
 2. The characteristics for continuous write operation.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{ZZ}=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



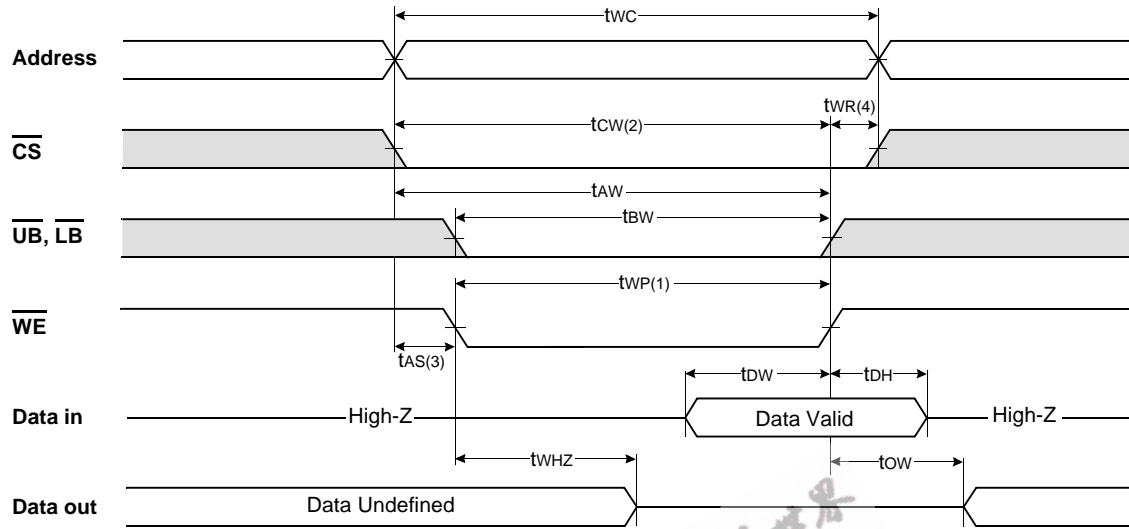
TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}=\overline{WE}=V_{IH}$)



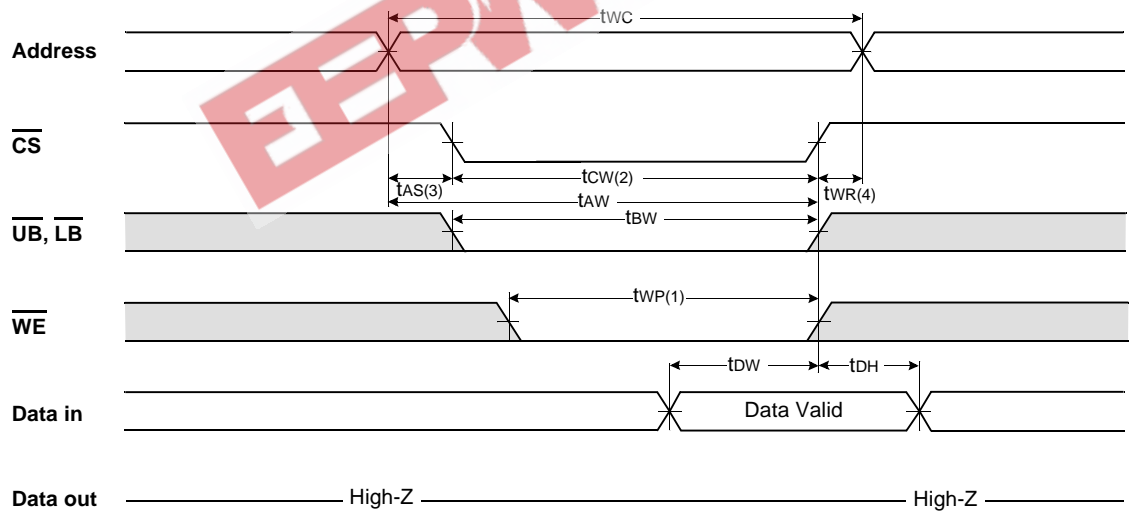
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined later one of the t_{RC1} and t_{RC2} .

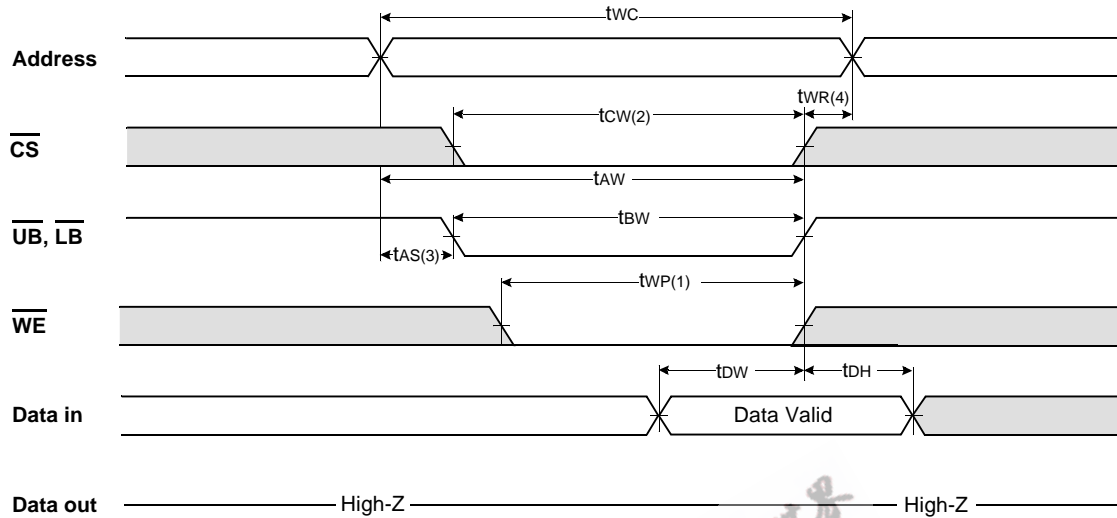
TIMING WAVEFORM OF WRITE CYCLE(1)(\overline{WE} Controlled, $\overline{ZZ}=V_{IH}$)



TIMING WAVEFORM OF WRITE CYCLE(2)(\overline{CS} Controlled, $\overline{ZZ}=V_{IH}$)



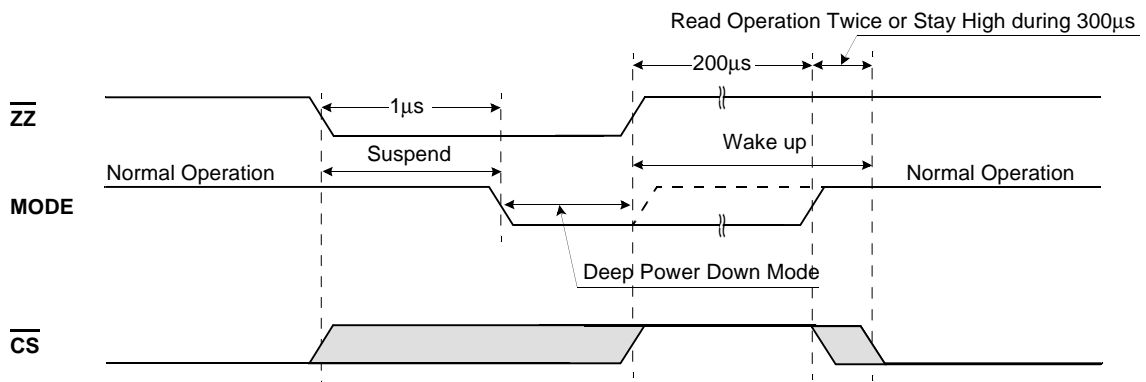
TIMING WAVEFORM OF WRITE CYCLE(3)(\overline{UB} , \overline{LB} Controlled, $\overline{ZZ}=V_{IH}$)



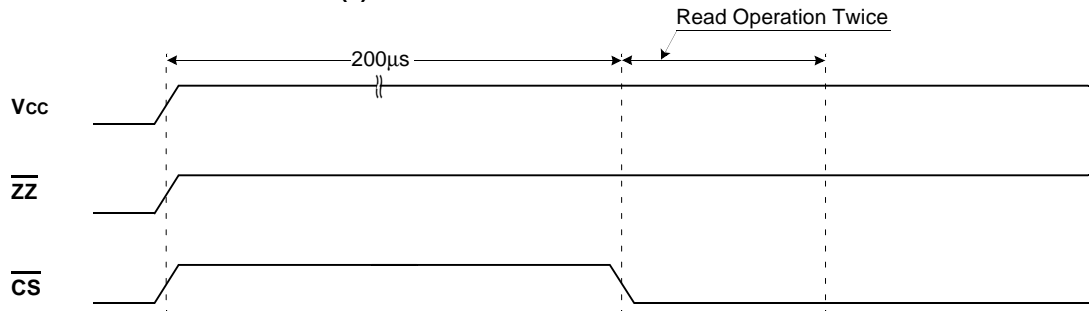
(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

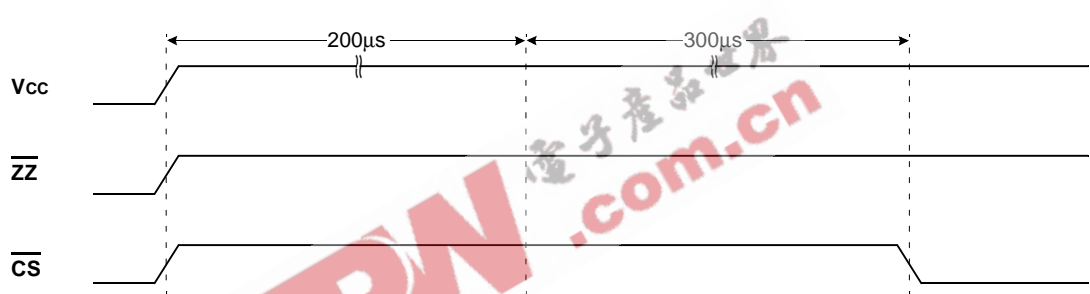
TIMING WAVEFORM OF DEEP POWER DOWN MODE



TIMING WAVEFORM OF POWER UP(1)



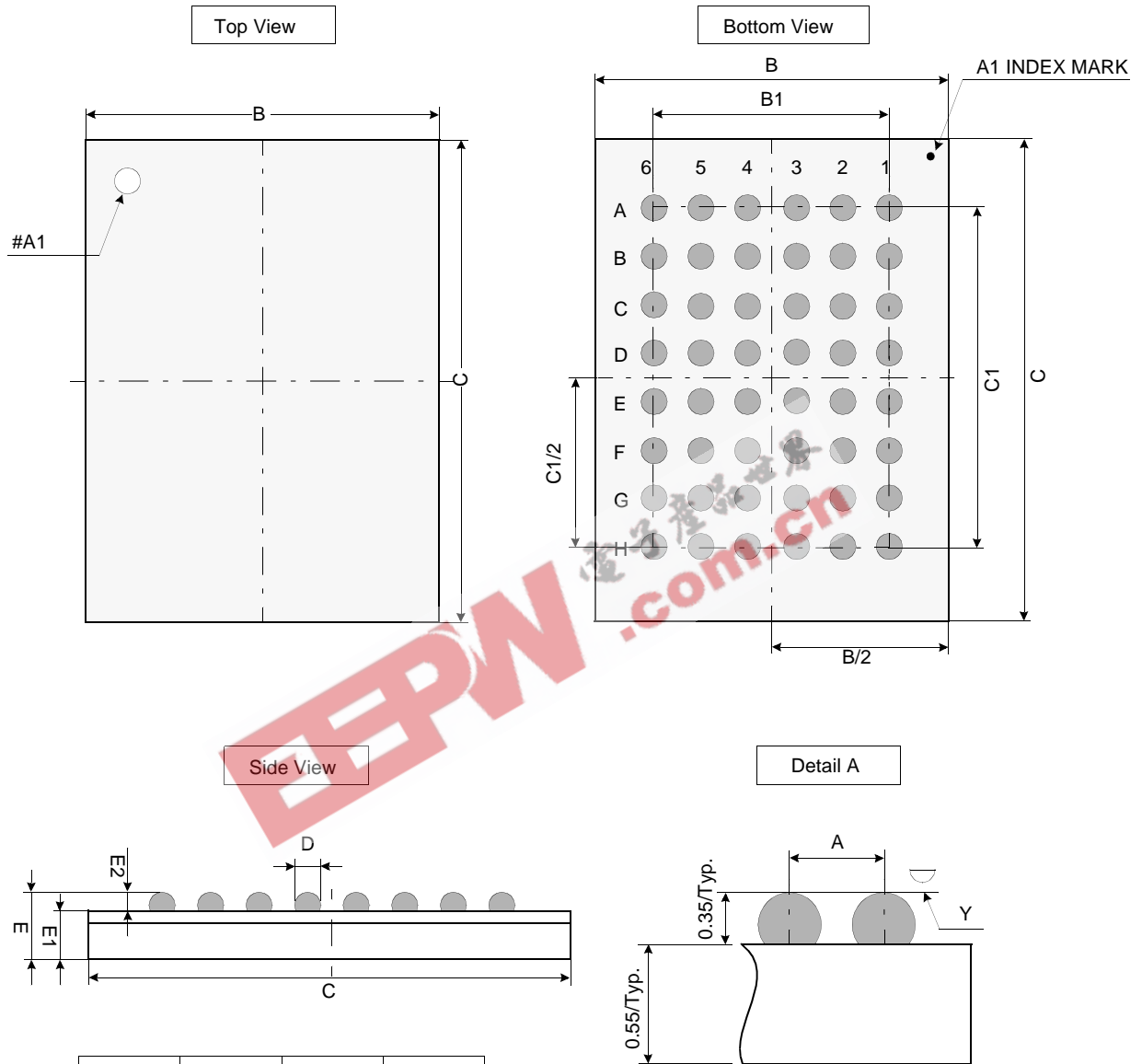
TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)



PACKAGE DIMENSION

Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)



| | Min | Typ | Max |
|----|-------|-------|-------|
| A | - | 0.75 | - |
| B | 8.90 | 9.00 | 9.10 |
| B1 | - | 3.75 | - |
| C | 11.90 | 12.00 | 12.10 |
| C1 | - | 5.25 | - |
| D | 0.40 | 0.45 | 0.50 |
| E | - | 0.90 | 1.00 |
| E1 | - | 0.55 | - |
| E2 | 0.30 | 0.35 | 0.40 |
| Y | - | - | 0.08 |

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)

TECHNICAL NOTE

U τ RAM USAGE AND TIMING

INTRODUCTION

U τ RAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the U τ RAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

The key to the U τ RAM is its high speed and low power. This speed comes from the use of many small blocks, often just 32Kbits each, to create U τ RAM arrays. The small blocks have short word lines with little capacitance, eliminating a major source of operating current in conventional DRAM blocks.

Each independent macro-cell on a U τ RAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. U τ RAM perform a complete read operation in every tRC, but U τ RAM needs power up sequence like a DRAM.

Power Up Sequence and Diagram

1. Apply power.
2. Maintain stable power for a minimum 200 μ s with \overline{CS} =high.
3. Issue read operation at least 2 times.

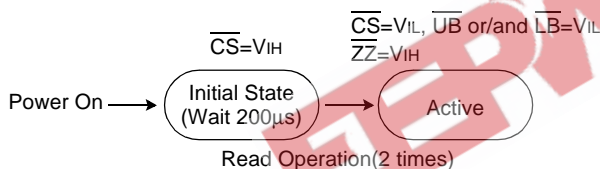


Figure 1.

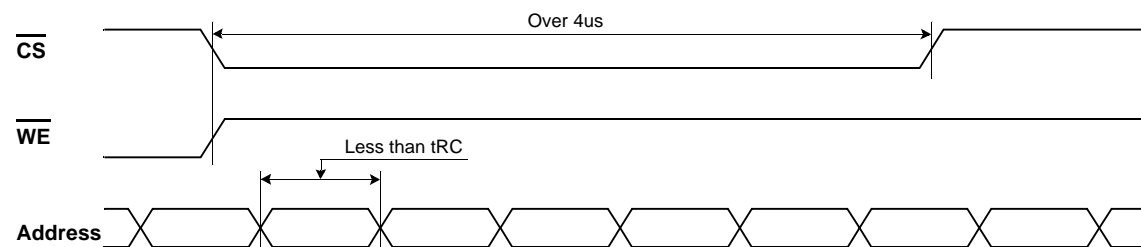
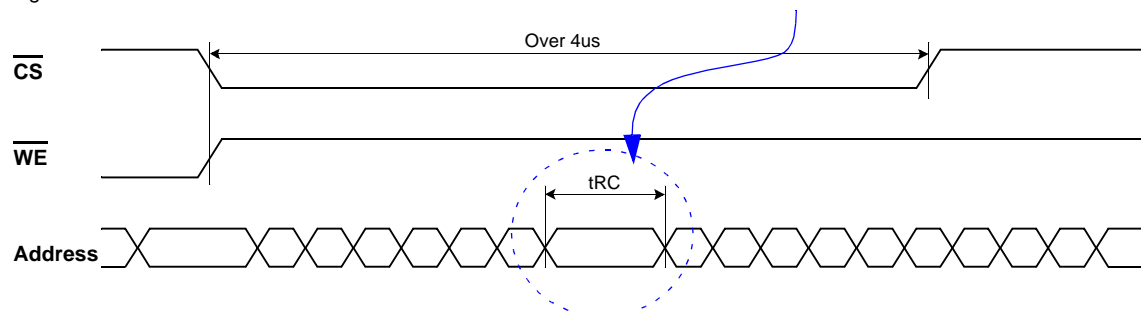


Figure 2.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The U τ RAM design works just like an SRAM, with no wait states or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations with advanced design. Precharging takes place during every access, overlapped with the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult, Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides a internal refresh controller for devices. When all accesses during a refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM, sometimes used on these applications, which is required a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the U τ RAM never needs to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

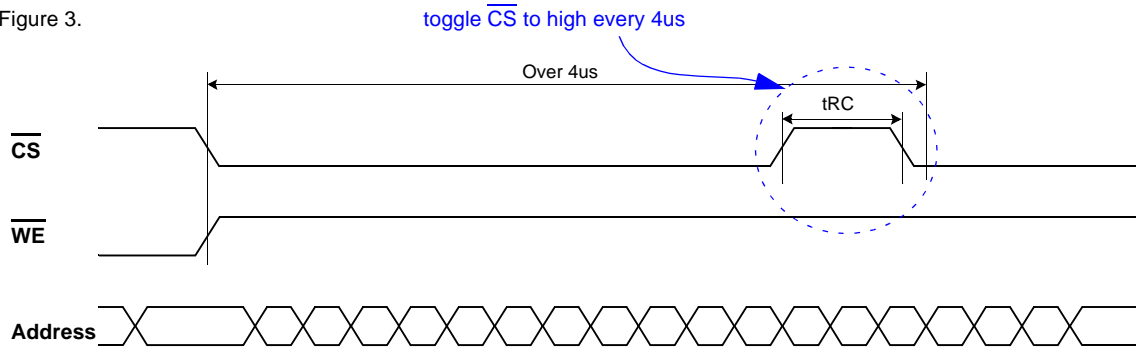
AVOID TIMING

Following figures are show you a abnormal timing which is not supported on U τ RAM and their solution.

At read operation, if your system have a timing which sustain invalid states over 4us at read mode like Figure 1. There are some guide line for proper operation of U τ RAM.

When your system have multiple invalid address signal shorter than tRC on the timing which showed in Figure 1, U τ RAM need a normal read timing during that cycle(Figure 2) or toggle the \overline{CS} to high about tRC(Figure 3).

Figure 3.



Write operation have similar restricted operation with Read. If your system have a timing which sustain invalid states over 4us at write mode and system have continuous write signal with Min. t_{WC} over 4us like Figure 4.

You must put read timing on the cycle(Figure 5) or toggle the CS to high about t_{RC} (Figure 6).

Figure 4.

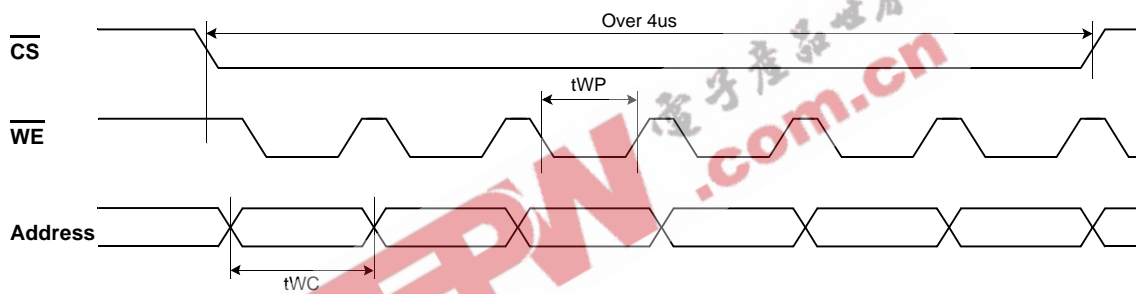


Figure 5.

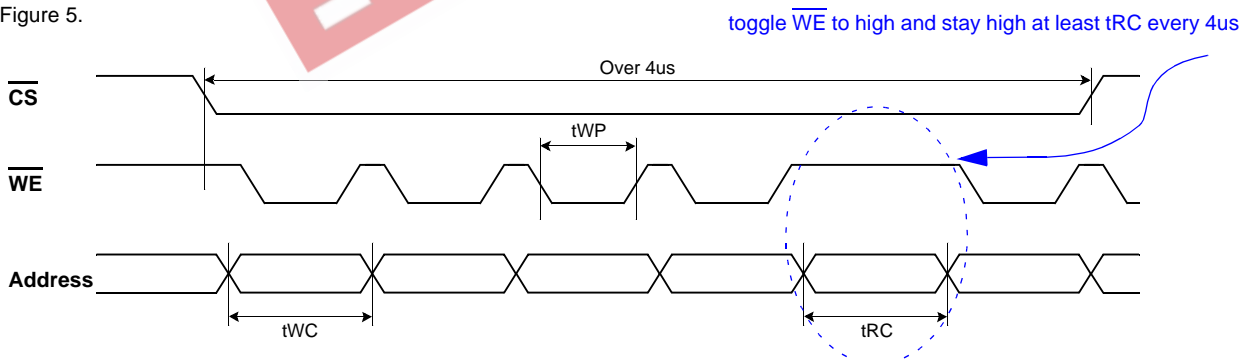


Figure 6.

