

K7P403622M
K7P401822M

128Kx36 & 256Kx18 SRAM

Document Title

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
Rev. 0.0	- Preliminary specification release		Preliminary
Rev. 0.1	- Change specification format. No change was made in parameters.	April, 1997	Preliminary
Rev. 0.2	- Updated IDD, I _{sb} and Input High Level. Updated t _{KHKL} , t _{KLKH} , t _{KHQX} , t _{KHQX1} and AC Test Conditions. For JTAG, updated Vendor Definition and added tsvch/tchsx.	Jan. 1998	Preliminary
Rev. 1.0	- Final specification release	Dec. 1998	Final

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128Kx36 & 256Kx18 SRAM

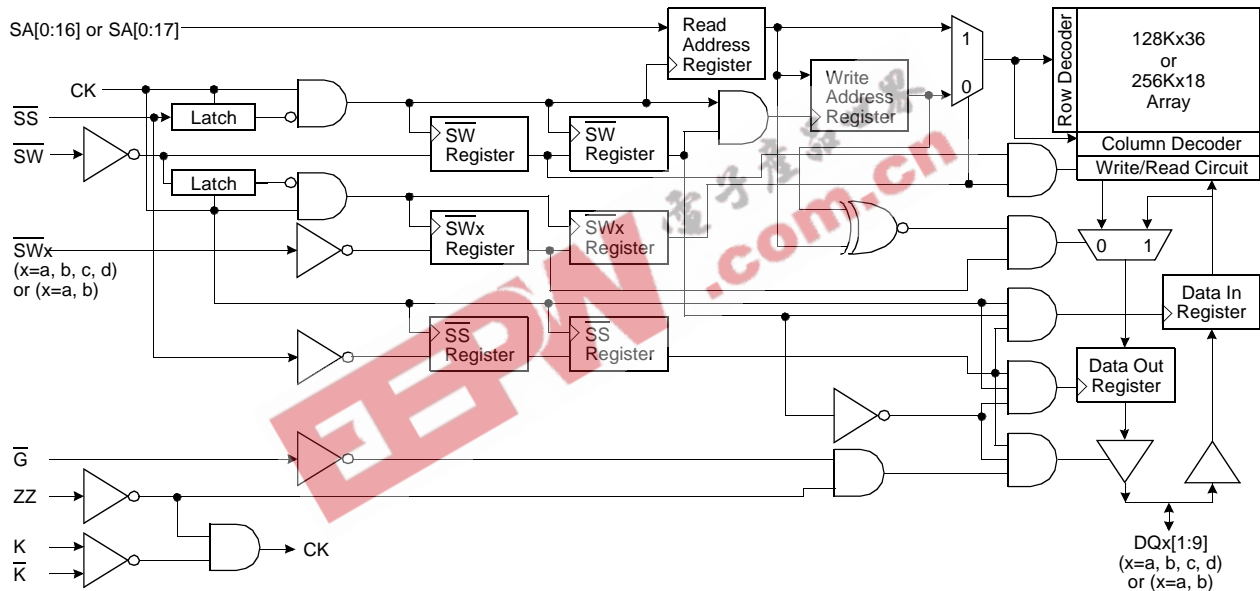
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V Core Power Supply.
- LVTTTL Input and Output Levels.
- Differential, PECL Clock Inputs K, \bar{K} .
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm)

Organization	Part Number	Cycle Time	Access Time
128Kx36	K7P403622M-H20	5	2.5
	K7P403622M-H16	6	3.0
	K7P403622M-H19	7	3.5
256Kx18	K7P401822M-H20	5	2.5
	K7P401822M-H16	6	3.0
	K7P401822M-H19	7	3.5

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, \bar{K}	Differential Clocks	VDDQ	Output Power Supply
SA _n	Synchronous Address Input	M1, M2	Read Protocol Mode Pins (M1=VSS, M2=VDD)
DQ _n	Bi-directional Data Bus	\bar{G}	Asynchronous Output Enable
\bar{SW}	Synchronous Global Write Enable	\bar{SS}	Synchronous Select
\bar{SW}_a	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
\bar{SW}_b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
\bar{SW}_c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
\bar{SW}_d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	VSS	GND
VDD	Core Power Supply	NC	No Connection

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128Kx36 & 256Kx18 SRAM

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P403622M(128Kx36)

	1	2	3	4	5	6	7
A	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
B	NC	NC	SA9	NC	SA8	NC	NC
C	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQc8	DQc9	VSS	NC	VSS	DQb9	DQb8
E	DQc6	DQc7	VSS	\overline{SS}	VSS	DQb7	DQb6
F	VDDQ	DQc5	VSS	\overline{G}	VSS	DQb5	VDDQ
G	DQc3	DQc4	\overline{SWc}	NC	\overline{SWb}	DQb4	DQb3
H	DQc1	DQc2	VSS	NC	VSS	DQb2	DQb1
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd1	DQd2	VSS	K	VSS	DQa2	DQa1
L	DQd3	DQd4	\overline{SWd}	\overline{K}	\overline{SWa}	DQa4	DQa3
M	VDDQ	DQd5	VSS	\overline{SW}	VSS	DQa5	VDDQ
N	DQd6	DQd7	VSS	SA16	VSS	DQa7	DQa6
P	DQd8	DQd9	VSS	SA0	VSS	DQa9	DQa8
R	NC	SA15	M1	VDD	M2	SA2	NC
T	NC	NC	SA14	SA1	SA3	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

K7P401822M(256Kx18)

	1	2	3	4	5	6	7
A	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
B	NC	NC	SA9	NC	SA8	NC	NC
C	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQb1	NC	VSS	NC	VSS	DQa9	NC
E	NC	DQb2	VSS	\overline{SS}	VSS	NC	DQa8
F	VDDQ	NC	VSS	\overline{G}	VSS	DQa7	VDDQ
G	NC	DQb3	\overline{SWb}	NC	NC	NC	DQa6
H	DQb4	NC	VSS	NC	VSS	DQa5	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb5	VSS	K	VSS	NC	DQa4
L	DQb6	NC	NC	\overline{K}	\overline{SWa}	DQa3	NC
M	VDDQ	DQb7	VSS	\overline{SW}	VSS	NC	VDDQ
N	DQb8	NC	VSS	SA16	VSS	DQa2	NC
P	NC	DQb9	VSS	SA1	VSS	NC	DQa1
R	NC	SA15	M1	VDD	M2	SA2	NC
T	NC	SA17	SA14	NC	SA3	SA0	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The K7P403622M and K7P401822M are 4,718,592 bit Synchronous Pipeline Mode SRAM. It is organized as 131,072 words of 36 bits (or 262, 144 words of 18 bits) and is implemented in SAMSUNG's advanced CMOS technology. Single differential PECL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During reads, the address is registered during the first clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. \overline{SS} is driven low during this cycle, signaling that the SRAM should drive out the data.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and \overline{SW} are sampled on the clock rising edge. \overline{SW} is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and \overline{SW} have been sampled by the SRAM. \overline{SS} will be driven low during the same cycle that the Address, \overline{SW} and $\overline{SW}[a:d]$ are valid to signal that a valid operation is on the Address and Control Input.

Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}[a:d]$ signal which 9-bit bytes will be written. Timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Low Power Dissipation Mode

During normal operation, asynchronous signal ZZ must be pulled low. Low Power Mode is enabled by switching ZZ high. When the SRAM is in Power Down Mode, the outputs will go to a Hi-Z state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (tZZR) is required before the SRAM resumes to normal operation.

TRUTH TABLE

K	ZZ	\overline{G}	\overline{SS}	\overline{SW}	\overline{SWa}	\overline{SWb}	\overline{SWc}	\overline{SWd}	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all byte

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.9	V	
Output Supply Voltage Relative to Vss	VDDQ	VDD	V	
Voltage on any I/O pin Relative to Vss	VTERM	-0.5 to VDD+0.5	V	
Maximum Power Dissipation	Pd	3	W	
Output Short-Circuit Current	IOUT	25	mA	
Operating Temperature	TOPR	0 to 70	°C	
Storage Temperature	TSTG	-55 to 125	°C	

NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	V	
Output Power Supply Voltage	VDDQ	2.35	2.5	3.45	V	
Input High Level	VIH	1.7	-	VDD+0.3	V	
Input Low Level	VIL	-0.3	-	0.7	V	
PECL Clock Input High Level	VIH-PECL	2.135	-	2.420	V	
PECL Clock Input Low Level	VIL-PECL	1.490	-	1.825	V	
Operating Junction Temperature	TJ	10	-	110	°C	

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD5 IDD6 IDD7	-	650 600 550	mA	1, 2
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD5 IDD6 IDD7	-	600 550 500	mA	1, 2
Power Supply Standby Current (VIN=VIH or VIL, ZZ=VIH)	ISB	-	60	mA	1
Input Leakage Current (VIN=Vss or VDD)	ILI	-1	1	μA	
Output Leakage Current (VOUT=Vss or VDDQ, ZZ=VIH, \bar{G} =VIH)	ILO	-1	1	μA	
Output High Voltage(IoH=-4mA) for VDDQ=3.3V	VOH1	2.4	VDDQ	V	
Output High Voltage(IoH=-4mA) for VDDQ=2.5V	VOH2	2.0			
Output Low Voltage(IoL=4mA)	VOL	Vss	0.4	V	

NOTE : 1. Minimum cycle. IOUT=0mA.
2. 50% read cycles.

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PIN CAPACITANCE

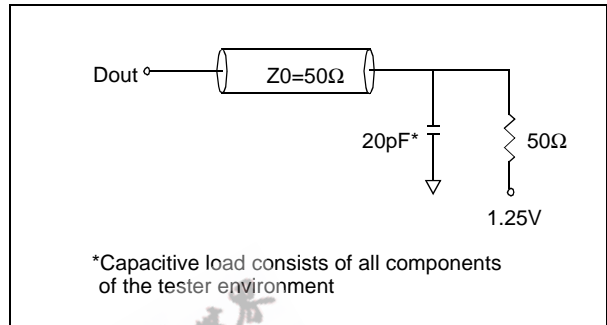
Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C _{IN}	4	5	pF
Output Capacitance	C _{OUT}	7	8	pF

NOTE : Periodically sampled and not 100% tested.(dV=0V, f=1MHz)

AC TEST CONDITIONS

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V _{DD}	3.15~3.45	V
Output Power Supply Voltage	V _{DDQ}	2.4~2.6	V
Input High/Low Level	V _{IH} /V _{IL}	1.7/0.7	V
Clock Input High/Low Level(PECL)	V _{IH} /V _{IL}	2.4/1.5	V
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns
Clock Input Rise/Fall Time(PECL)	T _R /T _F	1.0/1.0	ns
Input and Out Timing Reference Level		1.25	V
Clock Input Timing Reference Level		Cross Point	V

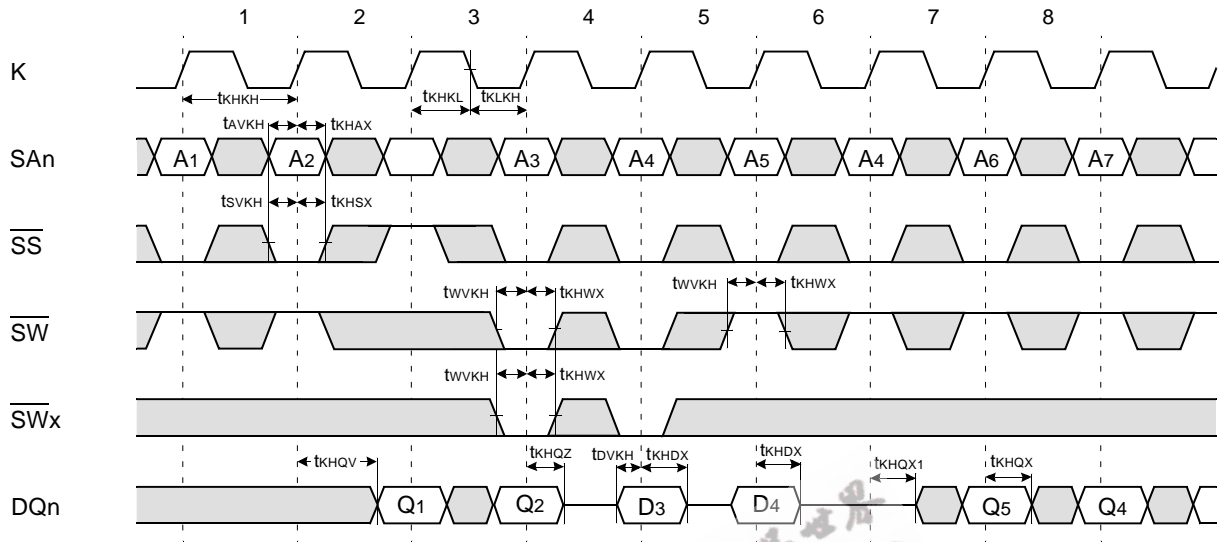
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol	-20		-16		-19		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t _{KHKH}	5.0	-	6.0	-	7.0	-	ns	
Clock High Pulse Width	t _{KHKL}	1.5	-	1.5	-	1.5	-	ns	
Clock Low Pulse Width	t _{KLKH}	1.5	-	1.5	-	1.5	-	ns	
Clock High to Output Valid	t _{KHQV}	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Hold	t _{KHQX}	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t _{AVKH}	0.5	-	0.5	-	0.5	-	ns	
Address Hold Time	t _{KHAX}	1.0	-	1.0	-	1.0	-	ns	
Write Data Setup Time	t _{DVKH}	0.5	-	0.5	-	0.5	-	ns	
Write Data Hold Time	t _{KHDX}	1.0	-	1.0	-	1.0	-	ns	
\overline{SW} , $\overline{SW}[a:d]$ Setup Time	t _{WVKH}	0.5	-	0.5	-	0.5	-	ns	
\overline{SW} , $\overline{SW}[a:d]$ Hold Time	t _{KHWX}	1.0	-	1.0	-	1.0	-	ns	
\overline{SS} Setup Time	t _{SVKH}	0.5	-	0.5	-	0.5	-	ns	
\overline{SS} Hold Time	t _{KHSX}	1.0	-	1.0	-	1.0	-	ns	
Clock High to Output Hi-Z	t _{KHQZ}	-	2.5	-	3.0	-	3.5	ns	
Clock High to Output Low-Z	t _{KHQX1}	0.5	-	0.5	-	0.5	-	ns	
\overline{G} High to Output High-Z	t _{GHQZ}	-	2.5	-	3.0	-	3.5	ns	
\overline{G} Low to Output Low-Z	t _{GLQX}	0.5	-	0.5	-	0.5	-	ns	
\overline{G} Low to Output Valid	t _{GLQV}	-	2.5	-	3.0	-	3.5	ns	
ZZ High to Power Down(Sleep Time)	t _{ZZE}	-	5.0	-	6.0	-	7.0	ns	
ZZ Low to Recovery(Wake-up Time)	t _{ZZR}	-	5.0	-	6.0	-	7.0	ns	

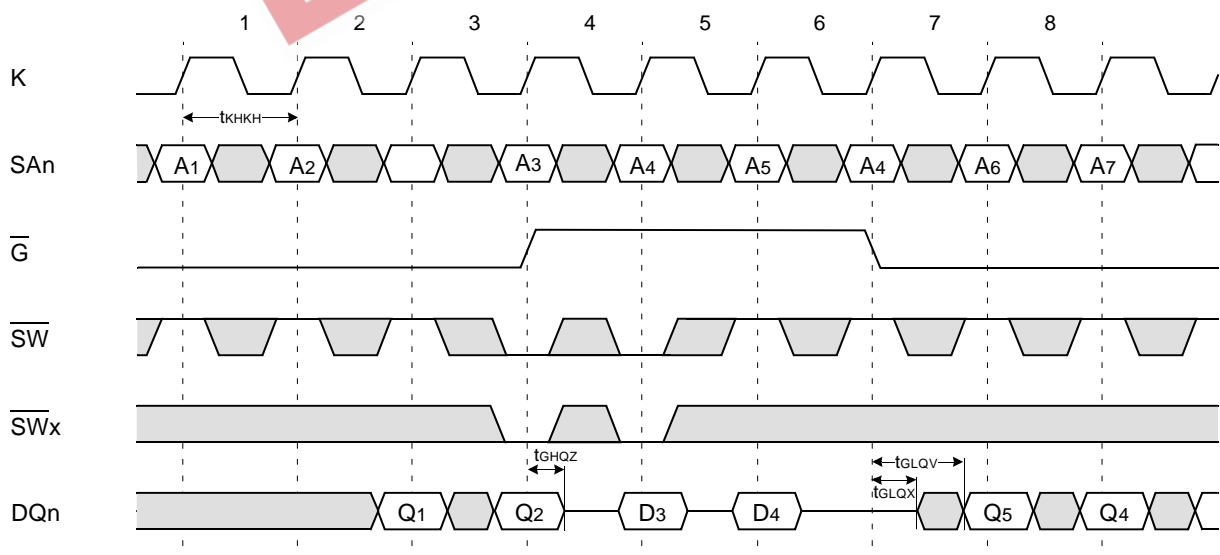
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{SS} Controlled, $\overline{G}=Low$)



NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

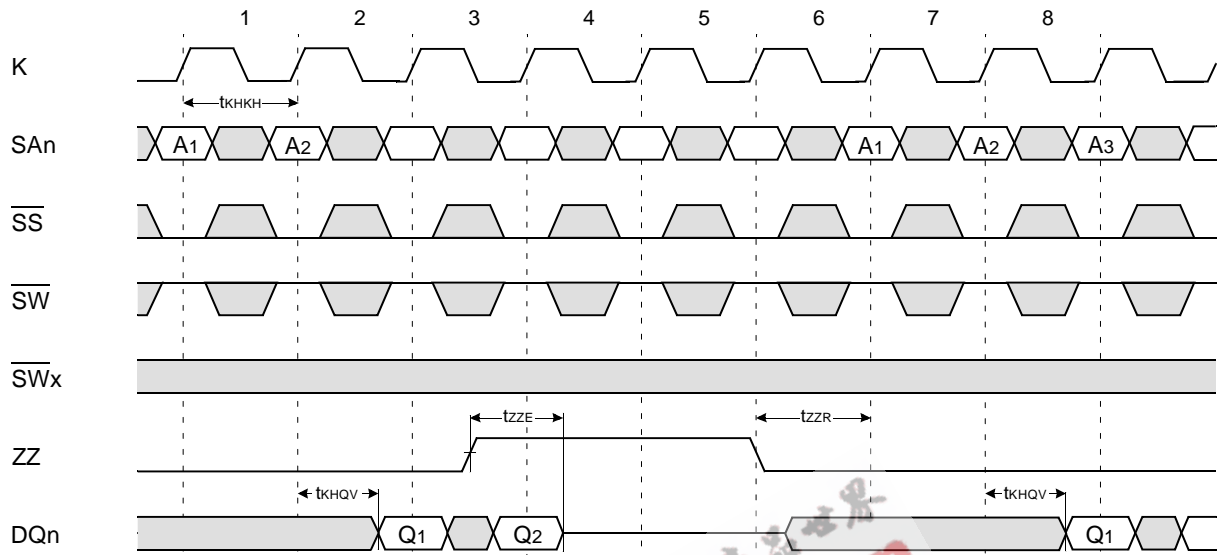
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{G} Controlled, $\overline{SS}=Low$)



NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

TIMING WAVEFORMS OF STANDBY CYCLES

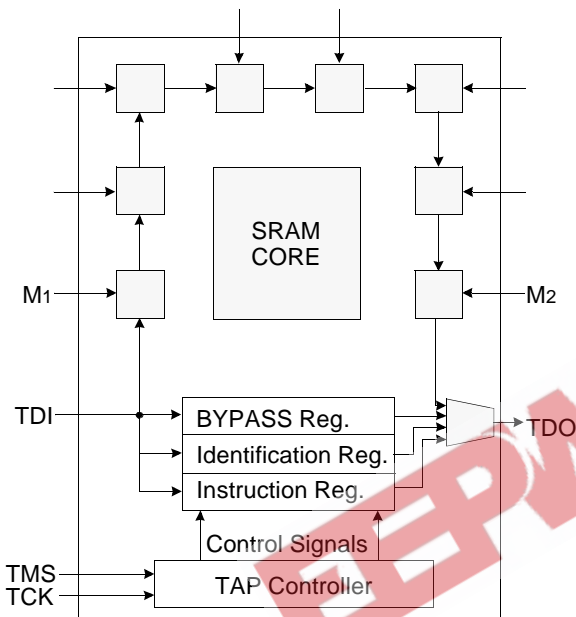


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IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



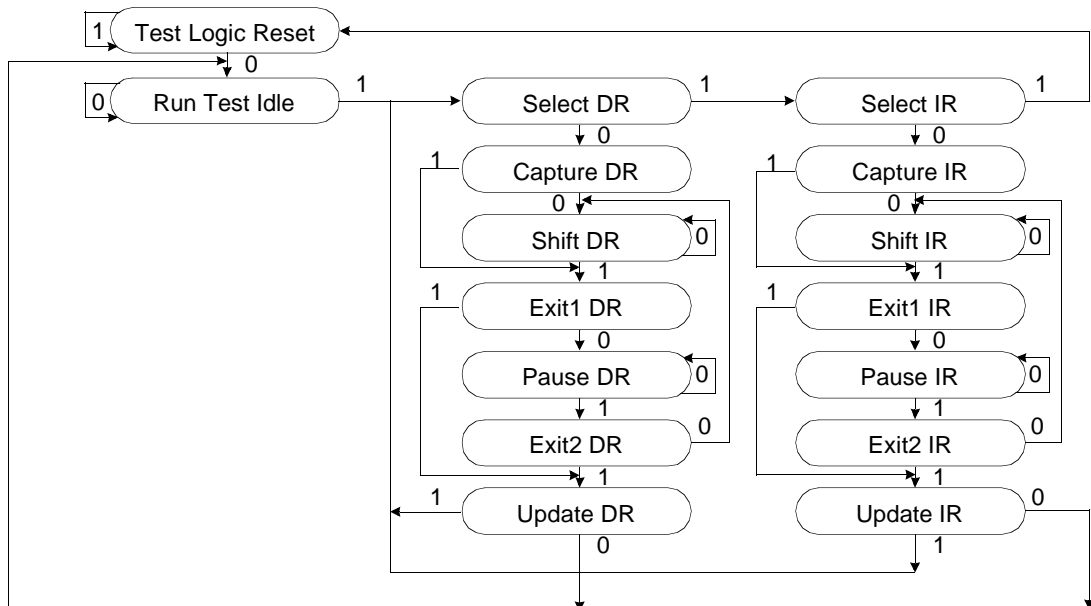
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



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128Kx36 & 256Kx18 SRAM

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	70 bits
256Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
128Kx36	0000	00101 00100	XXXXXX	00001001110	1
256Kx18	0000	00110 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA ₉		SA ₈	5B	35
37	2B	NC		NC	6B	34
38	3A	SA ₁₀		SA ₇	5A	33
39	3C	SA ₁₁		SA ₆	5C	32
40	2C	SA ₁₂		SA ₅	6C	31
41	2A	SA ₁₃		SA ₄	6A	30
42	2D	DQc ₉		DQb ₉	6D	29
43	1D	DQc ₈		DQb ₈	7D	28
44	2E	DQc ₇		DQb ₇	6E	27
45	1E	DQc ₆		DQb ₆	7E	26
46	2F	DQc ₅		DQb ₅	6F	25
47	2G	DQc ₄		DQb ₄	6G	24
48	1G	DQc ₃		DQb ₃	7G	23
49	2H	DQc ₂		DQb ₂	6H	22
50	1H	DQc ₁		DQb ₁	7H	21
51	3G	\overline{SWc}		\overline{SWb}	5G	20
52	4D	NC		\overline{G}	4F	19
53	4E	\overline{SS}		K	4K	18
54	4G	NC		\overline{K}	4L	17
55	4H	NC		\overline{SWa}	5L	16
56	4M	\overline{SW}		DQa ₁	7K	15
57	3L	\overline{SWd}		DQa ₂	6K	14
58	1K	DQd ₁		DQa ₃	7L	13
59	2K	DQd ₂		DQa ₄	6L	12
60	1L	DQd ₃		DQa ₅	6M	11
61	2L	DQd ₄		DQa ₆	7N	10
62	2M	DQd ₅		DQa ₇	6N	9
63	1N	DQd ₆		DQa ₈	7P	8
64	2N	DQd ₇		DQa ₉	6P	7
65	1P	DQd ₈		ZZ	7T	6
66	2P	DQd ₉		SA ₃	5T	5
67	3T	SA ₁₄		SA ₂	6R	4
68	2R	SA ₁₅		SA ₁	4T	3
69	4N	SA ₁₆		SA ₀	4P	2
70	3R	M ₁		M ₂	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA ₉		SA ₈	5B	25
27	2B	NC		NC	6B	24
28	3A	SA ₁₀		SA ₇	5A	23
29	3C	SA ₁₁		SA ₆	5C	22
30	2C	SA ₁₂		SA ₅	6C	21
31	2A	SA ₁₃		SA ₄	6A	20
				DQa ₉	6D	19
32	1D	DQb ₁				
33	2E	DQb ₂				
				DQa ₈	7E	18
				DQa ₇	6F	17
34	2G	DQb ₃				
				DQa ₆	7G	16
				DQa ₅	6H	15
35	1H	DQb ₄				
36	3G	\overline{SWb}				
37	4D	NC		\overline{G}	4F	14
38	4E	\overline{SS}		K	4K	13
39	4G	NC		\overline{K}	4L	12
40	4H	NC		\overline{SWa}	5L	11
41	4M	\overline{SW}		DQa ₄	7K	10
42	2K	DQb ₅		DQa ₃	6L	9
43	1L	DQb ₆				
44	2M	DQb ₇		DQa ₂	6N	8
45	1N	DQb ₈		DQa ₁	7P	7
				ZZ	7T	6
46	2P	DQb ₉		SA ₃	5T	5
47	3T	SA ₁₄		SA ₂	6R	4
48	2R	SA ₁₅				
49	4N	SA ₁₆		SA ₁	4P	3
50	2T	SA ₁₇		SA ₀	6T	2
51	3R	M ₁		M ₂	5R	1

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 16M part and the scanned data are fixed to "0" for this 4M parts.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.15	3.3	3.45	V	
Input High Level	V _{IH}	2.0	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.8	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	2.4	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

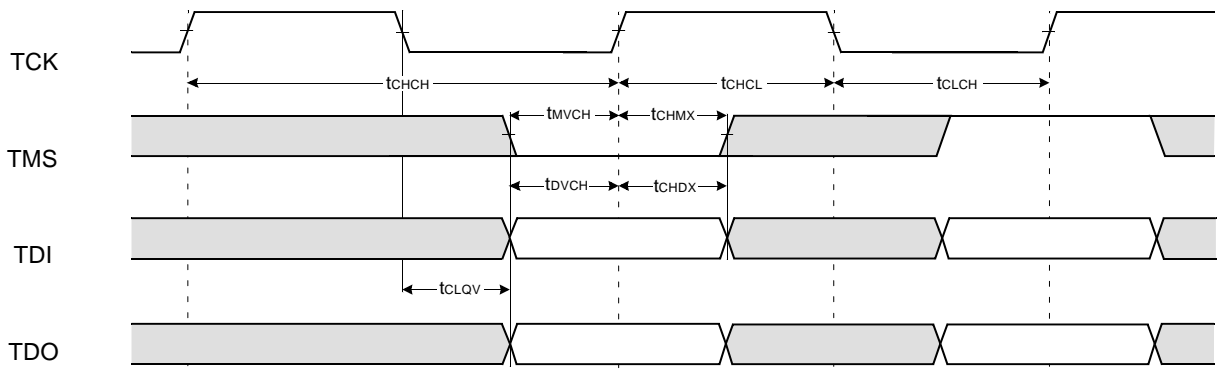
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	3.0/0.0	V	
Input Rise/Fall Time	TR/TF	2.0/2.0	ns	
Input and Output Timing Reference Level		1.5	V	1

NOTE : 1. See SRAM AC test output load on page 5.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

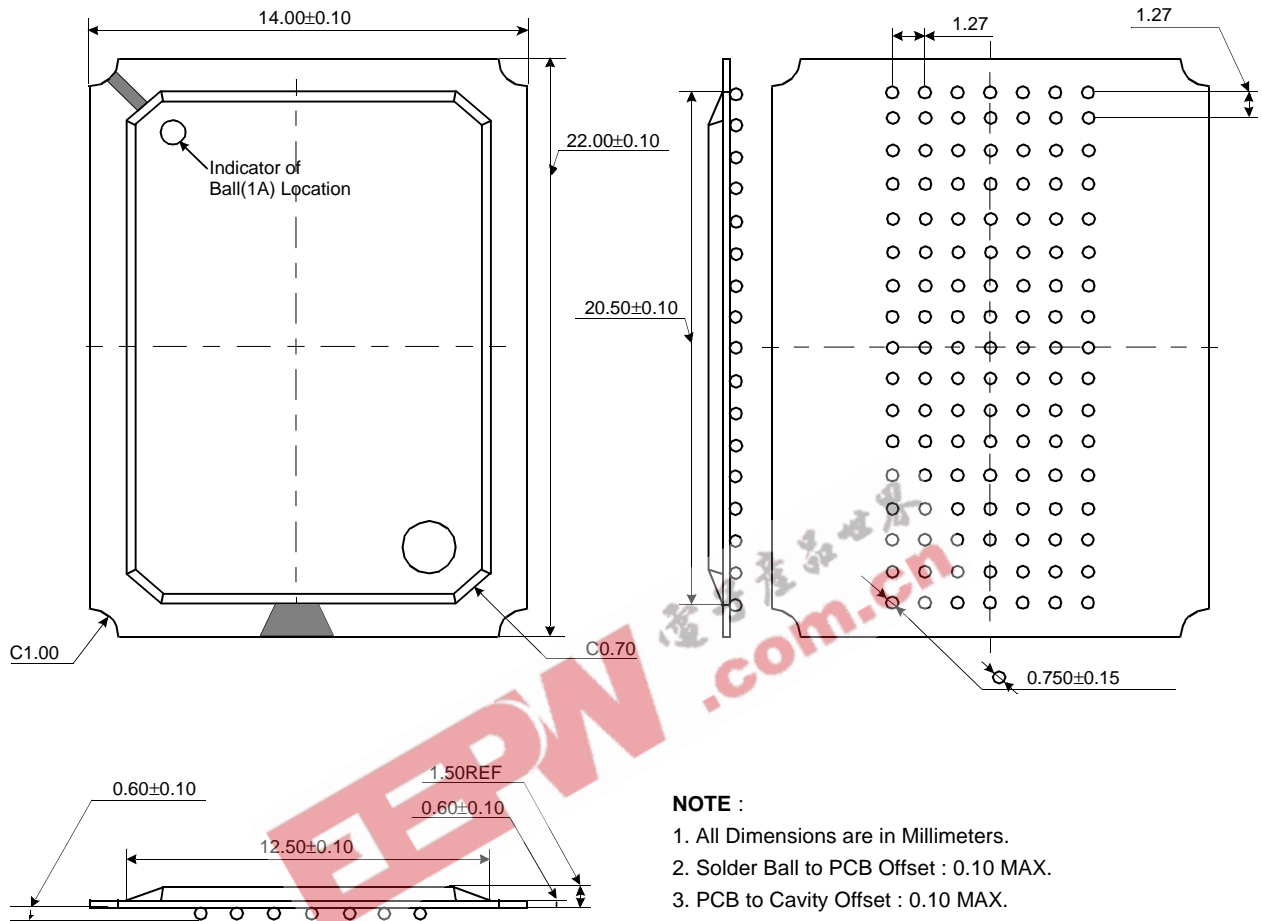
JTAG TIMING DIAGRAM



**K7P403622M
K7P401822M**

128Kx36 & 256Kx18 SRAM

119 BGA PACKAGE DIMENSIONS



119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Junction to Ambient(at air flow of 1m/sec)	Theta_JA	-	-	17	°C/W	
Junction to Case	Theta_JC	-	-	4	°C/W	
Junction to Solder Ball	Theta_JB	-	-	10	°C/W	