8Mx32
Mobile SDRAM
90FBGA

(VDD/VDDQ 3.0V/3.0V or 3.3V/3.3V)

Revision 1.1

December 2002

2M x 32Bit x 4 Banks SDRAM in 90FBGA

FEATURES

- 3.0V & 3.3V power supply
- LVCMOS compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (1, 2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle).
- Extended Temperature Operation (-25°C ~ 85°C).
- Inderstrial Temperature Operation (-40°C ~ 85°C).
- 90Balls DDP FBGA(-MXXX -Pb, -EXXX -Pb Free).

GENERAL DESCRIPTION

The K4M283233D is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 2,097,152 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

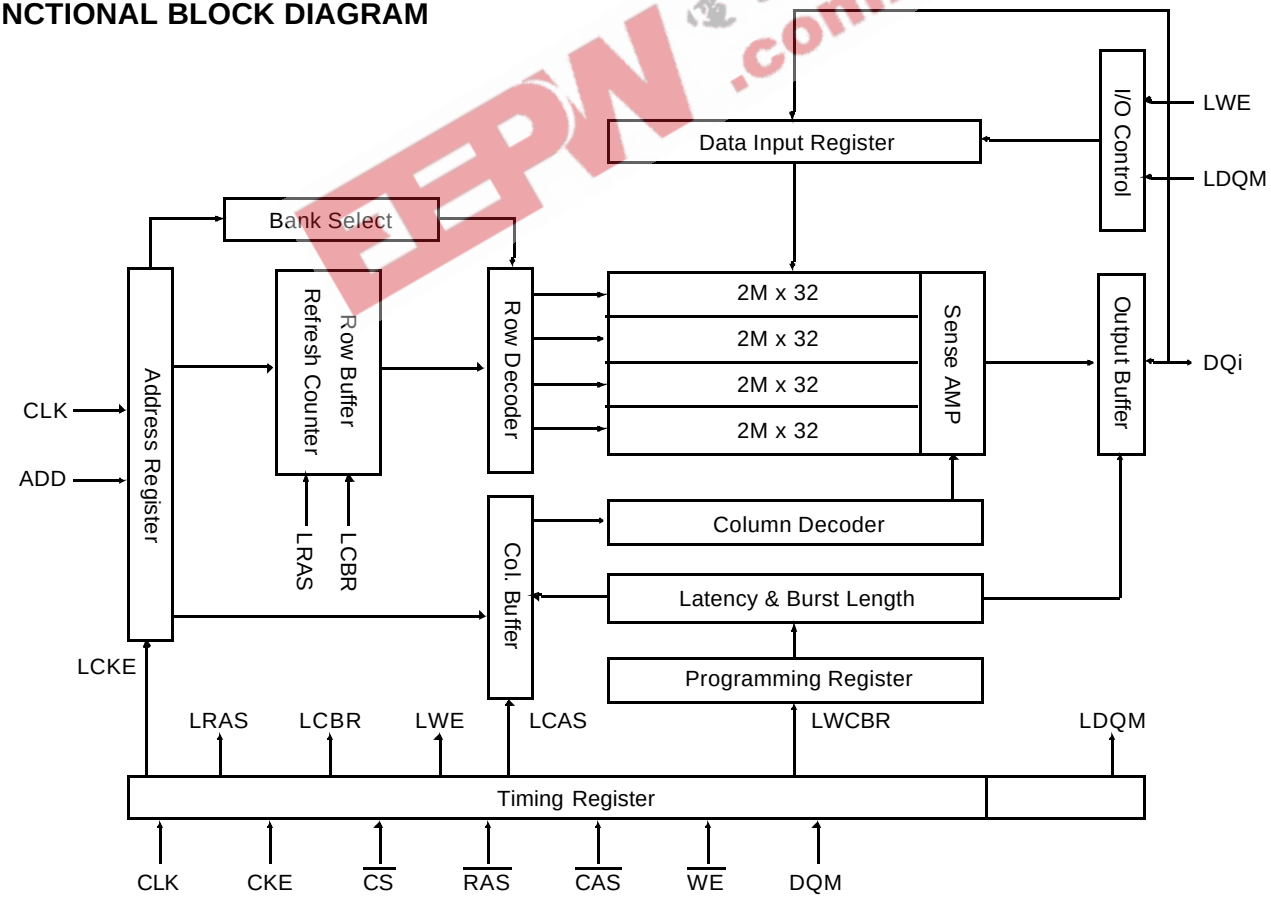
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4M563233D-M(E)E/N/I/P80	125MHz(CL=3) 105MHz(CL=2)	LVCMOS	90 FBGA Pb (Pb Free)
K4M563233D-M(E)E/N/I/P1H	105MHz(CL=2)		
K4M563233D-M(E)E/N/I/P1L	105MHz(CL=3)*1		

- M(E)E/N ; Normal/Low Power, Temp : -25°C ~ 85°C.
- M(E)I/P ; Noraml/Low Power, Temp : -40°C ~ 85°C.

Note : 1. In case of 40MHz Frequency, CL1 can be supported.

FUNCTIONAL BLOCK DIAGRAM



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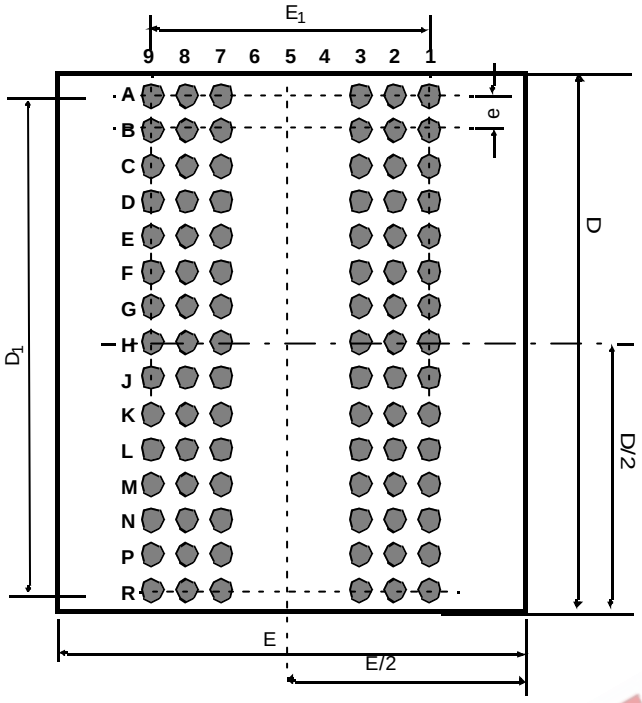
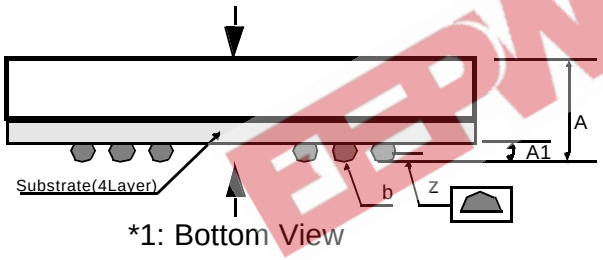
Package Dimension and Pin Configuration

< Bottom View*1 >

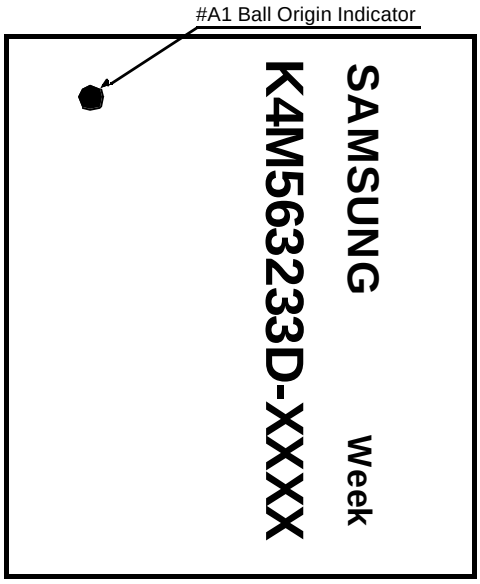


*2: Top View



*1: Bottom View

< Top View*2 >



< Top View*2 >

90Ball(6x15) CSP						
	1	2	3	7	8	9
A	DQ26	DQ24	V_{SS}	V_{DD}	DQ23	DQ21
B	DQ28	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{SSQ}	DQ19
C	V_{SSQ}	DQ27	DQ25	DQ22	DQ20	V_{DDQ}
D	V_{SSQ}	DQ29	DQ30	DQ17	DQ18	V_{DDQ}
E	V_{DDQ}	DQ31	NC	NC	DQ16	V_{SSQ}
F	V_{SS}	DQM3	A3	A2	DQM2	V_{DD}
G	A4	A5	A6	A10	A0	A1
H	A7	A8	NC	NC	BA1	A11
J	CLK	CKE	A9	BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC	$\overline{CAS}$	$\overline{WE}$	DQM0
L	V_{DDQ}	DQ8	V_{SS}	V_{DD}	DQ7	V_{SSQ}
M	V_{SSQ}	DQ10	DQ9	DQ6	DQ5	V_{DDQ}
N	V_{SSQ}	DQ12	DQ14	DQ1	DQ3	V_{DDQ}
P	DQ11	V_{DDQ}	V_{SSQ}	V_{DDQ}	V_{SSQ}	DQ4
R	DQ13	DQ15	V_{SS}	V_{DD}	DQ0	DQ2

Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A_0 ~ A_{11}	*Row Address*
A_0 ~ A_8	*Column Address*
BA_0 ~ BA_1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
DQM_0 ~ DQM_3	*Data Input/Output Mask*
$DQ_{0 \sim 31}$	*Data Input/Output*
V_{DD}/V_{SS}	*Power Supply/Ground*
V_{DDQ}/V_{SSQ}	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	1.35	1.40	1.45
A_1	0.30	0.35	0.40
E	-	11.00	-
E_1	-	6.40	-
D	-	13.00	-
D_1	-	11.20	-
e	-	0.80	-
b	0.40	0.45	0.50
z	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Notes :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C to 85°C for Extended, -40°C to 85°C for Industrial)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	2.7	3.0	3.6	V	
	V_{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V_{IH}	2.2	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.5	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes:
1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include HI-Z output leakage for all bi-directional buffers with tri-state outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 3.0V & 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	3.0	9.0	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE	C_{IN}	3.0	9.0	pF	
DQM	C_{IN}	1.5	4.5	pF	
Address	C_{ADD}	3.0	9.0	pF	
DQ_0 ~ DQ_{31}	C_{OUT}	3.0	6.5	pF	

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C to 85°C for Extended, -40°C to 85°C for Industrial)

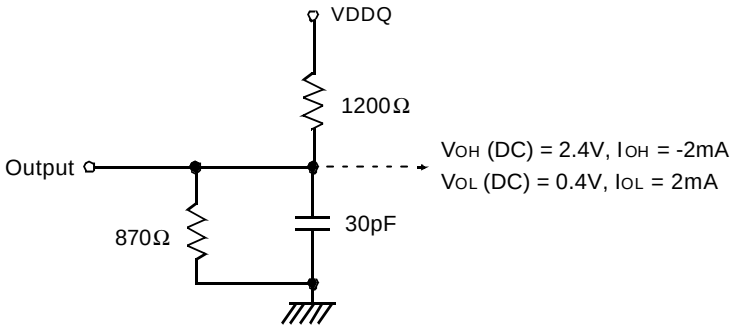
Parameter	Symbol	Test Condition		Version			Unit	Note
				-80	-1H	-1L		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		150	150	140	mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns		1.2			mA	
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		1.2				
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20			mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10				
Active Standby Current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns		8			mA	
	$I_{CC3}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		8				
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		45			mA	
	$I_{CC3}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		40			mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		190	160	160	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		320	300	290	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	-M(E)E/I	3			mA	3
			-M(E)N/P	1000			uA	4

Notes :

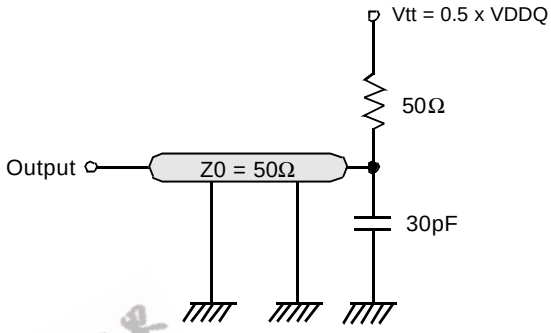
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4M563233D-M(E)E/I**
4. K4M563233D-M(E)N/P**
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 2.7V ~ 3.6V, T_A = -25°C to 85°C for Extended, -40°C to 85°C for Industrial)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-80	-1H	-1L		
Row active to row active delay		t_{RRD}(min)	16	19	19	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	19	19	24	ns	1
Row precharge time		t_{RP}(min)	19	19	24	ns	1
Row active time		t_{RAS}(min)	48	50	60	ns	1
		t_{RAS}(max)	100			us	
Row cycle time		t_{RC}(min)	68	70	84	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2,3
Last data in to Active delay		t_{DAL}(min)	tRDL + tRP			-	3
Last data in to new col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	4
Number of valid output data	CAS latency=3		2			ea	5
	CAS latency=2		1				
	CAS latency=1		-		0		

Notes :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. Minimum tRDL=2CLK and tDAL(=tRDL + tRP) is required to complete both of last data wite command(tRDL) and precharge command(tRP). tRDL=1CLK can be supported only in the case under 100MHz with manual precharge mode.
4. All parts allow every cycle column address change.
5. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 80		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	8	1000	9.5	1000	9.5	1000	ns	1
	CAS latency=2		9.5		9.5		12			
	CAS latency=1		-		-		25			
CLK to valid output delay	CAS latency=3	tSAC		6		7		7	ns	1,2
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		
Output data hold time	CAS latency=3	tOH	2.5		2.5		2.5		ns	2
	CAS latency=2		2.5		2.5		2.5			
	CAS latency=1		-		-		2.5			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	2.0		2.5		2.5		ns	3
Input hold time		tSH	1.0		1.5		1.5		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6		7		7	ns	
	CAS latency=2			7		7		8		
	CAS latency=1			-		-		20		

Notes :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Notes :

1. This is to advise Samsung customers that, in accordance with certain terms of an agreement, Samsung is prohibited from selling any DRAM products configured in "Multi-Die Plastic" format for use as components in general and scientific computers, such as mainframes, servers, work stations or desk top personal computers (hereinafter "Prohibited Computer Use"). Applications such as mobile, including cell phones, telecom, including televisions and display monitors, or non-desktop computer systems, including laptops, notebook computers, are, however, permissible. "Multi-Die Plastic" is defined as two or more DRAM die encapsulated within a single plastic leaded package.

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SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes :

1. OP Code : Operand Code
   $A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation it makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).