

K7P803611B
K7P801811B

256Kx36 & 512Kx18 SRAM

Document Title

256Kx36 & 512Kx18 Synchronous Pipelined SRAM

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
Rev. 0.0	- Initial Document.	Feb. 2001	Preliminary
Rev. 1.0	- Final specification release	May. 2001	Final
Rev. 2.0	- Absolute Maximum Rating VDDQ changed from 2.825V to 2.4V.	Jan. 2002	Final
Rev. 3.0	- Function Description modified	Mar. 2002	Final
Rev. 4.0	- Add -HC27 part (Part Number, Idd, AC Characteristics)	Aug. 2002	Final

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256Kx36 & 512Kx18 SRAM

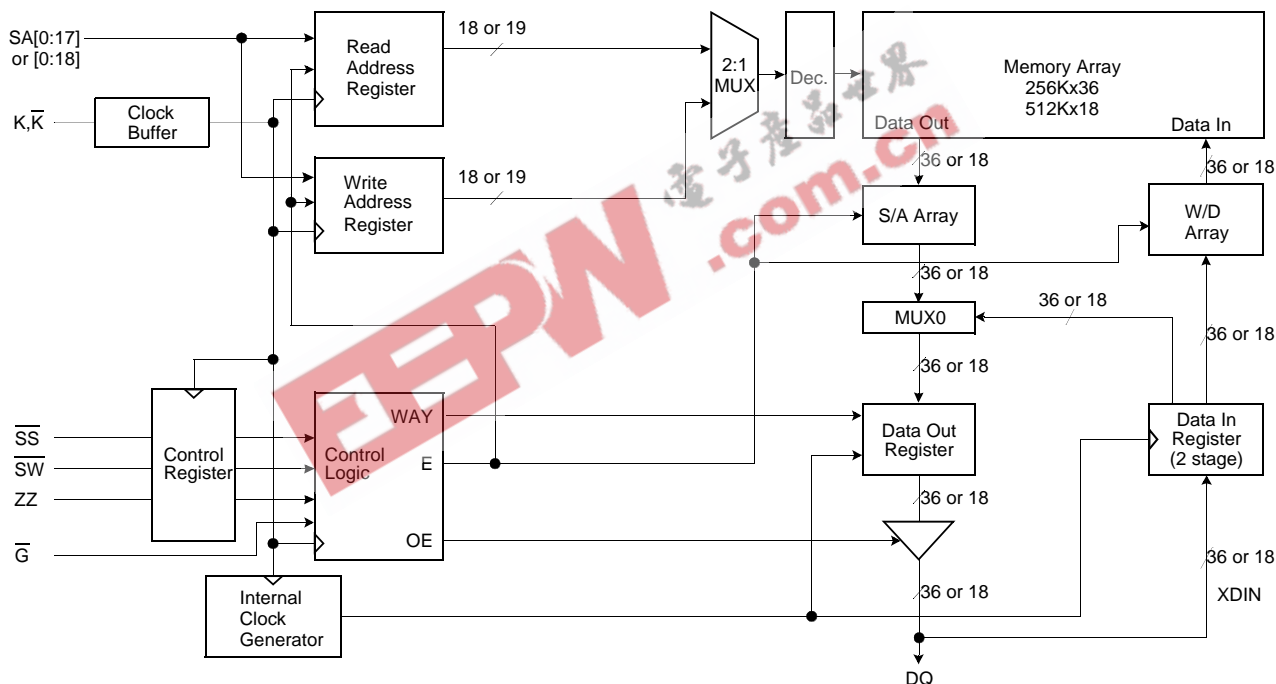
256Kx36 & 512Kx18 Synchronous Pipelined SRAM

FEATURES

- 256Kx36 or 512Kx18 Organizations.
- 3.3V V_{DD}/1.5V V_{DDQ} (2.0V max V_{DDQ}).
- HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K, \bar{K} .
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability (four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1).
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm).

Organization	Part Number	Maximum Frequency	Access Time
256Kx36	K7P803611B-HC33	333MHz	1.5
	K7P803611B-HC30	300MHz	1.6
	K7P803611B-HC27	250MHz	1.85
	K7P803611B-HC25	250MHz	2.0
512Kx18	K7P801811B-HC33	333MHz	1.5
	K7P801811B-HC30	300MHz	1.6
	K7P801811B-HC27	300MHz	1.85
	K7P801811B-HC25	250MHz	2.0

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, \bar{K}	Differential Clocks	ZZ	Asynchronous Power Down
SAn	Synchronous Address Input	ZQ	Output Driver Impedance Control
DQn	Bi-directional Data Bus	TCK	JTAG Test Clock
\bar{SS}	Synchronous Select	TMS	JTAG Test Mode Select
\bar{SW}	Synchronous Global Write Enable	TDI	JTAG Test Data Input
\bar{SWa}	Synchronous Byte a Write Enable	TDO	JTAG Test Data Output
\bar{SWb}	Synchronous Byte b Write Enable	VREF	HSTL Input Reference Voltage
\bar{SWc}	Synchronous Byte c Write Enable	V _{DD}	Power Supply
\bar{SWd}	Synchronous Byte d Write Enable	V _{DDQ}	Output Power Supply
M1, M2	Read Protocol Mode Pins (M1=V _{SS} , M2=V _{DDQ})	V _{SS}	GND
\bar{G}	Asynchronous Output Enable	NC	No Connection

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PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P803611B(256Kx36)

	1	2	3	4	5	6	7
A	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
B	NC	NC	SA9	NC	SA8	SA17	NC
C	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQc8	DQc9	VSS	ZQ	VSS	DQb9	DQb8
E	DQc6	DQc7	VSS	\overline{SS}	VSS	DQb7	DQb6
F	VDDQ	DQc5	VSS	\overline{G}	VSS	DQb5	VDDQ
G	DQc3	DQc4	\overline{SWc}	NC	\overline{SWb}	DQb4	DQb3
H	DQc1	DQc2	VSS	NC	VSS	DQb2	DQb1
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	DQd1	DQd2	VSS	K	VSS	DQa2	DQa1
L	DQd3	DQd4	\overline{SWd}	\overline{K}	\overline{SWa}	DQa4	DQa3
M	VDDQ	DQd5	VSS	\overline{SW}	VSS	DQa5	VDDQ
N	DQd6	DQd7	VSS	SA0	VSS	DQa7	DQa6
P	DQd8	DQd9	VSS	SA1	VSS	DQa9	DQa8
R	NC	SA15	M1	VDD	M2	SA2	NC
T	NC	NC	SA14	SA16	SA3	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

K7P801811B(512Kx18)

	1	2	3	4	5	6	7
A	VDDQ	SA13	SA10	NC	SA7	SA4	VDDQ
B	NC	NC	SA9	NC	SA8	SA17	NC
C	NC	SA12	SA11	VDD	SA6	SA5	NC
D	DQb1	NC	VSS	ZQ	VSS	DQa9	NC
E	NC	DQb2	VSS	\overline{SS}	VSS	NC	DQa8
F	VDDQ	NC	VSS	\overline{G}	VSS	DQa7	VDDQ
G	NC	DQb3	\overline{SWb}	NC	NC	NC	DQa6
H	DQb4	NC	VSS	NC	VSS	DQa5	NC
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	NC	DQb5	VSS	K	VSS	NC	DQa4
L	DQb6	NC	NC	\overline{K}	\overline{SWa}	DQa3	NC
M	VDDQ	DQb7	VSS	\overline{SW}	VSS	NC	VDDQ
N	DQb8	NC	VSS	SA0	VSS	DQa2	NC
P	NC	DQb9	VSS	SA1	VSS	NC	DQa1
R	NC	SA15	M1	VDD	M2	SA2	NC
T	NC	SA18	SA14	NC	SA3	SA16	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

FUNCTION DESCRIPTION

The K7P803611B and K7P801811B are 9,437,184 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 262,144 words by 36 bits for K7P803611B and 524,288 words by 18 bits for K7P801811B, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level K clocks are used to initiate read/write operation and all internal operations are self-timed. At the rising edge of K clock, Addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers at the next rising edge of K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During read operations, addresses and controls are registered during the first rising edge of K clock and then the internal array is read between first and second edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During consecutive read operations where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write Operation(Late Write)

During write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array. Byte write operation is supported using SW[a:d] and the timing of SW[a:d] is the same as the SW signal.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array. Bypass read operation occurs on a byte to byte basis. If only one byte is written during a write operation but a read operation is required on the same address, a partial bypass read operation occurs since the new byte data is from the data in registers while the remaining bytes are from SRAM array.

Sleep Mode

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin high. During sleep mode, all other inputs are ignored and outputs are brought to a High-Impedance state. Sleep mode current and output High-Z are guaranteed after the specified sleep mode enable time. During sleep mode the memory array data content is preserved. Sleep mode must not be initiated until after all pending operations have completed, since any pending operation will not be guaranteed once sleep mode is initiated. Normal operations can be resumed by bringing the ZZ pin low, but only after the specified sleep mode recovery time.

Mode Control

There are two mode control select pins (M1 and M2) used to set the proper read protocol. This SRAM supports single clock pipelined operating mode. For proper specified device operation, M1 must be connected to Vss and M2 must be connected to VDDQ. These mode pins must be set at power-up and must not change during device operation.

Programmable Impedance Output Driver

The data output driver impedance is adjusted by an external resistor, RQ, connected between ZQ pin and Vss, and is equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with G high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time G are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles. The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to Vss or VDDQ.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: Vss, VDD, VDDQ, VREF, then VIN. VDD and VDDQ can be applied simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: VIN, VREF, VDDQ, VDD, Vss. VDD and VDDQ can be removed simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-down.

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TRUTH TABLE

K	ZZ	\bar{G}	\bar{SS}	\bar{SW}	\bar{SWa}	\bar{SWb}	\bar{SWc}	\bar{SWd}	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all bytes

NOTE : K & \bar{K} are complementary

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.9	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 2.4	V
Voltage on any pin Relative to Vss	VIN	-0.5 to VDDQ+0.5 (2.4V MAX)	V
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	3.15	3.3	3.45	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	2.0	V	
Input High Level	V _{IH}	VREF+0.1	-	VDDQ+0.3	V	
Input Low Level	V _{IL}	-0.3	-	VREF-0.1	V	
Input Reference Voltage	VREF	0.68	0.75	1.0	V	
Clock Input Signal Voltage	V _{IN-CLK}	-0.3	-	VDDQ+0.3	V	
Clock Input Differential Voltage	V _{DIF-CLK}	0.1	-	VDDQ+0.3	V	
Clock Input Common Mode Voltage	V _{CM-CLK}	0.68	0.75	1.0	V	

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PIN CAPACITANCE

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	4	pF
Data Output Capacitance	COUT	VOUT=0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(TA=25°C, f=1MHz)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD33		700	mA	1, 2
	IDD30	-	620		
	IDD27		580		
	IDD25		550		
Average Power Supply Operating Current-x18 (VIN=VIH or VIL, ZZ & SS=VIL)	IDD33		650	mA	1, 2
	IDD30	-	570		
	IDD27		530		
	IDD25		500		
Power Supply Standby Current (VIN=VIH or VIL, ZZ=VIH)	ISBZZ	-	70	mA	1
Active Standby Power Supply Current (VIN=VIH or VIL, SS=VIH, ZZ=VIL)	ISBSS	-	200	mA	1
Input Leakage Current (VIN=VSS or VDDQ)	ILI	-1	1	μA	
Output Leakage Current (VOUT=VSS or VDDQ, DQ in High-Z)	ILO	-1	1	μA	
Output High Voltage(Programmable Impedance Mode)	VOH1	VDDQ/2	VDDQ	V	3,5
Output Low Voltage(Programmable Impedance Mode)	VOL1	VSS	VDDQ/2	V	4,5
Output High Voltage(IoH=-0.1mA)	VOH2	VDDQ-0.2	VDDQ	V	6
Output Low Voltage(IoL=0.1mA)	VOL2	VSS	0.2	V	6
Output High Voltage(IoH=-6mA)	VOH3	VDDQ-0.4	VDDQ	V	6
Output Low Voltage(IoL=6mA)	VOL3	VSS	0.4	V	6

NOTE : 1. Minimum cycle. IOUT=0mA.

2. 50% read cycles.

3. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5) \pm 15\%$ @ $V_{OH} = V_{DDQ}/2$ for $175\Omega \leq RQ \leq 350\Omega$.

4. $|I_{OL}| = (V_{DDQ}/2)/(RQ/5) \pm 15\%$ @ $V_{OL} = V_{DDQ}/2$ for $175\Omega \leq RQ \leq 350\Omega$.

5. Programmable Impedance Output Buffer Mode. The ZQ pin is connected to VSS through RQ.

6. Minimum Impedance Output Buffer Mode. The ZQ pin is connected to VSS or VDDQ.

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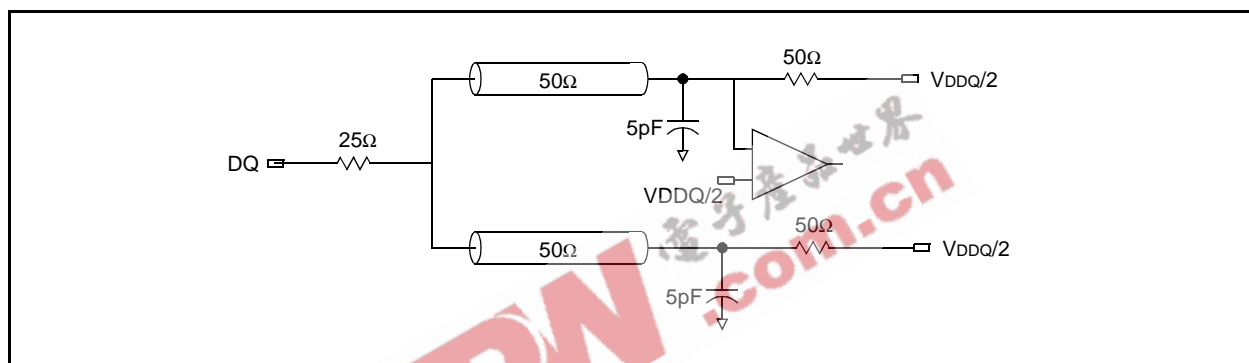
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AC TEST CONDITIONS (TA=0 to 70°C, VDD=3.15~3.45V, VDDQ=1.5V)

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	VDD	3.15~3.45	V
Output Power Supply Voltage	VDDQ	1.5	V
Input High/Low Level	VIH/VIL	1.25/0.25	V
Input Reference Level	VREF	0.75	V
Input Rise/Fall Time	TR/TF	0.5/0.5	ns
Input and Out Timing Reference Level		0.75	V
Clock Input Timing Reference Level		Cross Point	V

NOTE : Parameters are tested with RQ=250Ω and VDDQ=1.5V.

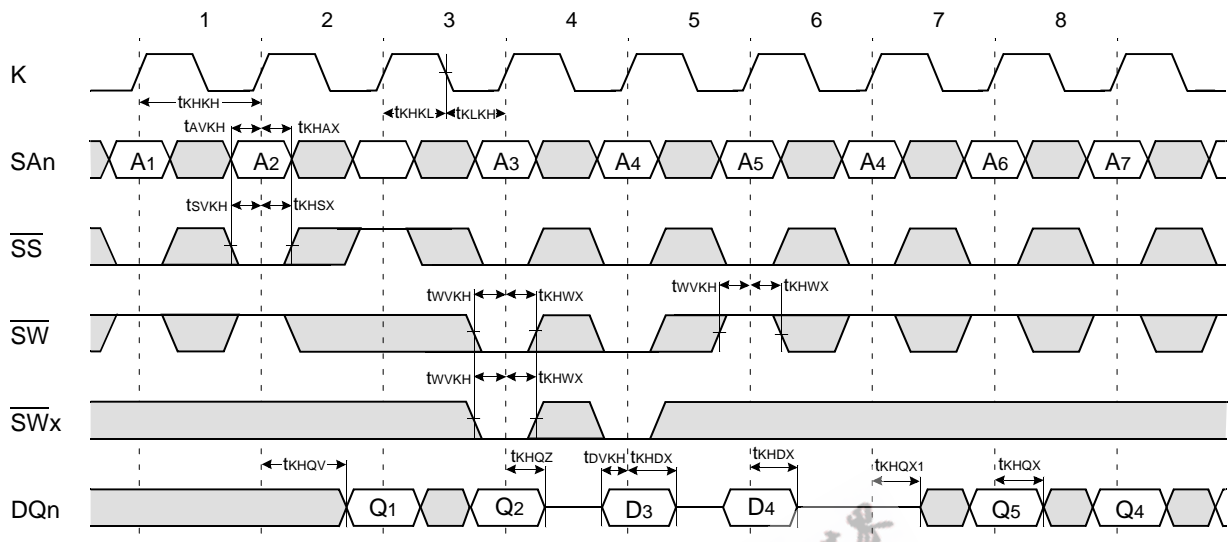
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol	-33		-30		-27		-25		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	tkHKH	3.0	-	3.3	-	3.65	-	4.0	-	ns	
Clock High Pulse Width	tkHKL	1.2	-	1.3	-	1.5	-	1.6	-	ns	
Clock Low Pulse Width	tkLKH	1.2	-	1.3	-	1.5	-	1.6	-	ns	
Clock High to Output Valid	tkHQV	-	1.5	-	1.6	-	1.85	-	2.0	ns	
Clock High to Output Hold	tkHQX	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	tAVKH	0.4	-	0.4	-	0.4	-	0.4	-	ns	
Address Hold Time	tkHAX	0.5	-	0.6	-	0.7	-	0.7	-	ns	
Write Data Setup Time	tDVKH	0.4	-	0.4	-	0.4	-	0.4	-	ns	
Write Data Hold Time	tkHDX	0.5	-	0.6	-	0.7	-	0.7	-	ns	
SW, SW[a:d] Setup Time	twVKH	0.4	-	0.4	-	0.4	-	0.4	-	ns	
SW, SW[a:d] Hold Time	tkHWX	0.5	-	0.6	-	0.7	-	0.7	-	ns	
SS Setup Time	tsVKH	0.4	-	0.4	-	0.4	-	0.4	-	ns	
SS Hold Time	tkHSX	0.5	-	0.6	-	0.7	-	0.7	-	ns	
Clock High to Output Hi-Z	tkHQZ	-	1.5	-	1.6	-	1.85	-	2.0	ns	
Clock High to Output Low-Z	tkHQX1	0.5	-	0.5	-	0.5	-	0.5	-	ns	
\bar{G} High to Output High-Z	tGHQZ	-	1.5	-	1.6	-	1.85	-	2.0	ns	
\bar{G} Low to Output Low-Z	tGLQX	0.5	-	0.5	-	0.5	-	0.5	-	ns	
\bar{G} Low to Output Valid	tGLQV	-	1.5	-	1.6	-	1.85	-	2.0	ns	
ZZ High to Power Down(Sleep Time)	tzZE	-	15	-	15	-	15	-	15	ns	
ZZ Low to Recovery(Wake-up Time)	tzZR	-	20	-	20	-	20	-	20	ns	

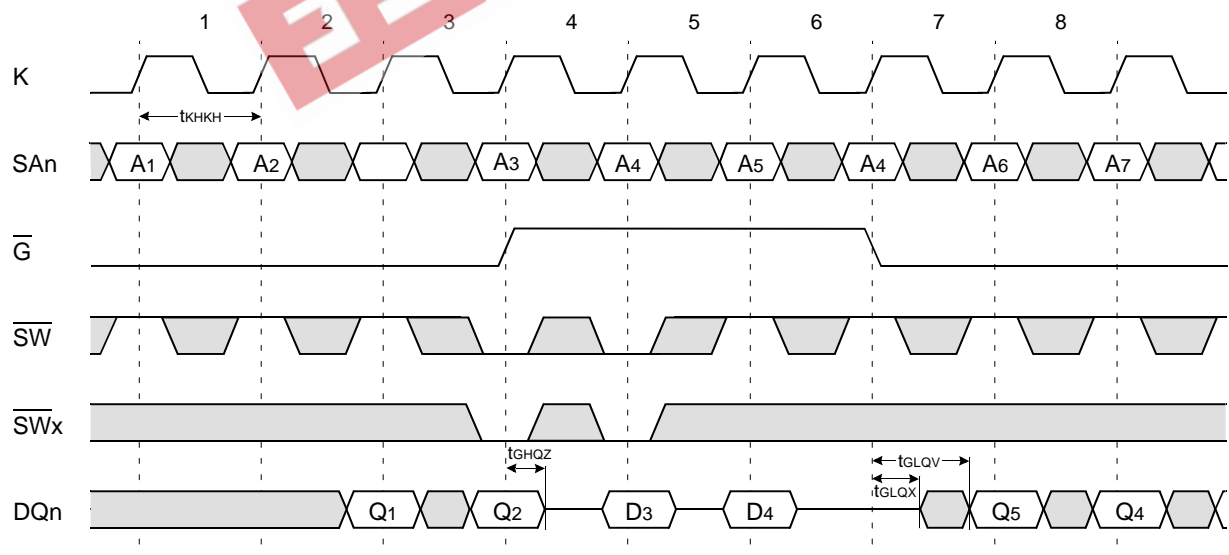
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{SS} Controlled, \overline{G} =Low)



NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

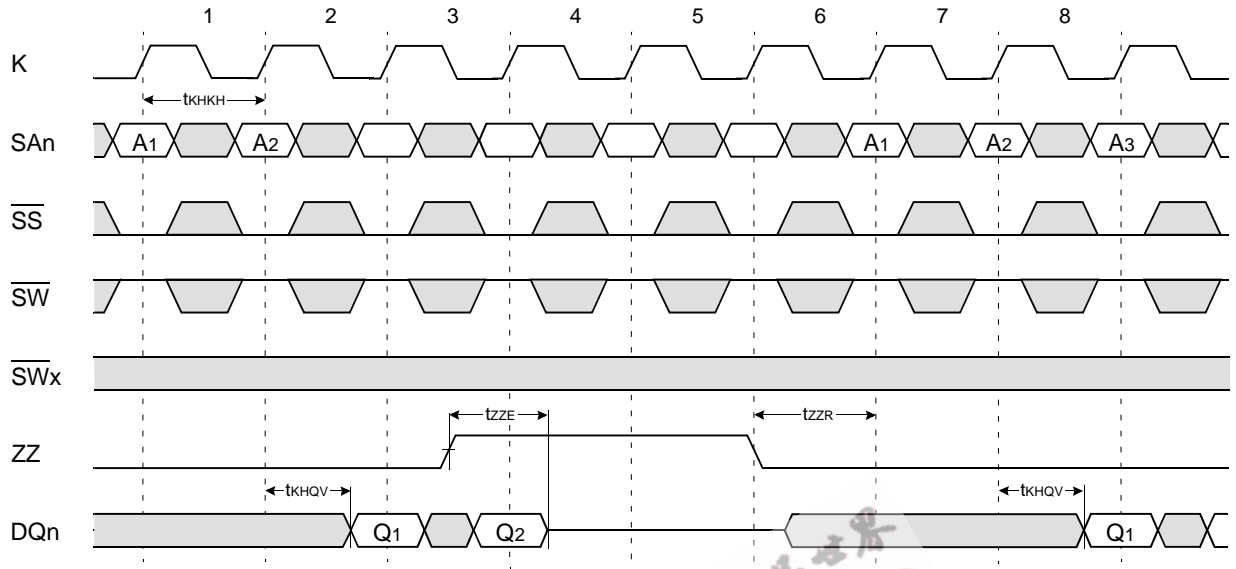
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{G} Controlled, \overline{SS} =Low)



NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

TIMING WAVEFORMS OF STANDBY CYCLES

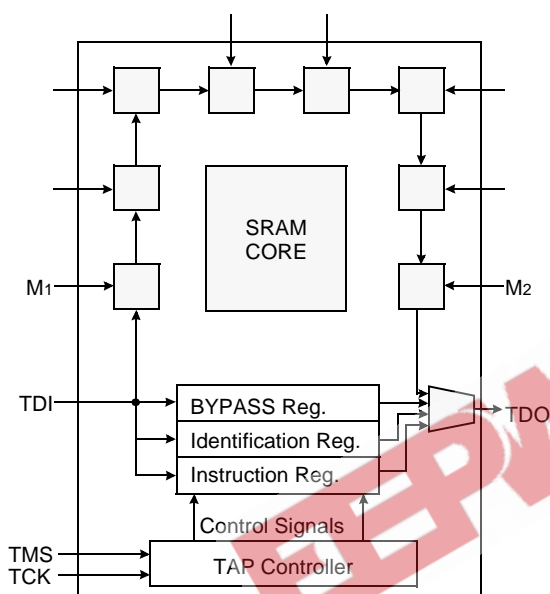


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IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



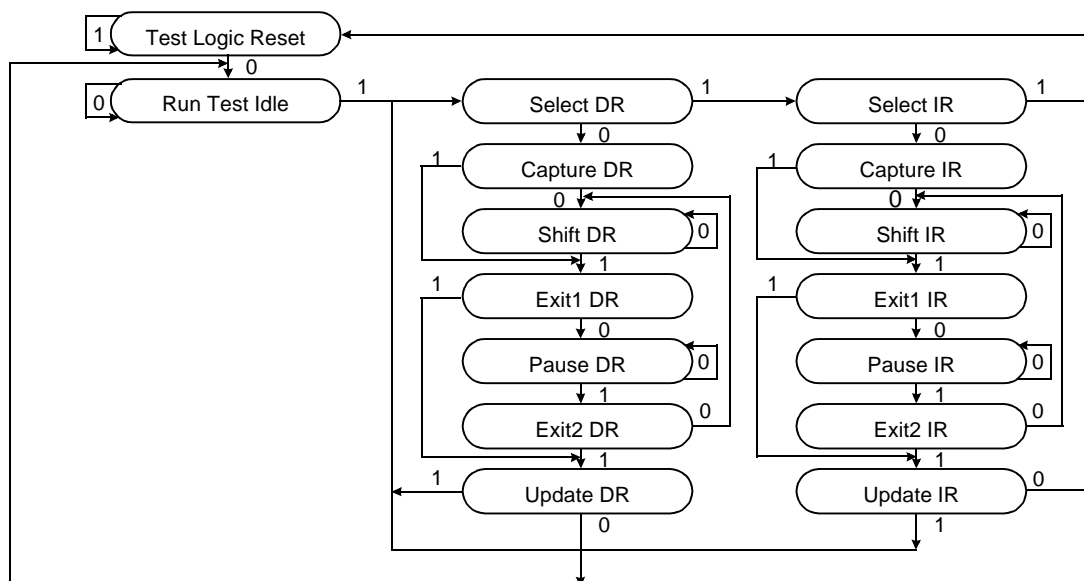
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not places DQs in Hi-Z.

TAP Controller State Diagram



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SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	70 bits
512Kx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA ₉		SA ₈	5B	35
37	2B	NC		SA ₁₇	6B	34
38	3A	SA ₁₀		SA ₇	5A	33
39	3C	SA ₁₁		SA ₆	5C	32
40	2C	SA ₁₂		SA ₅	6C	31
41	2A	SA ₁₃		SA ₄	6A	30
42	2D	DQc ₉		DQb ₉	6D	29
43	1D	DQc ₈		DQb ₈	7D	28
44	2E	DQc ₇		DQb ₇	6E	27
45	1E	DQc ₆		DQb ₆	7E	26
46	2F	DQc ₅		DQb ₅	6F	25
47	2G	DQc ₄		DQb ₄	6G	24
48	1G	DQc ₃		DQb ₃	7G	23
49	2H	DQc ₂		DQb ₂	6H	22
50	1H	DQc ₁		DQb ₁	7H	21
51	3G	SWc		SWb	5G	20
52	4D	ZQ		G	4F	19
53	4E	SS		K	4K	18
54	4G	NC		K	4L	17
55	4H	NC		SWa	5L	16
56	4M	SW		DQa ₁	7K	15
57	3L	SWd		DQa ₂	6K	14
58	1K	DQd ₁		DQa ₃	7L	13
59	2K	DQd ₂		DQa ₄	6L	12
60	1L	DQd ₃		DQa ₅	6M	11
61	2L	DQd ₄		DQa ₆	7N	10
62	2M	DQd ₅		DQa ₇	6N	9
63	1N	DQd ₆		DQa ₈	7P	8
64	2N	DQd ₇		DQa ₉	6P	7
65	1P	DQd ₈		ZZ	7T	6
66	2P	DQd ₉		SA ₃	5T	5
67	3T	SA ₁₄		SA ₂	6R	4
68	2R	SA ₁₅		SA ₁₆	4T	3
69	4N	SA ₀		SA ₁	4P	2
70	3R	M ₁		M ₂	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA ₉		SA ₈	5B	25
27	2B	NC		SA ₁₇	6B	24
28	3A	SA ₁₀		SA ₇	5A	23
29	3C	SA ₁₁		SA ₆	5C	22
30	2C	SA ₁₂		SA ₅	6C	21
31	2A	SA ₁₃		SA ₄	6A	20
				DQa ₉	6D	19
32	1D	DQb ₁				
33	2E	DQb ₂				
				DQa ₈	7E	18
				DQa ₇	6F	17
34	2G	DQb ₃				
				DQa ₆	7G	16
				DQa ₅	6H	15
35	1H	DQb ₄				
36	3G	SWb				
37	4D	ZQ		G	4F	14
38	4E	SS		K	4K	13
39	4G	NC		K	4L	12
40	4H	NC		SWa	5L	11
41	4M	SW		DQa ₄	7K	10
42	2K	DQb ₅		DQa ₃	6L	9
43	1L	DQb ₆				
44	2M	DQb ₇		DQa ₂	6N	8
45	1N	DQb ₈		DQa ₁	7P	7
				ZZ	7T	6
46	2P	DQb ₉		SA ₃	5T	5
47	3T	SA ₁₄		SA ₂	6R	4
48	2R	SA ₁₅				
49	4N	SA ₀		SA ₁	4P	3
50	2T	SA ₁₈		SA ₁₆	6T	2
51	3R	M ₁		M ₂	5R	1

NOTE : 1. Pin 2B is a no connection pin to internal chip. This pin is a place holder for 16M part and the scanned data is fixed to "0" for this 8M part.
2. Pins 4G and 4H are no connection pin to internal chip. The scanned data are fixed to "0" and "1" respectively.

K7P803611B K7P801811B

256Kx36 & 512Kx18 SRAM

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.15	3.3	3.45	V	
Input High Level	V _{IH}	1.7	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.8	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	2.1	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

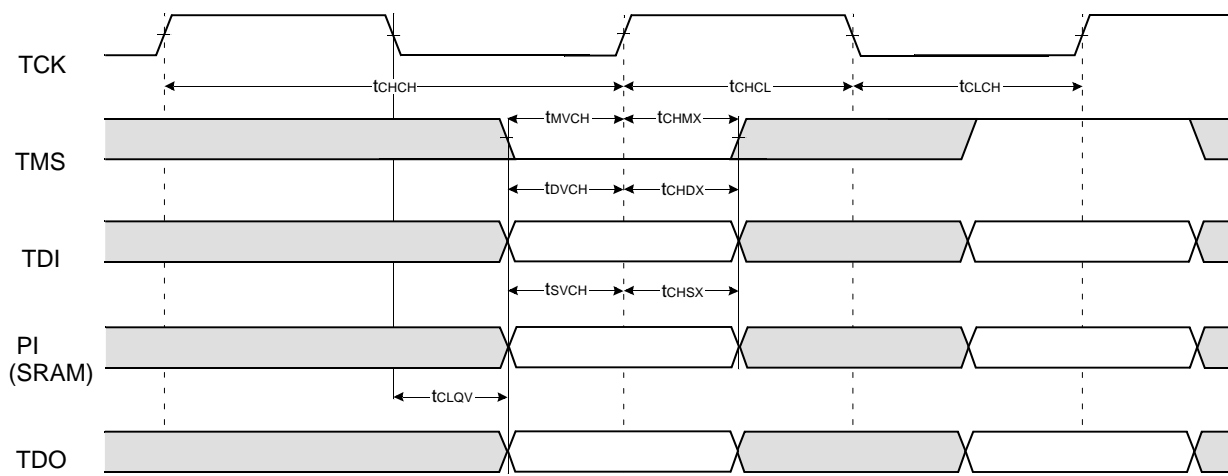
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

NOTE : 1. See SRAM AC test output load on page 7.

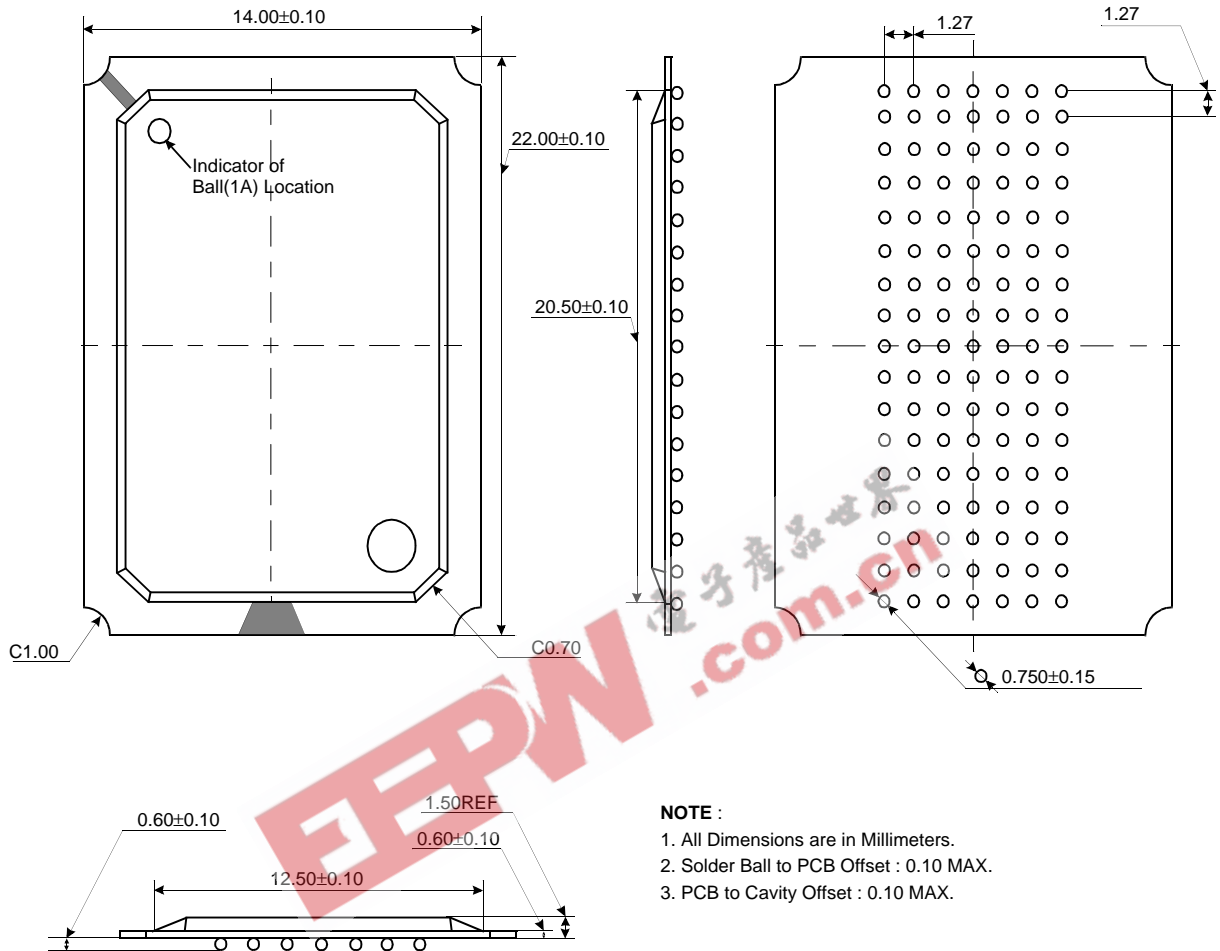
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	30.2	°C/W	1W Heating
Junction to Case	Theta_JC	5.9	°C/W	
Junction to Solder Ball	Theta_JB	4.8	°C/W	2W Heating

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \text{Theta}_{JA}$.