Document Title

16M Bit (2M x8/1M x16) Dual Bank NOR Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	July 25, 2004	Advance
0.1	Support 48TSOP1 Lead Free Package	Sep 16, 2004	Preliminary
0.2	Support 48FBGA Leaded/Lead Free Package	Nov 29, 2004	Preliminary
1.0	Specification finalized	Dec 16, 2004	

16M Bit (2M x8/1M x16) Dual Bank NOR Flash Memory

FEATURES

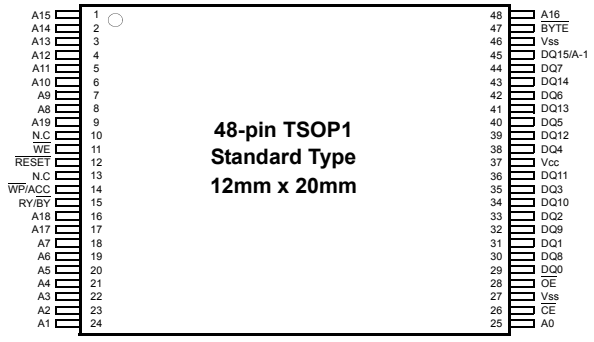
- Single Voltage, 2.7V to 3.6V for Read and Write operations
- Organization
  1,048,576 x 16 bit (Word mode)
- Fast Read Access Time : 70ns
- Read While Program/Erase Operation
- Dual Bank architectures
  Bank 1 / Bank 2 : 8Mb / 8Mb
- Secode(Security Code) Block : Extra 64K Byte block
- Power Consumption (typical value @5MHz)
  - Read Current : 14mA
  - Program/Erase Current : 15mA
  - Read While Program or Read While Erase Current : 25mA
  - Standby Mode/Auto Sleep Mode : 5μA
- WP/ACC input pin
  - Allows special protection of two outermost boot blocks at V_{IL}, regardless of block protect status
  - Removes special protection of two outermost boot block at V_{IH}, the two blocks return to normal block protect status
  - Program time at V_{HH} : 9μs/word
- Erase Suspend/Resume
- Unlock Bypass Program
- Hardware RESET Pin
- Command Register Operation
- Block Group Protection / Unprotection
- Supports Common Flash Memory Interface
- Industrial Temperature : -40°C to 85°C
- Endurance : 100,000 Program/Erase Cycles Minimum
- Data Retention : 10 years
- Package : 48 Pin TSOP1 : 12 x 20 mm / 0.5 mm Pin pitch
  48 Ball FBGA : 6 x 8.5 mm / 0.8 mm Ball pitch

GENERAL DESCRIPTION

The K8D1716U featuring single 3.0V power supply, is a 16Mbit NOR-type Flash Memory organized as 2Mx8 or 1M x16. The memory architecture of the device is designed to divide its memory arrays into 39 blocks to be protected by the block group. This block architecture provides highly flexible erase and program capability. The K8D1716U NOR Flash consists of two banks. This device is capable of reading data from one bank while programming or erasing in the other bank. Access times of 70ns, 80ns and 90ns are available for the device. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in units of 8 bits (Byte) or 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.7 sec. The device requires 15mA as program/erase current in the standard and industrial temperature ranges.

The K8D1716U NOR Flash Memory is created by using Samsung's advanced CMOS process technology. This device is available in 48 pin TSOP1 and 48 ball FBGA package. The device is compatible with EPROM applications to require high-density and cost-effective nonvolatile read/write storage solutions.

PIN CONFIGURATION

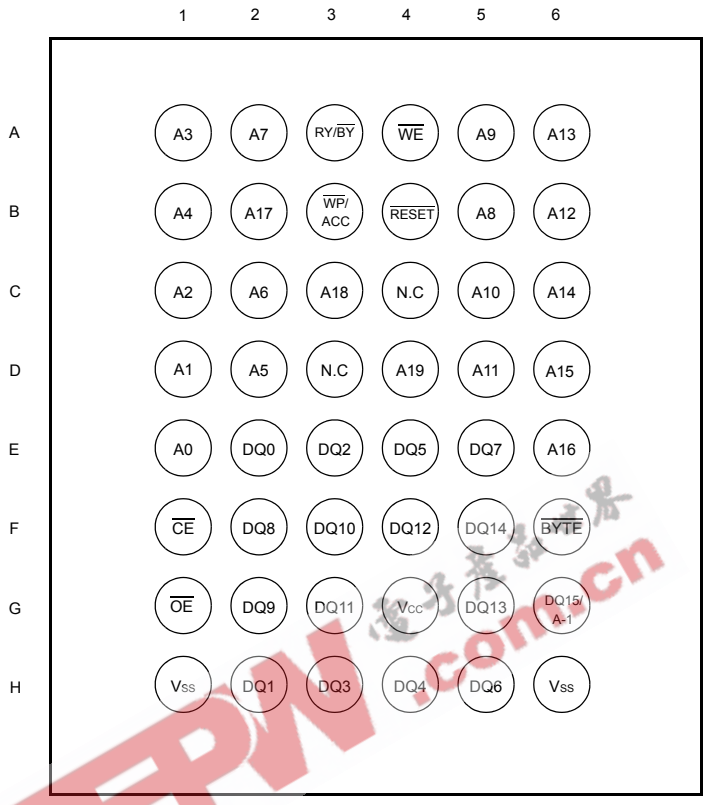


Note :
Please refer to the package dimension.

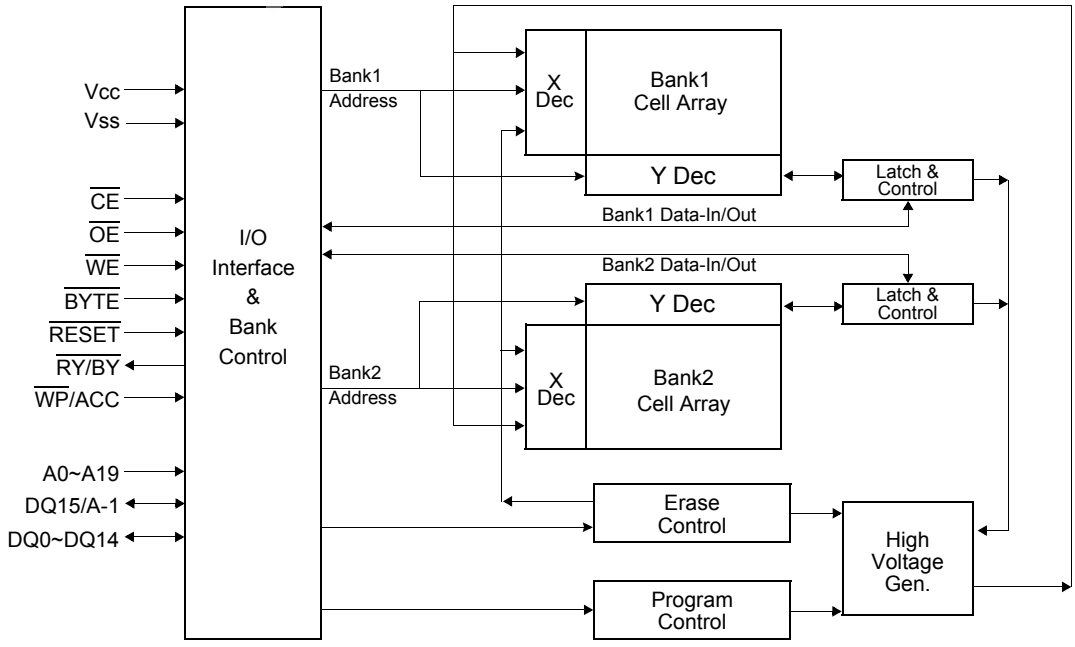
PIN DESCRIPTION

Pin Name	Pin Function
A0 - A19	Address Inputs
DQ0 - DQ14	Data Inputs / Outputs
DQ15/A-1	DQ15 Data Input / Output A-1 LSB Address
$\overline{BYTE}$	Word / Byte Selection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
RY/$\overline{BY}$	Ready/Busy Output
$\overline{WE}$	Write Enable
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
Vcc	Power Supply
Vss	Ground
N.C	No Connection

48 Ball FBGA TOP VIEW (BALL DOWN)



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

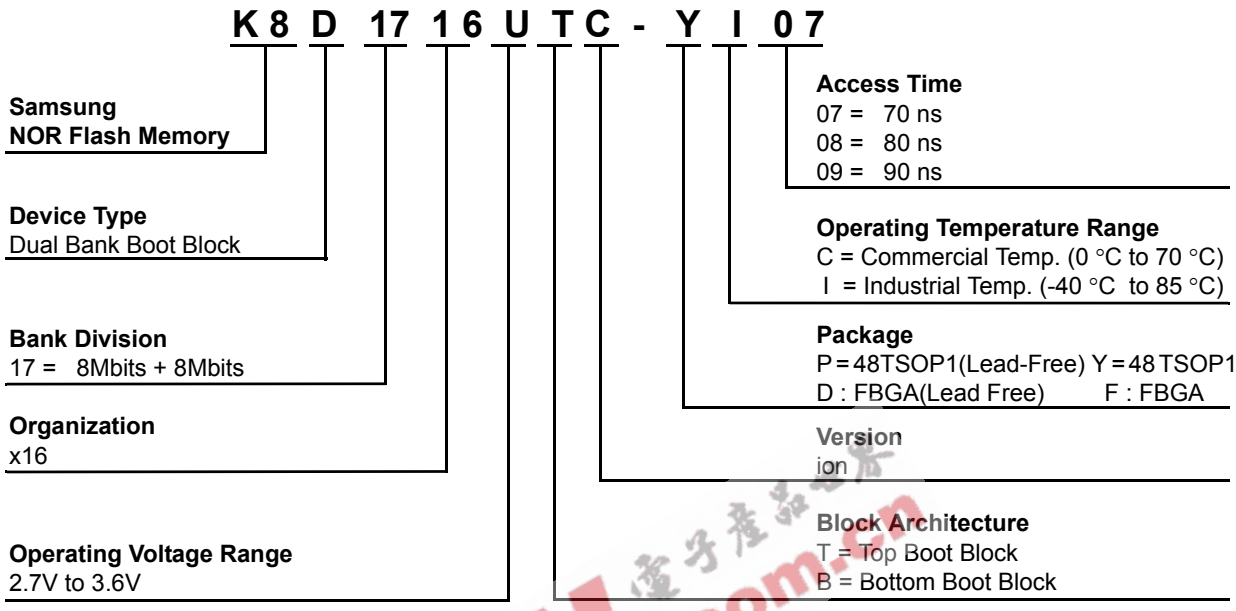


Table 1. PRODUCT LINE-UP

Part No.	- 7	-8	-9
Vcc	2.7V~3.6V		
Max. Address Access Time (ns)	70ns	80ns	90ns
Max. $\overline{CE}$ Access Time (ns)	70ns	80ns	90ns
Max. $\overline{OE}$ Access Time (ns)	25ns	25ns	35ns

Table 2. K8D1716U DEVICE BANK DIVISIONS

Device Part Number	Bank 1		Bank 2	
	Mbit	Block Sizes	Mbit	Block Sizes
K8D1716U	8 Mbit	Eight 8 Kbyte/4 Kword, fifteen 64 Kbyte/32 Kword	8 Mbit	Sixteen 64 Kbyte/32 Kword

Table 3. Top Boot Block Address (K8D1716UT)

K8D1716UT	Block	A19	A18	A17	A16	A15	A14	A13	A12	Block Size (KW/KB)	Address Range	
											Word Mode	Byte Mode
Bank1	BA38	1	1	1	1	1	1	1	1	4 / 8	FF000H-FFFFFH	1FE000H-1FFFFFH
	BA37	1	1	1	1	1	1	1	0	4 / 8	FE000H-FEFFFH	1FC000H-1FDFFFH
	BA36	1	1	1	1	1	1	0	1	4 / 8	FD000H-FDFFFH	1FA000H-1FBFFFH
	BA35	1	1	1	1	1	1	0	0	4 / 8	FC000H-FCFFFH	1F8000H-1F9FFFH
	BA34	1	1	1	1	1	0	1	1	4 / 8	FB000H-FBFFFH	1F6000H-1F7FFFH
	BA33	1	1	1	1	1	0	1	0	4 / 8	FA000H-FAFFFH	1F4000H-1F5FFFH
	BA32	1	1	1	1	1	0	0	1	4 / 8	F9000H-F9FFFH	1F2000H-1F3FFFH
	BA31	1	1	1	1	1	0	0	0	4 / 8	F8000H-F8FFFH	1F0000H-1F1FFFH
	BA30	1	1	1	1	0	X	X	X	32 / 64	F0000H-F7FFFH	1E0000H-1EFFFFH
	BA29	1	1	1	0	1	X	X	X	32 / 64	E8000H-EFFFFH	1D0000H-1DFFFFH
	BA28	1	1	1	0	0	X	X	X	32 / 64	E0000H-E7FFFH	1C0000H-1CFFFFH
	BA27	1	1	0	1	1	X	X	X	32 / 64	D8000H-DFFFFH	1B0000H-1BFFFFH
	BA26	1	1	0	1	0	X	X	X	32 / 64	D0000H-D7FFFH	1A0000H-1AFFFFH
	BA25	1	1	0	0	1	X	X	X	32 / 64	C8000H-CFFFFH	190000H-19FFFFH
	BA24	1	1	0	0	0	X	X	X	32 / 64	C0000H-C7FFFH	180000H-18FFFFH
	BA23	1	0	1	1	1	X	X	X	32 / 64	B8000H-BFFFFH	170000H-17FFFFH
	BA22	1	0	1	1	0	X	X	X	32 / 64	B0000H-B7FFFH	160000H-16FFFFH
	BA21	1	0	1	0	1	X	X	X	32 / 64	A8000H-AFFFFH	150000H-15FFFFH
	BA20	1	0	1	0	0	X	X	X	32 / 64	A0000H-A7FFFH	140000H-14FFFFH
	BA19	1	0	0	1	1	X	X	X	32 / 64	98000H-9FFFFH	130000H-13FFFFH
	BA18	1	0	0	1	0	X	X	X	32 / 64	90000H-97FFFH	120000H-12FFFFH
	BA17	1	0	0	0	1	X	X	X	32 / 64	88000H-8FFFFH	110000H-11FFFFH
	BA16	1	0	0	0	0	X	X	X	32 / 64	80000H-87FFFH	100000H-10FFFFH
Bank2	BA15	0	1	1	1	1	X	X	X	32 / 64	78000H-7FFFFH	0F0000H-0FFFFFH
	BA14	0	1	1	1	0	X	X	X	32 / 64	70000H-77FFFH	0E0000H-0EFFFFH
	BA13	0	1	1	0	1	X	X	X	32 / 64	68000H-6FFFFH	0D0000H-0DFFFFH
	BA12	0	1	1	0	0	X	X	X	32 / 64	60000H-67FFFH	0C0000H-0CFFFFH
	BA11	0	1	0	1	1	X	X	X	32 / 64	58000H-5FFFFH	0B0000H-0BFFFFH
	BA10	0	1	0	1	0	X	X	X	32 / 64	50000H-57FFFH	0A0000H-0AFFFFH
	BA9	0	1	0	0	1	X	X	X	32 / 64	48000H-4FFFFH	090000H-09FFFFH
	BA8	0	1	0	0	0	X	X	X	32 / 64	40000H-47FFFH	080000H-08FFFFH
	BA7	0	0	1	1	1	X	X	X	32 / 64	38000H-3FFFFH	070000H-07FFFFH
	BA6	0	0	1	1	0	X	X	X	32 / 64	30000H-37FFFH	060000H-06FFFFH
	BA5	0	0	1	0	1	X	X	X	32 / 64	28000H-2FFFFH	050000H-05FFFFH
	BA4	0	0	1	0	0	X	X	X	32 / 64	20000H-27FFFH	040000H-04FFFFH
	BA3	0	0	0	1	1	X	X	X	32 / 64	18000H-1FFFFH	030000H-03FFFFH
	BA2	0	0	0	1	0	X	X	X	32 / 64	10000H-17FFFH	020000H-02FFFFH
	BA1	0	0	0	0	1	X	X	X	32 / 64	08000H-0FFFFH	010000H-01FFFFH
	BA0	0	0	0	0	0	X	X	X	32 / 64	00000H-07FFFH	000000H-00FFFFH

Table 4. Secode Block Addresses for Top Boot Devices

Device	Block Address A19-A12	Block Size	(X8) Address Range	(X16) Address Range
K8D1716UT	11111xxx	64/32	1F0000H-1FFFFFH	F8000H-FFFFFH

Table 5. Bottom Boot Block Address (K8D1716UB)

K8D1716UT	Block	A19	A18	A17	A16	A15	A14	A13	A12	Block Size (KW/KB)	Address Range	
											Word Mode	Byte Mode
Bank2	BA38	1	1	1	1	1	X	X	X	32 / 64	F8000H-FFFFFH	1F0000H-1FFFFFH
	BA37	1	1	1	1	0	X	X	X	32 / 64	F0000H-F7FFFH	1E0000H-1EFFFFH
	BA36	1	1	1	0	1	X	X	X	32 / 64	E8000H-EFFFFH	1D0000H-1DFFFFH
	BA35	1	1	1	0	0	X	X	X	32 / 64	E0000H-E7FFFH	1C0000H-1CFFFFH
	BA34	1	1	0	1	1	X	X	X	32 / 64	D8000H-DFFFFH	1B0000H-1BFFFFH
	BA33	1	1	0	1	0	X	X	X	32 / 64	D0000H-D7FFFH	1A0000H-1AFFFFH
	BA32	1	1	0	0	1	X	X	X	32 / 64	C8000H-CFFFFH	190000H-19FFFFH
	BA31	1	1	0	0	0	X	X	X	32 / 64	C0000H-C7FFFH	180000H-18FFFFH
	BA30	1	0	1	1	1	X	X	X	32 / 64	B8000H-BFFFFH	170000H-17FFFFH
	BA29	1	0	1	1	0	X	X	X	32 / 64	B0000H-B7FFFH	160000H-16FFFFH
	BA28	1	0	1	0	1	X	X	X	32 / 64	A8000H-AFFFFH	150000H-15FFFFH
	BA27	1	0	1	0	0	X	X	X	32 / 64	A0000H-A7FFFH	140000H-14FFFFH
	BA26	1	0	0	1	1	X	X	X	32 / 64	98000H-9FFFFH	130000H-13FFFFH
	BA25	1	0	0	1	0	X	X	X	32 / 64	90000H-97FFFH	120000H-12FFFFH
	BA24	1	0	0	0	1	X	X	X	32 / 64	88000H-8FFFFH	110000H-11FFFFH
	BA23	1	0	0	0	0	X	X	X	32 / 64	80000H-87FFFH	100000H-10FFFFH
Bank1	BA22	0	1	1	1	1	X	X	X	32 / 64	78000H-7FFFFH	0F0000H-0FFFFFH
	BA21	0	1	1	1	0	X	X	X	32 / 64	70000H-77FFFH	0E0000H-0EFFFFH
	BA20	0	1	1	0	1	X	X	X	32 / 64	68000H-6FFFFH	0D0000H-0DFFFFH
	BA19	0	1	1	0	0	X	X	X	32 / 64	60000H-67FFFH	0C0000H-0CFFFFH
	BA18	0	1	0	1	1	X	X	X	32 / 64	58000H-5FFFFH	0B0000H-0BFFFFH
	BA17	0	1	0	1	0	X	X	X	32 / 64	50000H-57FFFH	0A0000H-0AFFFFH
	BA16	0	1	0	0	1	X	X	X	32 / 64	48000H-4FFFFH	090000H-09FFFFH
	BA15	0	1	0	0	0	X	X	X	32 / 64	40000H-47FFFH	080000H-08FFFFH
	BA14	0	0	1	1	1	X	X	X	32 / 64	38000H-3FFFFH	070000H-07FFFFH
	BA13	0	0	1	1	0	X	X	X	32 / 64	30000H-37FFFH	060000H-06FFFFH
	BA12	0	0	1	0	1	X	X	X	32 / 64	28000H-2FFFFH	050000H-05FFFFH
	BA11	0	0	1	0	0	X	X	X	32 / 64	20000H-27FFFH	040000H-04FFFFH
	BA10	0	0	0	1	1	X	X	X	32 / 64	18000H-1FFFFH	030000H-03FFFFH
	BA9	0	0	0	1	0	X	X	X	32 / 64	10000H-17FFFH	020000H-02FFFFH
	BA8	0	0	0	0	1	X	X	X	32 / 64	08000H-0FFFFH	010000H-01FFFFH
	BA7	0	0	0	0	0	1	1	1	4 / 8	07000H-07FFFH	00E000H-00FFFFH
	BA6	0	0	0	0	0	1	1	0	4 / 8	06000H-06FFFH	00C000H-00DFFFH
	BA5	0	0	0	0	0	1	0	1	4 / 8	05000H-05FFFH	00A000H-00BFFFH
	BA4	0	0	0	0	0	1	0	0	4 / 8	04000H-04FFFH	008000H-009FFFH
	BA3	0	0	0	0	0	0	1	1	4 / 8	03000H-03FFFH	006000H-007FFFH
	BA2	0	0	0	0	0	0	1	0	4 / 8	02000H-02FFFH	004000H-005FFFH
	BA1	0	0	0	0	0	0	0	1	4 / 8	01000H-01FFFH	002000H-003FFFH
	BA0	0	0	0	0	0	0	0	0	4 / 8	00000H-00FFFH	000000H-001FFFH

Table 6. Secode Block Addresses for Bottom Boot Devices

Device	Block Address A19-A12	Block Size	(X8) Address Range	(X16) Address Range
K8D1716UB	00000xxx	64/32	000000H-00FFFFH	00000H-07FFFH

PRODUCT INTRODUCTION

The K8D1716U is a 16Mbit (16,777,216 bits) NOR-type Flash memory. The device features single voltage power supply operating within the range of 2.7V to 3.6V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 39 blocks (64-Kbyte x 31 , 8-Kbyte x 8). Programming is done in units of 8 bits (Byte) or 16 bits (Word). All bits of data in one or multiple blocks can be erased simultaneously when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 39 memory blocks can be hardware protected by the block group. Byte/Word modes are available for read operation. These modes can be selected via $\overline{BYTE}$ pin. The device provides read access times of 70ns, 80ns and 90ns supporting high speed microprocessors to operate without any wait states.
The command set of K8D1716U is fully compatible with standard Flash devices. The device is controlled by chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$). Device operations are executed by selective command codes. The command codes to be combined wih addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8D1716U is implemented with Internal Program/Erase Algorithms to execute the program/erase operations. The Internal Program/Erase Algorithms are invoked by program/erase command sequences. The Internal Program Algorithm automatically programs and verifies data at specified addresses. The Internal Erase Algorithm automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8D1716U has means to indicate the status of completion of program/erase operations. The status can be indicated via the RY/$\overline{BY}$ pin, $\overline{Data}$ polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The device requires only 14 mA as active read current and 15 mA for program/erase operations.

Table 7. Operations Table

Operation		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	$\overline{WP}$/ACC	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Read	word	L	L	H	H	L/H	A9	A6	A1	A0	DQ15	DOUT	DOUT	H
	byte	L	L	H	L		A9	A6	A1	A0	A-1	High-Z	DOUT	H
Stand-by		VCC ± 0.3V	X	X	X	(2)	X	X	X	X	High-Z	High-Z	High-Z	(2)
Output Disable		L	H	H	X	L/H	X	X	X	X	High-Z	High-Z	High-Z	H
Reset		X	X	X	X	L/H	X	X	X	X	High-Z	High-Z	High-Z	L
Write	word	L	H	L	H	(4)	A9	A6	A1	A0	DIN	DIN	DIN	H
	byte	L	H	L	L		A9	A6	A1	A0	A-1	High-Z	DIN	H
Enable Block Group Protect (3)		L	H	L	X	L/H	X	L	H	L	X	X	DIN	VID
Enable Block Group Unprotect (3)		L	H	L	X	(4)	X	H	H	L	X	X	DIN	VID
Temporary Block Group		X	X	X	X	(4)	X	X	X	X	X	X	X	VID
Auto Select Manufacturer ID (5)		L	L	H	X	L/H	VID	L	L	L	X	X	Code(See Table 9)	H
Auto Select Device Code (5)		L	L	H	X	L/H	VID	L	L	H	X	X	Code(See Table 9)	H

Notes :
1. L = VIL (Low), H = VIH (High), VID = 8.5V~12.5V, DIN = Data in, DOUT = Data out, X = Don't care.
2. $\overline{WP}$/ACC and $\overline{RESET}$ pin are asserted at Vcc±0.3 V or Vss±0.3 V in the Stand-by mode.
3. Addresses must be composed of the Block address (A12 - A19).
   The Block Protect and Unprotect operations may be implemented via programming equipment too.
   Refer to the "Block Group Protection and Unprotection".
4. If $\overline{WP}$/ACC=VIL, the two outermost boot blocks is protected. If $\overline{WP}$/ACC=VIH, the two outermost boot block protection depends on whether those blocks were last protected or unprotected using the method described in "Block Group Protection and Unprotection". If $\overline{WP}$/ACC=VHH, all blocks will be temporarily unprotected.
5. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 9.

COMMAND DEFINITIONS

The K8D1716U operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 8. Note that Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Block Erase Operation is in progress.

Table 8. Command Sequences

Command Sequence		Cycle	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
			Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
Read	Addr	1	RA											
	Data		RD											
Reset	Addr	1	XXXH											
	Data		F0H											
Autoselect Manufacturer ID (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X00H	DA/ X00H				
	Data		AAH		55H		90H		ECH					
Autoselect Device Code (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA/ X01H	DA/ X02H				
	Data		AAH		55H		90H		(See Table 9)					
Autoselect Block Group Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	BA / X02H	BA/ X04H				
	Data		AAH		55H		90H		(See Table 9)					
Auto Select Secode Block Factory Protect Verify (2,3)	Addr	4	555H	AAAH	2AAH	555H	DA/ 555H	DA/ AAAH	DA / X03H	DA/ X06H				
	Data		AAH		55H		90H		(See Table 9)					
Enter Secode Block Region	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		88H							
Exit Secode Block Region	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	XXXH					
	Data		AAH		55H		90H		00H					
Program	Addr	4	555H	AAAH	2AAH	555H	555H	AAAH	PA					
	Data		AAH		55H		A0H		PD					
Unlock Bypass	Addr	3	555H	AAAH	2AAH	555H	555H	AAAH						
	Data		AAH		55H		20H							
Unlock Bypass Program	Addr	2	XXXH		PA									
	Data		A0H		PD									
Unlock Bypass Reset	Addr	2	XXXH		XXXH									
	Data		90H		00H									
Chip Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	555H	AAAH
	Data		AAH		55H		80H		AAH		55H		10H	
Block Erase	Addr	6	555H	AAAH	2AAH	555H	555H	AAAH	555H	AAAH	2AAH	555H	BA	
	Data		AAH		55H		80H		AAH		55H		30H	
Block Erase Suspend (4, 5)	Addr	1	XXXH											
	Data		B0H											
Block Erase Resume	Addr	1	XXXH											
	Data		30H											
CFI Query (6)	Addr	1	55H	AAH										
	Data		98H											

Notes : 1. RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data
DA : Dual Bank Address, BA : Block Address (A12 - A19), X = Don't care .
2. To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
3. The 4th cycle data of Autoselect mode is output data.
The 3rd and 4th cycle bank addresses of Autoselect mode must be same.
4. The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
5. The Erase Suspend command is applicable only to the Block Erase operation.
6. Command is valid when the device is in read mode or Autoselect mode.
7. DQ8 - DQ15 are don't care in command sequence, but RD and PD is excluded.
8. A11 - A19 are also don't care, except for the case of special notice.

Table 9. K8D1716U Autoselect Codes, (High Voltage Method)

Description	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
												$\overline{BYTE}$ =V_{IH}	$\overline{BYTE}$ =V_{IL}	
Manufacturer ID	L	L	H	DA	X	V_{ID}	X	L	X	L	L	X	X	ECH
Device Code K8D1716UT (Top Boot Block)	L	L	H	DA	X	V_{ID}	X	L	X	L	H	22H	X	75H
Device Code K8D1716UB (Bottom Boot Block)	L	L	H	DA	X	V_{ID}	X	L	X	L	H	22H	X	77H
Block Protection Verification	L	L	H	BA	X	V_{ID}	X	L	X	H	L	X	X	01H (Protected), 00H (Unprotected)
Secode Block (2) Indicator Bit (DQ7)	L	L	H	DA	X	V_{ID}	X	L	X	H	H	X	X	80H (Factory locked), 00H (Not factory locked)

Notes : 1. L=Logic Low=V_{IL}, H=Logic High=V_{IH}, DA=Dual Bank Address, BA=Block Address, X=Don't care.
2. Secode Block : Security Code Block.

DEVICE OPERATION

Byte/Word Mode

If the $\overline{BYTE}$ pin is set at logical "1" , the device is in word mode, DQ0-DQ15 are active. Otherwise the $\overline{BYTE}$ pin is set at logical "0" , the device is in byte mode, DQ0-DQ7 are active. DQ8-DQ14 are in the High-Z state and DQ15 pin is used as an input for the LSB (A-1) address pin.

Read Mode

The K8D1716U is controlled by Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.

Standby Mode

The K8D1716U features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is deselected by making $\overline{CE}$ high ($\overline{CE}$ = V_{IH}). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE}$ = V_{IH}). The output pins are in high impedance state.

Automatic Sleep Mode

K8D1716U features Automatic Sleep Mode to minimize the device power consumption. Since the device typically draws 5μA of the current in Automatic Sleep Mode, this feature plays an extremely important role in battery-powered applications. When addresses remain steady for t_{AA}+50ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

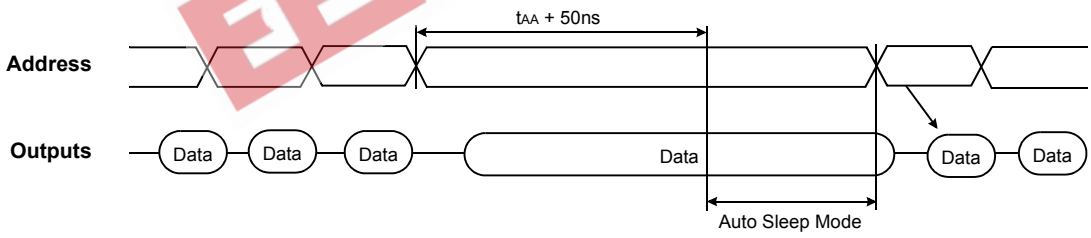
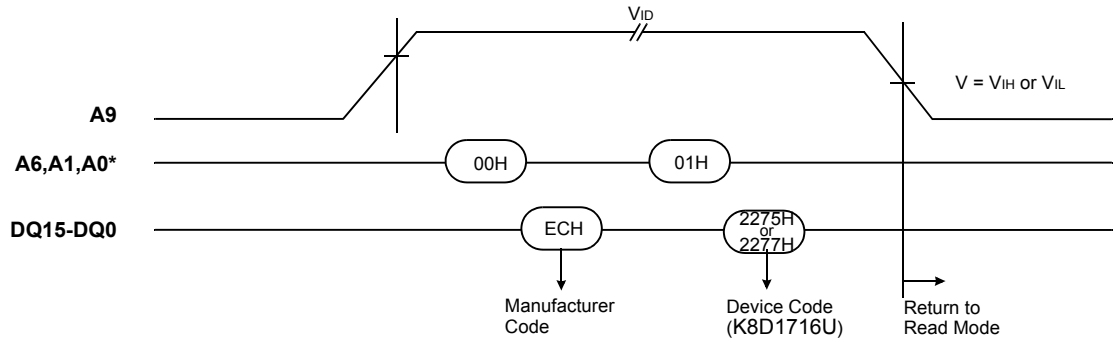


Figure 1. Auto Sleep Mode Operation

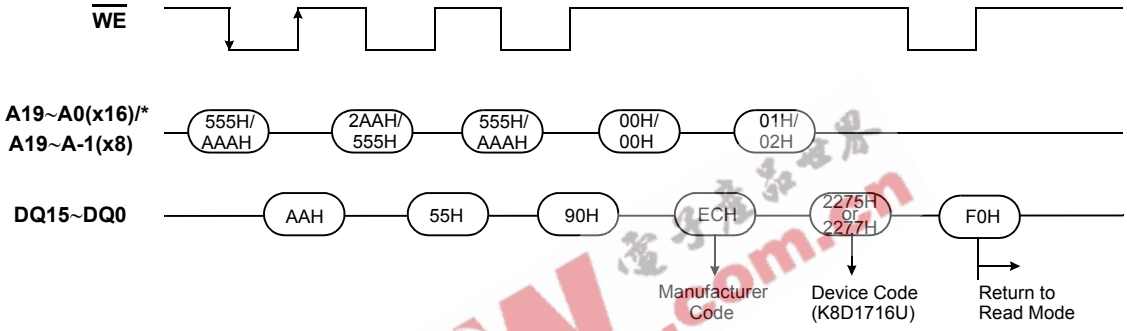
Autoselect Mode

The K8D1716U offers the Autoselect Mode to identify manufacturer and device type by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. In addition, this mode allows the verification of the status of write protected blocks. This mode is used by two method. The one is high voltage method to be required V_{ID} (8.5V~12.5V) on address pin A9. When A9 is held at V_{ID} and the bank address or block address is asserted, the device outputs the valid data via DQ pins(see Table 9 and Figure 2). The rest of addresses except A0, A1 and A6 are Don't Care. The other is autoselect command method that the autoselect code is accessible by the commamd sequence without V_{ID}. The manufacturer and device code may also be read via the command register. The Command Sequence is shown in Table 8 and Figure 3. The autoselect operation of block protect verification is initiated by first writing two unlock cycle. The third cycle must contain the bank address and autoselect command (90H). If Block address while (A6, A1, A0) = (0,1,0) is finally asserted on the address pin, it will produce a logical "1" at the device output DQ0 to indicate a write protected block or a logical "0" at the device output DQ0 to indicate a write unprotected block. To terminate the autoselect operation, write Reset command (F0H) into the command register.



Note : The addresses other than A0 , A1 and A6 are Don't care. Please refer to Table 9 for device code.

Figure 2. Autoselect Operation (by high voltage method)



Note : The 3rd Cycle and 4th Cycle address must include the same bank address. Please refer to Table 9 for device code.

Figure 3. Autoselect Operation (by command sequence method)

Write (Program/Erase) Mode

The K8D1716U executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

The K8D1716U can be programmed in units of a word or a byte. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

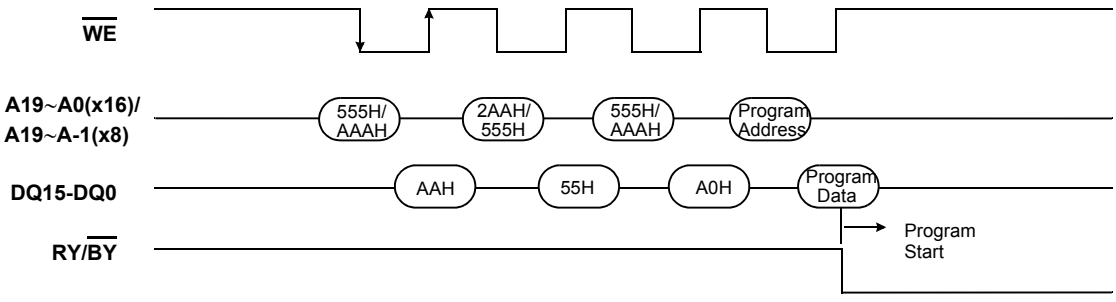


Figure 4. Program Command Sequence

Unlock Bypass

The K8D1716U provides the unlock bypass mode to save its program time for program operation. The mode is invoked by the unlock bypass command sequence. Then, the unlock bypass program command sequence is required to program the device.
Unlike the standard program command sequence that contains four bus cycles, the unlock bypass program command sequence comprises only two bus cycles.
The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program command sequence is necessary to program in this mode. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode.
The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last WE or CE pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

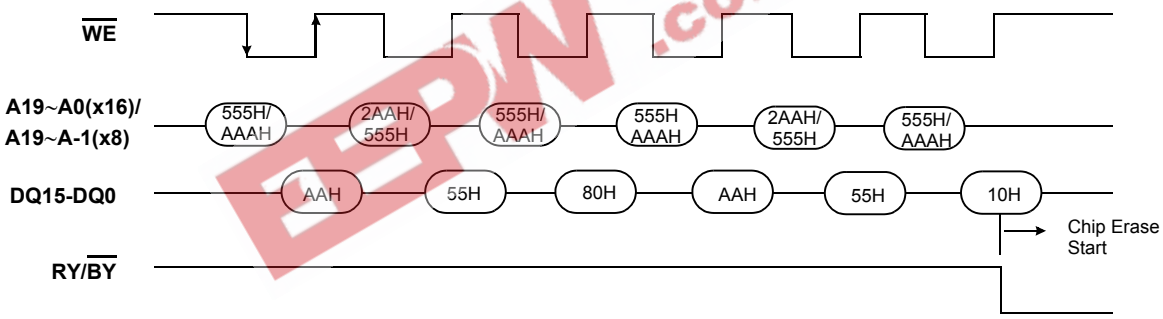


Figure 5. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 8. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of WE or CE, while the Block Erase command is latched on the rising edge of WE or CE.
Multiple blocks can be erased sequentially by writing the six bus-cycle operation in Figure 6. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50μs (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50μs "time window", otherwise the Block Erase command will be ignored. The 50μs "time window" is reset when the falling edge of the WE occurs within the 50μs of "time window" to latch the Block Erase command. During the 50μs of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50μs of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command during Block Erase operation.

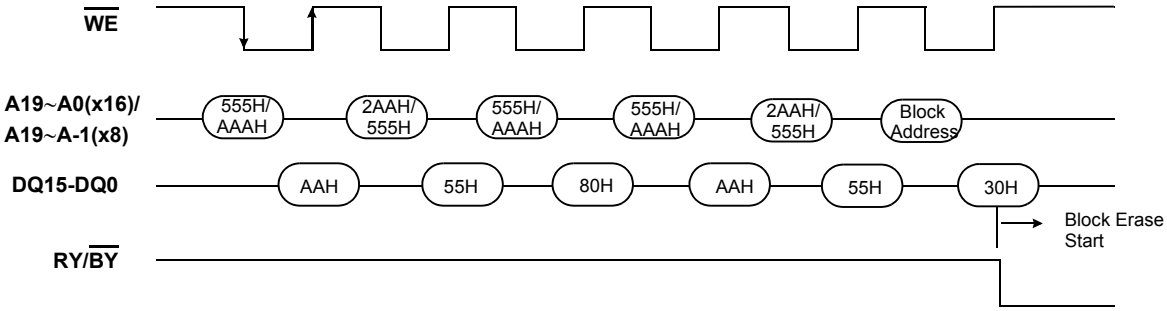


Figure 6. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50μs. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20μs to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50μs) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in Don't Care state.

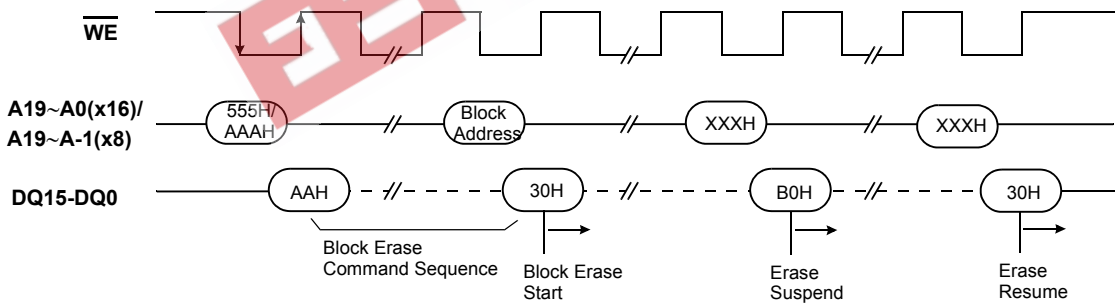


Figure 7. Erase Suspend/Resume Command Sequence

Read While Write

The K8D1716U provides dual bank memory architecture that divides the memory array into two banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with dual bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation.
The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from Bank1 and another blocks from Bank2 are loaded all together for the multi-block erase operation.

Block Group Protection & Unprotection

The K8D1716U feature hardware block group protection. This feature will disable both program and erase operations in any combination of twenty five block groups of memory. Please refer to Tables 10 and 11. The block group protection feature is enabled using programming equipment at the user's site. The device is shipped with all block groups unprotected.
This feature can be hardware protected or unprotected. If a block is protected, program or erase command in the protected block will be ignored by the device. The protected block can only be read. This is useful method to preserve an important program data. The block group unprotection allows the protected blocks to be erased or programed. All blocks must be protected before unprotect operation is executing. The block group protection and unprotection can be implemented by two methods.
The first method needs the following conditions.

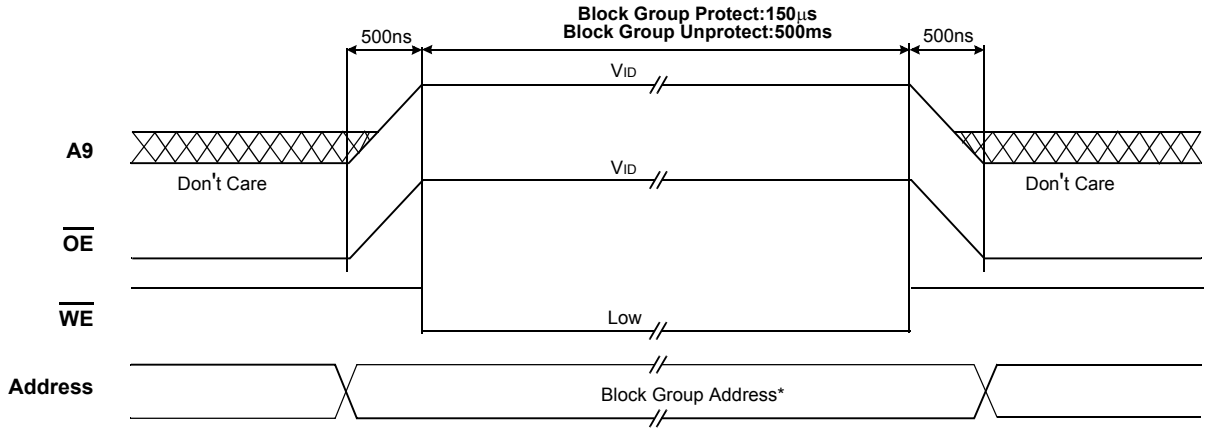
Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Block Group Protect	L	H	L	X	X	L	H	L	X	X	D_{IN}	V_{ID}
Block Group Unprotect	L	H	L	X	X	H	H	L	X	X	D_{IN}	V_{ID}

Address must be inputted to the block group address (A12~A19) during block group protection operation. Please refer to Figure 9 (Algorithm) and Switching Waveforms of Block Group Protect & Unprotect Operations.

The second method needs the following conditions in order to keep backward compatibility. Please refer to Figure 8.

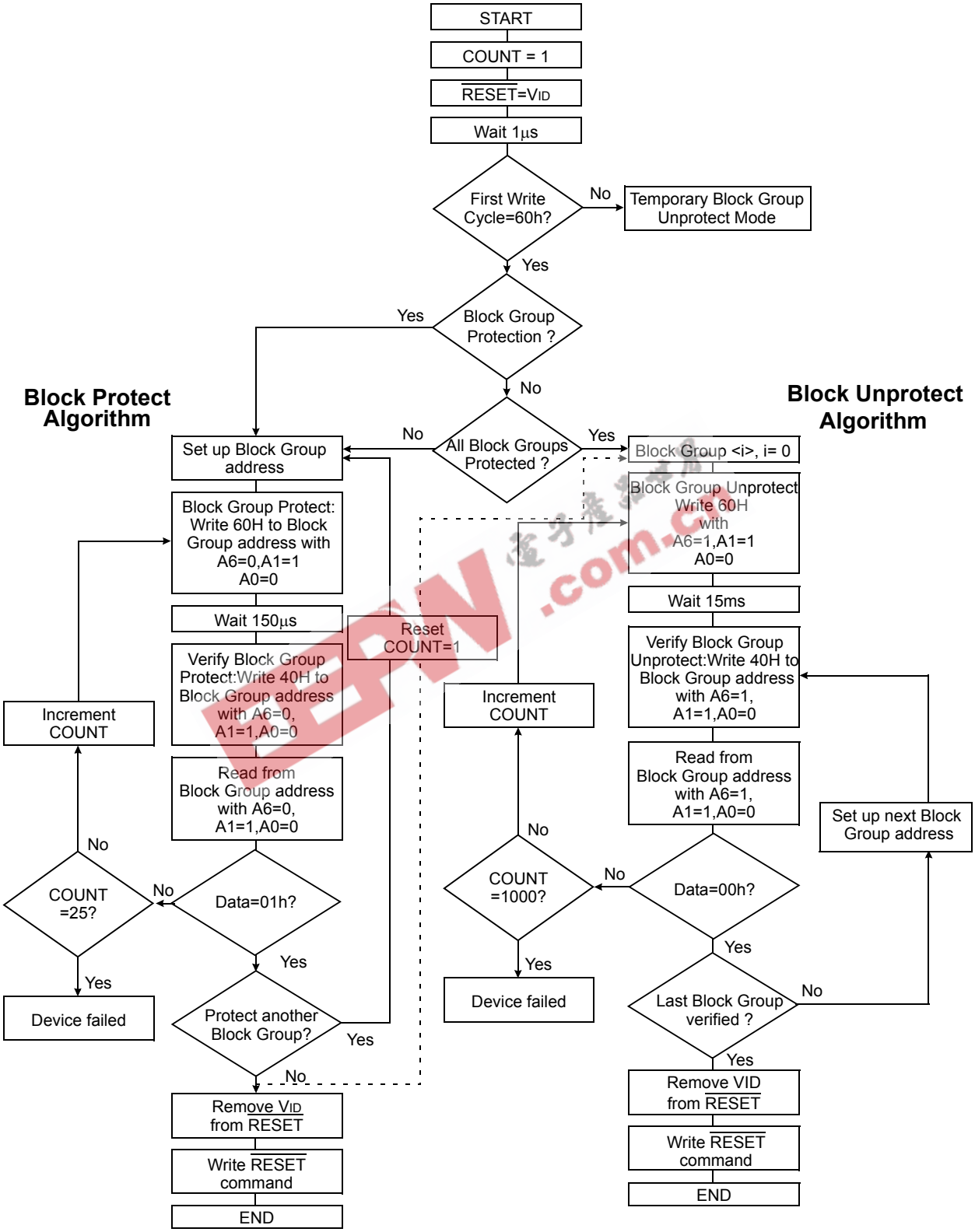
Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BYTE}$	A9	A6	A1	A0	DQ15/ A-1	DQ8/ DQ14	DQ0/ DQ7	$\overline{RESET}$
Block Group Protect	L	V_{ID}	⎍	X	V_{ID}	L	H	L	X	X	X	H
Block Group Unprotect	L	V_{ID}	⎍	X	V_{ID}	H	H	L	X	X	X	H

The K8D1716U needs the recovery time (20μs) from the rising edge of $\overline{WE}$ in order to execute its program, erase and read operations.



Notes : * Block Group Address is Don't Care during Block Group Unprotection.

Figure 8. Block Group Protect Sequence (The second method)



Note : All blocks must be protected before unprotect operation is executing.

Figure 9. Block Group Protection & Unprotection Algorithms

Table 10. Block Group Address (Top Boot Block)

Block Group	Block Address								Block
	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	X	X	X	BA0
BGA1	0	0	0	0	1	X	X	X	BA1 to BA3
				1	0				
				1	1				
BGA2	0	0	1	X	X	X	X	X	BA4 to BA7
BGA3	0	1	0	X	X	X	X	X	BA8 to BA11
BGA4	0	1	1	X	X	X	X	X	BA12 to BA15
BGA5	1	0	0	X	X	X	X	X	BA16 to BA19
BGA6	1	0	1	X	X	X	X	X	BA20 to BA23
BGA7	1	1	0	X	X	X	X	X	BA24 to BA27
BGA8	1	1	1	0	0	X	X	X	BA28 to BA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
BGA9	1	1	1	1	1	0	0	0	BA31
BGA10	1	1	1	1	1	0	0	1	BA32
BGA11	1	1	1	1	1	0	1	0	BA33
BGA12	1	1	1	1	1	0	1	1	BA34
BGA13	1	1	1	1	1	1	0	0	BA35
BGA14	1	1	1	1	1	1	0	1	BA36
BGA15	1	1	1	1	1	1	1	0	BA37
BGA16	1	1	1	1	1	1	1	1	BA38

Table 11. Block Group Address (Bottom Boot Block)

Block Group	Block Address								Block
	A19	A18	A17	A16	A15	A14	A13	A12	
BGA0	0	0	0	0	0	0	0	0	BA0
BGA1	0	0	0	0	0	0	0	1	BA1
BGA2	0	0	0	0	0	0	1	0	BA2
BGA3	0	0	0	0	0	0	1	1	BA3
BGA4	0	0	0	0	0	1	0	0	BA4
BGA5	0	0	0	0	0	1	0	1	BA5
BGA6	0	0	0	0	0	1	1	0	BA6
BGA7	0	0	0	0	0	1	1	1	BA7
BGA8	0	0	0	1	1	X	X	X	BA8 to BA10
				1	0				
				0	1				
BGA9	0	0	1	X	X	X	X	X	BA11 to BA14
BGA10	0	1	0	X	X	X	X	X	BA15 to BA18
BGA11	0	1	1	X	X	X	X	X	BA19 to BA22
BGA12	1	0	0	X	X	X	X	X	BA23 to BA26
BGA13	1	0	1	X	X	X	X	X	BA27 to BA30
BGA14	1	1	0	X	X	X	X	X	BA31 to BA34
BGA15	1	1	1	0	0	X	X	X	BA35 to BA37
				0	1				
				1	0				
BGA16	1	1	1	1	1	X	X	X	BA38

Temporary Block Group Unprotect

The protected blocks of the K8D1716U can be temporarily unprotected by applying high voltage (V_{ID} = 8.5V~12.5V) to the $\overline{RESET}$ pin. In this mode, previously protected blocks can be programmed or erased with the program or erase command routines. When the $\overline{RESET}$ pin goes high ($\overline{RESET}$ = V_{IH}), all the previously protected blocks will be protected again. If the $\overline{WP}$/ACC pin is asserted at V_{IL} , the two outermost boot blocks remain protected.

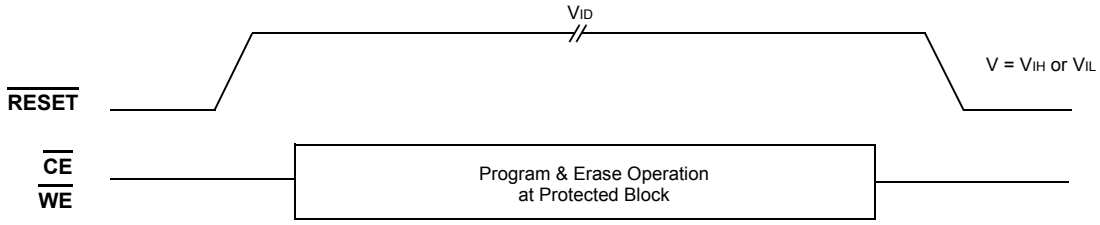


Figure 10. Temporary Block Group Unprotect Sequence

Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC pin has two useful functions. The one is that certain boot block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC pin is asserted at V_{IL}, the device can not perform program and erase operation in the two "outermost" 8K byte boot blocks independently of whether those blocks were protected or unprotected using the method described in "Block Group protection/Unprotection".
The write protected blocks can only be read. This is useful method to preserve an important program data.
The two outermost 8K byte boot blocks are the two blocks containing the lowest addresses in a bottom-boot-configured device, or the two blocks containing the highest addresses in a top-boot-congfigured device.
(K8D1716UT : BA37 and BA38, K8D1716UB : BA0 and BA1)
When the $\overline{WP}$/ACC pin is asserted at V_{IH}, the device reverts to whether the two outermost 8K byte boot blocks were last set to be protected or unprotected. That is, block protection or unprotection for these two blocks depends on whether they were last protected or unprotected using the method described in "Block Group protection/unprotection".
Recommend that the $\overline{WP}$/ACC pin must not be in the state of floating or unconnected, or the device may be led to malfunction.

Secode(Security Code) Block Region

The Secode Block feature provides a Flash memory region to be stored unique and permanent identification code, that is, Electronic Serial Number (ESN), customer code and so on. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the Secode Block region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field.
The Secode Block is factory locked or customer lockable. Before the device is shipped, the factory locked Secode Block is written on the special code and it is protected. The Secode Indicator bit (DQ7) is permanently fixed at "1" and it is not changed. The customer lockable Secode Block is unprotected, therefore it is programmed and erased. The Secode Indicator bit (DQ7) of it is permanently fixed at "0" and it is not changed. But once it is protected, there is no procedure to unprotect and modify the Secode Block.
The Secode Block region is 64K bytes in length and is accessed through a new command sequence (see Table 8). After the system has written the Enter Secode Block command sequence, the system may read the Secode Block region by using the same addresses of the boot blocks (8KBx8). The K8D1716UT occupies the address of the byte mode 3F0000H to 3FFFFFH (word mode 1F8000H to 1FFFFFH) and the K8D1716UB type occupies the address of the byte mode 000000H to 00FFFFH (word mode 000000H to 007FFFH). This mode of operation continues until the system issues the Exit Secode Block command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to read mode.

Accelerated Program Operation

Accelerated program operation reduces the program time. This is one of two functions provided by the $\overline{WP}$/ACC pin. When the $\overline{WP}$/ACC pin is asserted as V_{HH}, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotecting any protected blocks, and reduces the program operation time. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the $\overline{WP}$/ACC pin returns the device to normal operation. **Recommend that the $\overline{WP}$/ACC pin must not be asserted at V_{HH} except accelerated program operation, or the device may be damaged. In addition, the $\overline{WP}$/ACC pin must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.**

Software Reset

The reset command provides that the bank is reseted to read mode or erase-suspend-read mode. The addresses are in Don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

Hardware Reset

The K8D1716U offers a reset feature by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin must be kept low (V_{IL}) for at least 500ns. When the $\overline{RESET}$ pin is driven low, any operation in progress will be terminated and the internal state machine will be reset to the standby mode after 20μs. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ pin is taken high, the device requires 200ns of wake-up time until outputs are valid for read access. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse.
The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc Power-up, $\overline{RESET}$ low must be asserted during power-up. After $\overline{RESET}$ goes high, the device is reset to the read mode.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 1.8V. If Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 1.8V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{CE}$, $\overline{OE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be "0", while $\overline{OE}$ is "1".

Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, byte/word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode(or address AAH in byte mode), the device enters the CFI mode. And then if the system writes the address shown in Table 12, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

Table 12. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	20H 22H 24H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	26H 28H	0002H 0000H
Address for Primary Extended Table	15H 16H	2AH 2CH	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	2EH 30H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	32H 34H	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	36H	0027H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	38H	0036H
Vpp Min. voltage(00H = no Vpp pin present)	1DH	3AH	0000H
Vpp Max. voltage(00H = no Vpp pin present)	1EH	3CH	0000H
Typical timeout per single byte/word write 2^N us	1FH	3EH	0004H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	40H	0000H
Typical timeout per individual block erase 2^N ms	21H	42H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	44H	0000H
Max. timeout for byte/word write 2^N times typical	23H	46H	0005H
Max. timeout for buffer write 2^N times typical	24H	48H	0000H
Max. timeout per individual block erase 2^N times typical	25H	4AH	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	4CH	0000H
Device Size = 2^N byte	27H	4EH	0015H
Flash Device Interface description	28H 29H	50H 52H	0002H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	54H 56H	0000H 0000H
Number of Erase Block Regions within device	2CH	58H	0002H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	5AH 5CH 5EH 60H	0007H 0000H 0020H 0000H
Erase Block Region 2 Information	31H 32H 33H 34H	62H 64H 66H 68H	001EH 0000H 0000H 0001H
Erase Block Region 3 Information	35H 36H 37H 38H	6AH 6CH 6EH 70H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	72H 74H 76H 78H	0000H 0000H 0000H 0000H

Table 12. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Addresses (Byte Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	80H 82H 84H	0050H 0052H 0049H
Major version number, ASCII	43H	86H	0031H
Minor version number, ASCII	44H	88H	0032H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	8AH	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	8CH	0002H
Block Protect 0 = Not Supported, 1 = Number of blocks in per group	47H	8EH	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	90H	0001H
Block Protect/Unprotect scheme 04=K8D1x16U mode	49H	92H	0004H
Simultaneous Operation (1) 00 = Not Supported, XX = Number of Blocks in Bank2	4AH	94H	00XXH
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	96H	0000H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page	4CH	98H	0000H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	9AH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	9CH	00C5H
Top/Bottom Boot Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device	4FH	9EH	000XH

Note :
1. The number of blocks in Bank2 is device dependent.
K8D1716U(8Mb/8Mb) = 10h (16blocks)

DEVICE STATUS FLAGS

The K8D1716U has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being excuted internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins or the RY/ $\overline{BY}$ pin. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3 and DQ2. The statuses are as follows :

Table 13. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle (Note 1)	1
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0

Notes :
1. DQ2 will toggle when the device performs successive read operations from the erase suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the device during the Erase operation, DQ7 will be low. If the device is placed in the Erase Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erased, DQ7 will be high. If a non-erased block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase Suspend Mode, an attempt to read an address that belongs to a block that is being erased will produce a high output of DQ6. If an address belongs to a block that is not being erased, toggling is halted and valid data is produced at DQ6.
If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

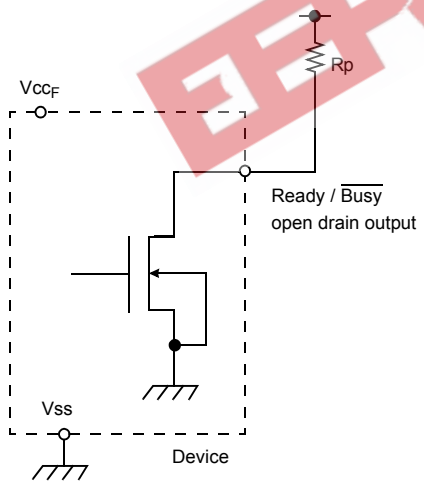
The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase Suspend mode, DQ2 toggles only if an address in the erasing block is read. If a non-erasing block address is read during the Erase Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. Combination of the status in DQ6 and DQ2 can be used to distinguish the erase operation from the program operation.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The K8D1716U has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the K8D1716U is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.
The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc_F\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ ball.

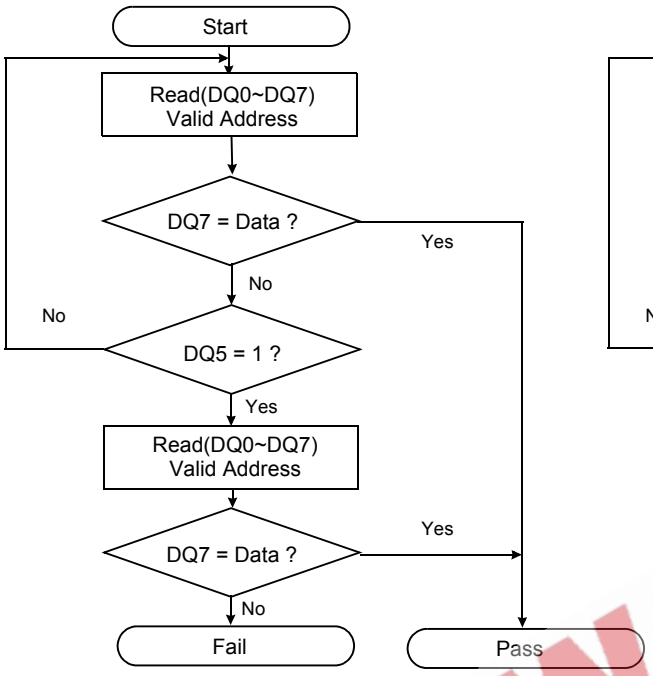


Figure 11. Data Polling Algorithms

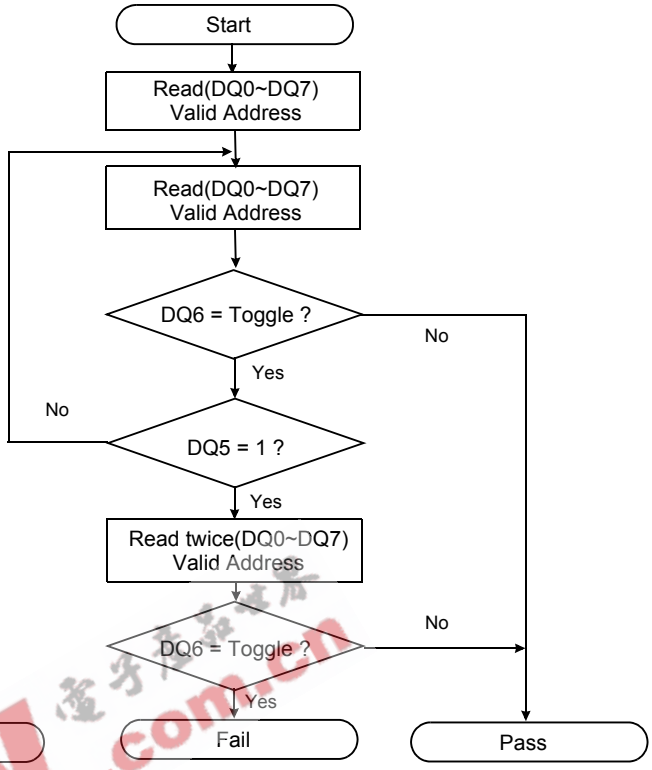
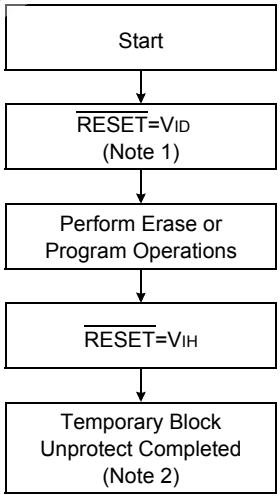


Figure 12. Toggle Bit Algorithms



Notes :
1. All protected block groups are unprotected.
   (If $\overline{WP}$/ACC = V_{IL} , the two outermost boot blocks remain protected)
2. All previously protected block groups are protected once again.

Figure 13. Temporary Block Group Unprotect Routine

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc	-0.5 to +4.0	V
	A9, $\overline{OE}$, $\overline{RESET}$	V_{IN}	-0.5 to +12.5	
	$\overline{WP}$/ACC		-0.5 to +12.5	
	All Other Pins		-0.5 to +4.0	
Temperature Under Bias	Commercial	T_{bias}	-10 to +125	°C
	Industrial		-40 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Commercial Temp.)	0 to +70	°C
		T_A (Industrial Temp.)	-40 to + 85	°C

Notes :
1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Minimum DC voltage is -0.5V on A9, $\overline{OE}$, $\overline{RESET}$ and $\overline{WP}$/ACC pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on A9, $\overline{OE}$, $\overline{RESET}$ pins is 12.5V which, during transitions, may overshoot to 14.0V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	2.7	3.0	3.6	V
Supply Voltage	Vss	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		– 1.0	-	+ 1.0	µA
A9,$\overline{OE}$,$\overline{RESET}$ Input Leakage Current	I_{LIT}	V_{CC}=V_{CCmax}, A9,$\overline{OE}$,$\overline{RESET}$=12.5V		-	-	35	µA
$\overline{WP}$/ACC Input Leakage Current	I_{LIW}	V_{CC}=V_{CCmax}, $\overline{WP}$/ACC=12.5V		-	-	35	µA
Output Leakage Current	I_{LO}	V_{OUT}=V_{SS} to V_{CC},V_{CC}=V_{CCmax},$\overline{OE}$=V_{IH}		– 1.0	-	+ 1.0	µA
Active Read Current (1)	I_{CC1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	5MHz	-	14	20	mA
			1MHz	-	3	6	
Active Write Current (2)	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}		-	15	30	mA
Read While Program Current (3)	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	25	50	mA
Read While Erase Current (3)	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	25	50	mA
Program While Erase Suspend Current	I_{CC5}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	35	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	ACC Pin	-	5	10	mA
			Vcc Pin	-	15	30	
Standby Current	I_{SB1}	V_{CC}=V_{CCmax},$\overline{CE}$, $\overline{RESET}$=V_{CC}±0.3V $\overline{WP}$/ACC= V_{CC}± 0.3V or Vss±0.3V		-	5	18	µA
Standby Current During Reset	I_{SB2}	V_{CC}=V_{CCmax}, $\overline{RESET}$=Vss± 0.3V, $\overline{WP}$/ACC=V_{CC}± 0.3V or Vss±0.3V		-	5	18	µA
Automatic Sleep Mode	I_{SB3}	V_{IH}=V_{CC}±0.3V, V_{IL}=V_{SS}±0.3V, $\overline{OE}$=V_{IL}, I_{OL}=I_{OH}=0		-	5	18	µA
Input Low Level	V_{IL}			-0.5	-	0.8	V
Input High Level	V_{IH}			0.7xVcc	-	Vcc+0.3	V
Voltage for $\overline{WP}$/ACC Block Temporarily Unprotect and Program Acceleration (4)	V_{HH}	V_{CC} = 3.0V ± 0.3V		8.5	-	12.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage for Autoselect and Block Protect (4)	V_{ID}	V_{CC} = 3.0V ± 0.3V	8.5	-	12.5	V
Output Low Level	V_{OL}	I_{OL}=100μA, V_{CC}=V_{CCmin}	-	-	0.4	V
Output High Level	V_{OH}	I_{OH}=-100μA, Vcc = V_{CCmin}	V_{CC}-0.4	-	-	V
Low Vcc Lock-out Voltage (5)	V_{LKO}		1.8	-	2.5	V

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
   The read current is typically 14 mA (@ VCC=3.0V , $\overline{OE}$ at VIH.)
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. The high voltage (V_{HH} or V_{ID}) must be used in the range of Vcc = 3.0V ± 0.3V
5. Not 100% tested.
6. Typical value are measured at Vcc = 3.0V,T_A=25°C , Not 100% tested.

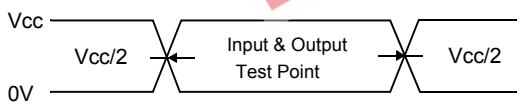
CAPACITANCE(T_A = 25 °C, V_{CC} = 3.3V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

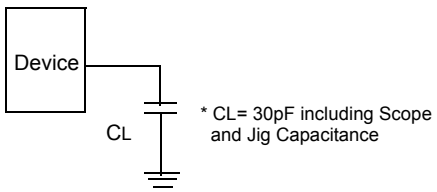
Note : Capacitance is periodically sampled and not 100% tested.

AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	C_L = 30pF



Input Pulse and Test Point



Output Load

AC CHARACTERISTICS

Read Operations

Parameter	Symbol	Vcc=2.7V~3.6V						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Read Cycle Time (1)	t_{RC}	70	-	80	-	90	-	ns
Address Access Time	t_{AA}	-	70	-	80	-	90	ns
Chip Enable Access Time	t_{CE}	-	70	-	80	-	90	ns
Output Enable Time	t_{OE}	-	25	-	25	-	35	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$ (1)	t_{OH}	0	-	0	-	0	-	ns

Note : 1. Not 100% tested.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{WE}$ Controlled Write

Parameter		Symbol	Vcc=2.7V~3.6V						Unit
			-7		-8		-9		
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		tWC	70	-	80	-	90	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	ns
		tASO	55	-	55	-	55	-	ns
Address Hold Time		tAH	45	-	45	-	45	-	ns
		tAHT	0	-	0	-	0	-	ns
Data Setup Time		tDS	35	-	35	-	45	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		tOES	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	tOEH1	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	tOEH2	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time		tCS	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		tCH	0	-	0	-	0	-	ns
Write Pulse Width		tWP	35	-	35	-	45	-	ns
Write Pulse Width High		tWPH	25	-	25	-	30	-	ns
Programming Operation	Word	tPGM	14(typ.)		14(typ.)		14(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		µs
Accelerated Programming Operation	Word	tACCPGM	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Block Erase Operation (2)		tBERS	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
Vcc Set Up Time		tVCS	50	-	50	-	50	-	µs
Write Recovery Time from RY/$\overline{BY}$		tRB	0	-	0	-	0	-	ns
$\overline{RESET}$ High Time Before Read		tRH	50	-	50	-	50	-	ns
$\overline{RESET}$ to Power Down Time		tRPD	20	-	20	-	20	-	µs
Program/Erase Valid to RY/$\overline{BY}$ Delay		tBUSY	90	-	90	-	90	-	ns
VID Rising and Falling Time		tVID	500	-	500	-	500	-	ns
$\overline{RESET}$ Pulse Width		tRP	500	-	500	-	500	-	ns
$\overline{RESET}$ Low to RY/BY High		tRRB	-	20	-	20	-	20	µs
$\overline{RESET}$ Setup Time for Temporary Unprotect		tRSP	1	-	1	-	1	-	µs
$\overline{RESET}$ Low Setup Time		tRSTS	500	-	500	-	500	-	ns
$\overline{RESET}$ High to Address Valid		tRSTW	200	-	200	-	200	-	ns
Read Recovery Time Before Write		tGHWL	0	-	0	-	0	-	ns
$\overline{CE}$ High during toggling bit polling		tCEPH	20	-	20	-	20	-	ns
$\overline{OE}$ High during toggling bit polling		tOEPH	20	-	20	-	20	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

AC CHARACTERISTICS
Write(Erase/Program)Operations
Alternate $\overline{CE}$ Controlled Writes

Parameter		Symbol	Vcc=2.7V~3.6V						Unit
			-7		-8		-9		
			Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		tWC	70	-	80	-	90	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	ns
Address Hold Time		tAH	45	-	45	-	45	-	ns
Data Setup Time		tDS	35	-	35	-	45	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	ns
Output Enable Setup Time (1)		tOES	0	-	0	-	0	-	ns
Output Enable Hold Time	Read (1)	tOEH1	0	-	0	-	0	-	ns
	Toggle and $\overline{Data}$ Polling (1)	tOEH2	10	-	10	-	10	-	ns
$\overline{WE}$ Setup Time		tWS	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		tWH	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		tCP	35	-	35	-	45	-	ns
$\overline{CE}$ Pulse Width High		tCPH	25	-	25	-	30	-	ns
Programming Operation	Word	tPGM	14(typ.)		14(typ.)		14(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		µs
Accelerated Programming Operation	Word	tACCPGM	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Block Erase Operation (2)		tBERS	0.7(typ.)		0.7(typ.)		0.7(typ.)		sec
$\overline{BYTE}$ Switching Low to Output HIGH-Z		tFLQZ	25	-	25	-	30	-	ns

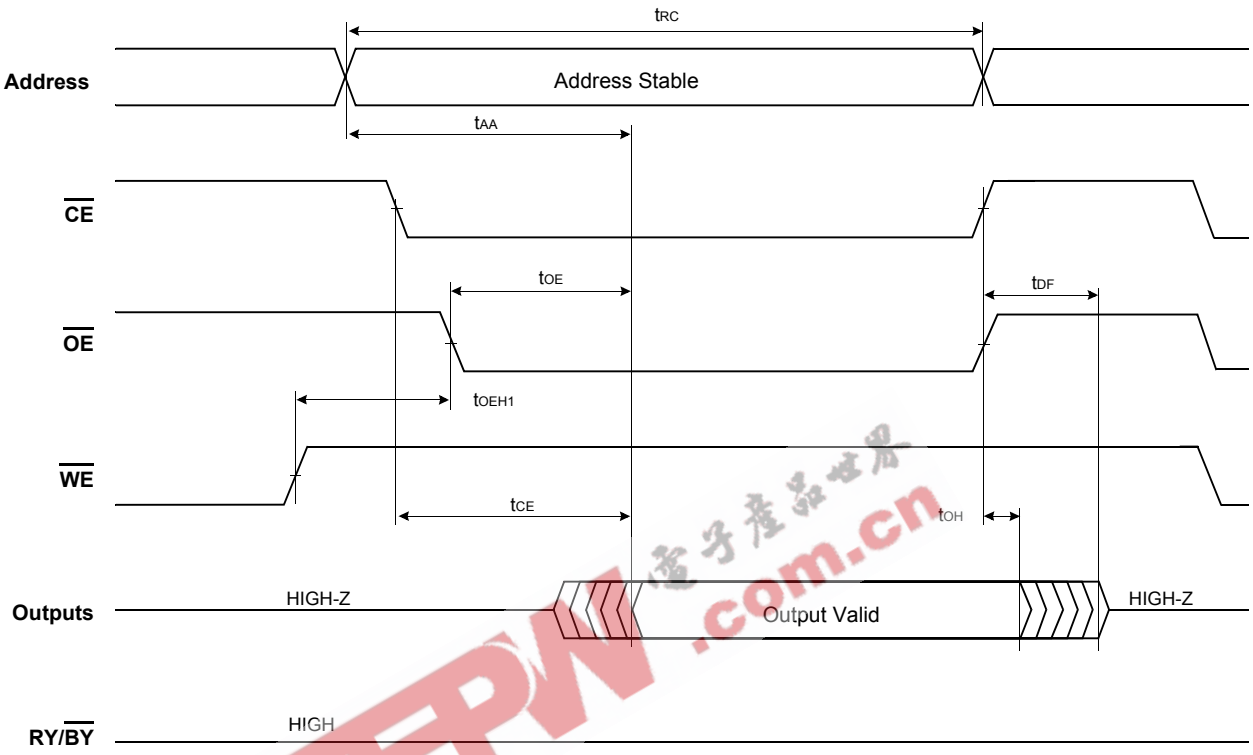
Notes : 1. Not 100% tested.
2.This does include the preprogramming time.

ERASE AND PROGRAM PERFORMANCE

Parameter		Limits			Unit	Comments
		Min	Typ	Max		
Block Erase Time		-	0.7	15	sec	Includes 00H programming prior to erasure
Chip Erase Time		-	25	-	sec	
Word Programming Time		-	14	330	µs	Excludes system-level overhead
Byte Programming Time		-	9	210	µs	Excludes system-level overhead
Accelerated Byte/Word Program Time	Word Mode	-	9	210	µs	Excludes system-level overhead
	Byte Mode	-	7	150	µs	Excludes system-level overhead
Chip Programming Time	Word Mode	-	14	42	sec	Excludes system-level overhead
	Byte Mode	-	18	54	sec	
Erase/Program Endurance		100,000	-	-	cycles	Minimum 100,000 cycles guaranteed

Notes : 1. 25 °C, Vcc = 3.0V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Internal Erase Routine, all bytes are programmed to 00H before erasure.

SWITCHING WAVEFORMS
Read Operations

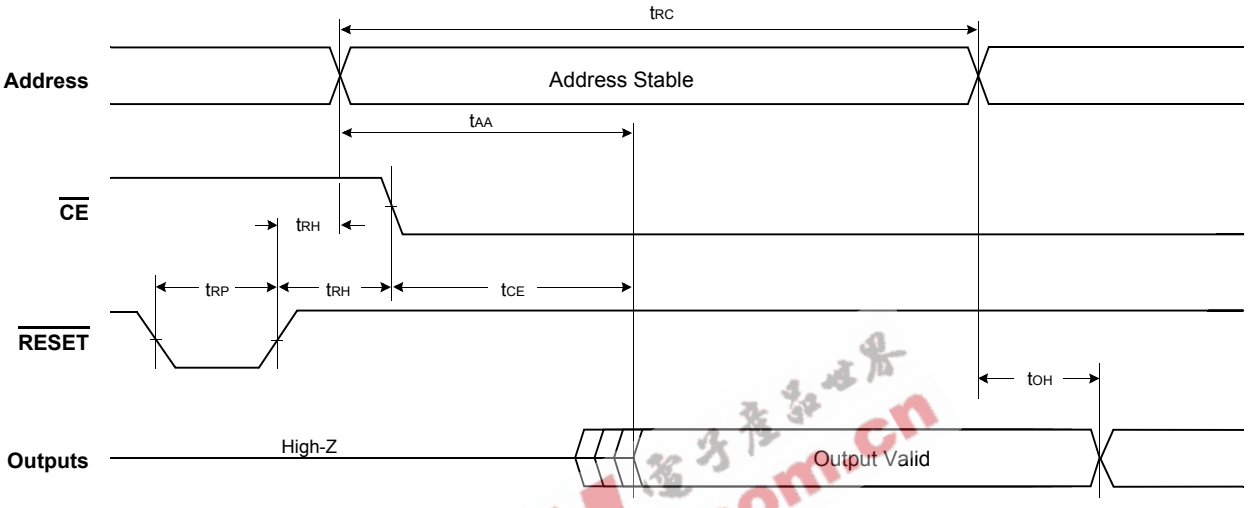


Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	70	-	80	-	90	-	ns
Address Access Time	tAA	-	70	-	80	-	90	ns
Chip Enable Access Time	tCE	-	70	-	80	-	90	ns
Output Enable Time	tOE	-	25	-	25	-	35	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	tDF	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	tOH	0	-	0	-	0	-	ns
$\overline{OE}$ Hold Time	tOEH1	0	-	0	-	0	-	ns

Note : 1. Not 100% tested.

SWITCHING WAVEFORMS

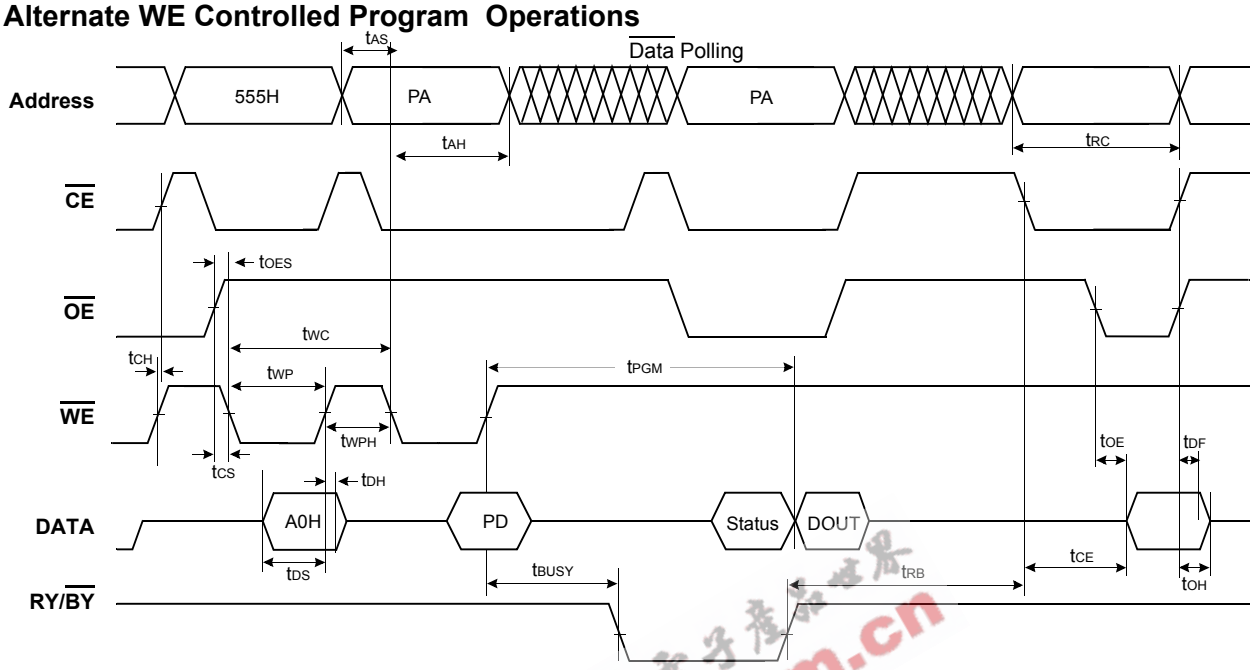
Hardware Reset/Read Operations



Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	70	-	80	-	90	-	ns
Address Access Time	tAA	-	70	-	80	-	90	ns
Chip Enable Access Time	tCE	-	70	-	80	-	90	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	tOH	0	-	0	-	0	-	ns
$\overline{RESET}$ Pulse Width	tRP	500	-	500	-	500	-	ns
$\overline{RESET}$ High Time Before Read	tRH	50	-	50	-	50	-	ns

SWITCHING WAVEFORMS

Alternate $\overline{WE}$ Controlled Program Operations

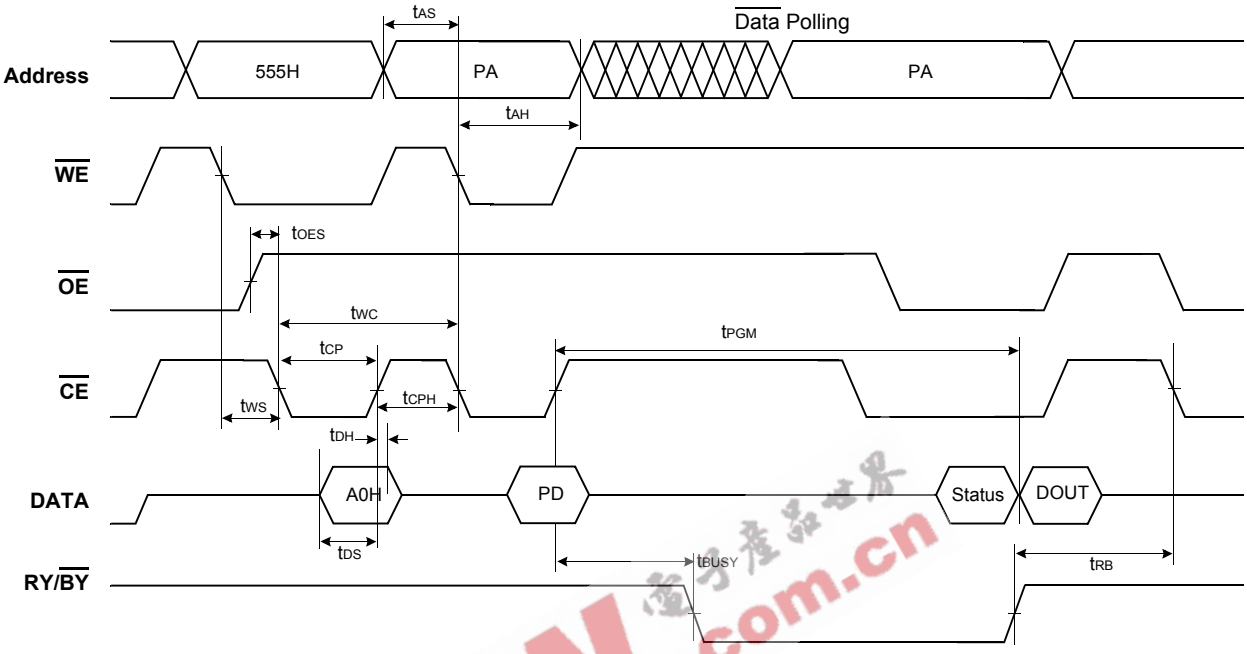


Notes : 1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Parameter		Symbol	-7		-8		-9		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time		tWC	70	-	80	-	90	-	ns
Address Setup Time		tAS	0	-	0	-	0	-	ns
Address Hold Time		tAH	45	-	45	-	45	-	ns
Data Setup Time		tDS	35	-	35	-	45	-	ns
Data Hold Time		tDH	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time		tCS	0	-	0	-	0	-	ns
$\overline{CE}$ Hold Time		tCH	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time		tOES	0	-	0	-	0	-	ns
Write Pulse Width		tWP	35	-	35	-	45	-	ns
Write Pulse Width High		tWPH	25	-	25	-	30	-	ns
Programming Operation	Word	tPGM	14(typ.)		14(typ.)		14(typ.)		us
	Byte		9(typ.)		9(typ.)		9(typ.)		us
Accelerated Programming Operation	Word	tACCPGM	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Read Cycle Time		tRC	70	-	80	-	90	-	ns
Chip Enable Access Time		tCE	-	70	-	80	-	90	ns
Output Enable Time		tOE	-	25	-	25	-	35	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time		tDF	-	16	-	16	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$		tOH	0	-	0	-	0	-	ns
Program/Erase Valide to RY/$\overline{BY}$ Delay		tBUSY	90	-	90	-	90	-	ns
Recovery Time from RY/$\overline{BY}$		tRB	0	-	0	-	0	-	ns

SWITCHING WAVEFORMS

Alternate $\overline{CE}$ Controlled Program Operations

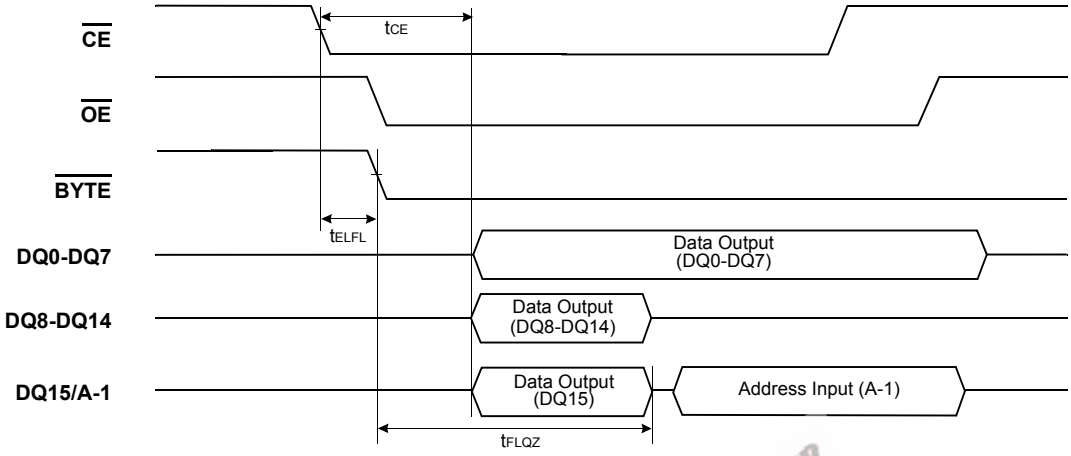


Notes :
1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

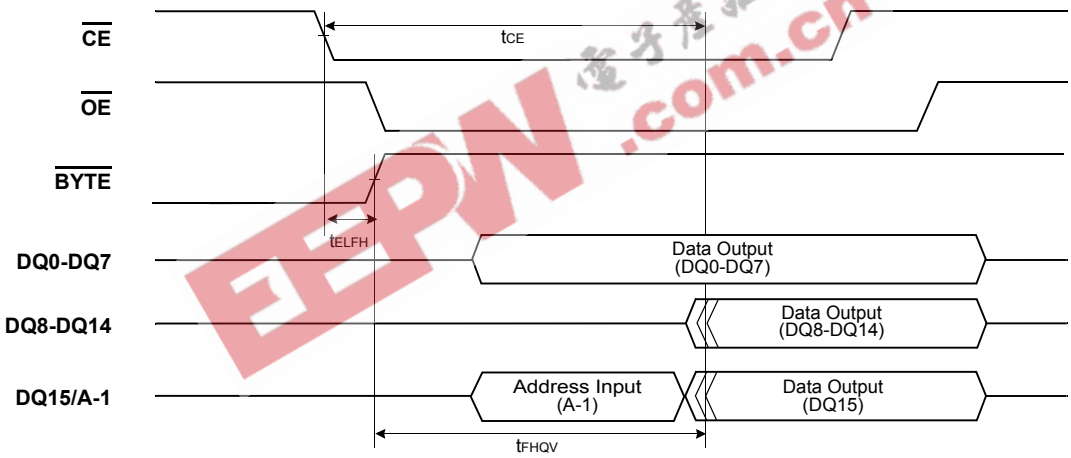
Parameter		Symbol	-7		-8		-9		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time		t_{WC}	70	-	80	-	90	-	ns
Address Setup Time		t_{AS}	0	-	0	-	0	-	ns
Address Hold Time		t_{AH}	45	-	45	-	45	-	ns
Data Setup Time		t_{DS}	35	-	35	-	45	-	ns
Data Hold Time		t_{DH}	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time		t_{OES}	0	-	0	-	0	-	ns
$\overline{WE}$ Setup Time		t_{WS}	0	-	0	-	0	-	ns
$\overline{WE}$ Hold Time		t_{WH}	0	-	0	-	0	-	ns
$\overline{CE}$ Pulse Width		t_{CP}	35	-	35	-	45	-	ns
$\overline{CE}$ Pulse Width High		t_{CPH}	25	-	25	-	30	-	ns
Programming Operation	Word	t_{PGM}	14(typ.)		14(typ.)		14(typ.)		µs
	Byte		9(typ.)		9(typ.)		9(typ.)		µs
Accelerated Programming Operation	Word	t_{ACCPGM}	9(typ.)		9(typ.)		9(typ.)		µs
	Byte		7(typ.)		7(typ.)		7(typ.)		µs
Program/Erase Valide to RY/$\overline{BY}$ Delay		t_{BUSY}	90	-	90	-	90	-	ns
Recovery Time from RY/$\overline{BY}$		t_{RB}	0	-	0	-	0	-	ns

SWITCHING WAVEFORMS

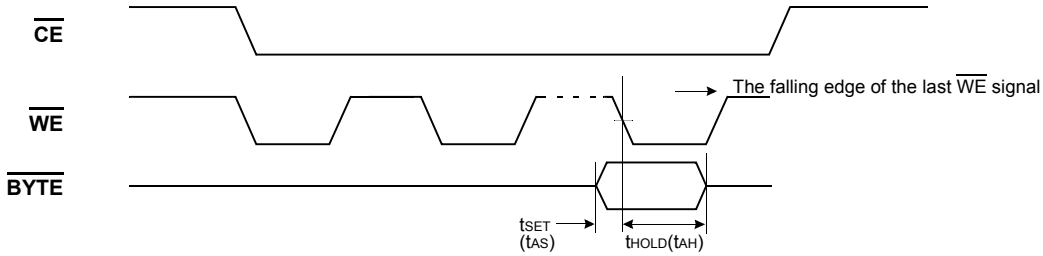
Word to Byte Timing Diagram for Read Operation



Byte to Word Timing Diagram for Read Operation



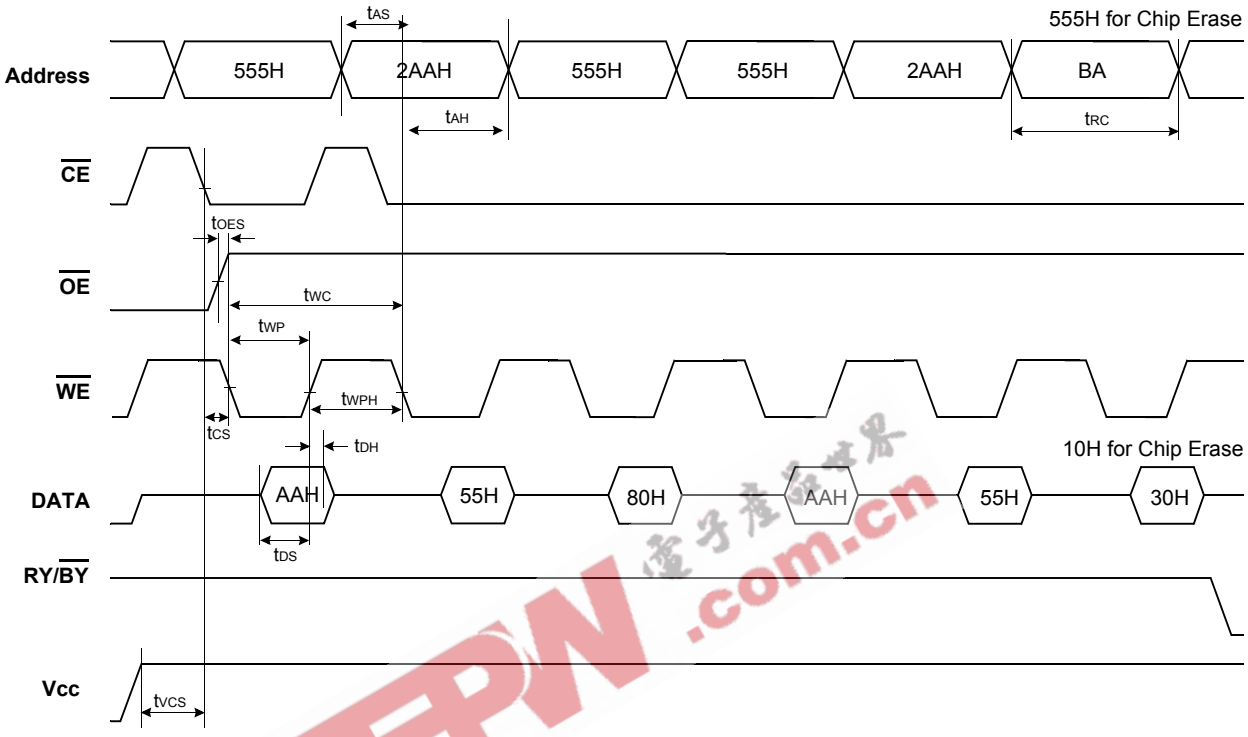
BYTE Timing Diagram for Write Operation



Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Access Time	tCE	-	70	-	80	-	90	ns
CE to BYTE Switching Low or High	tELFL/tELFH	-	5	-	5	-	5	ns
BYTE Switching Low to Output HIGH-Z	tFLQZ	-	25	-	25	-	30	ns
BYTE Switching High to Output Active	tFHQV	-	25	-	25	-	35	ns

SWITCHING WAVEFORMS

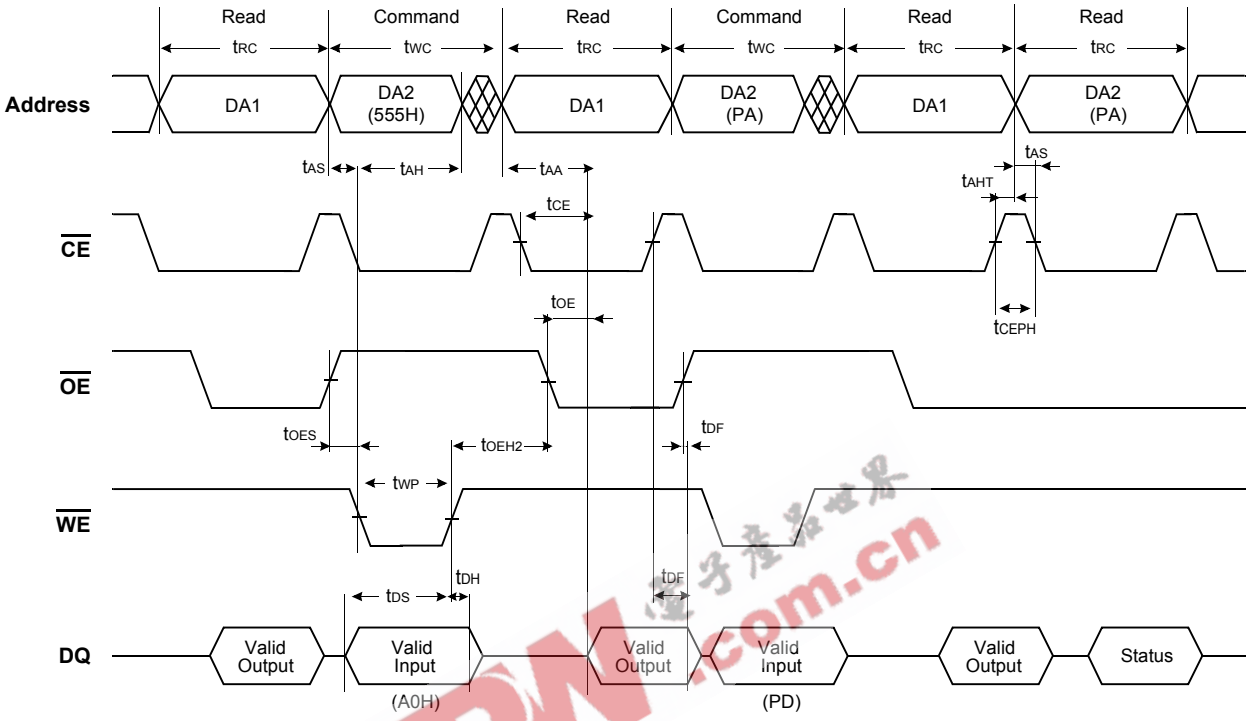
Chip/Block Erase Operations



Note : BA : Block Address

Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	70	-	80	-	90	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Hold Time	tAH	45	-	45	-	45	-	ns
Data Setup Time	tDS	35	-	35	-	45	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	ns
$\overline{OE}$ Setup Time	tOES	0	-	0	-	0	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	0	-	0	-	ns
Write Pulse Width	tWP	35	-	35	-	45	-	ns
Write Pulse Width High	tWPH	25	-	25	-	30	-	ns
Read Cycle Time	tRC	70	-	80	-	90	-	ns
Vcc Set Up Time	tVCS	50	-	50	-	50	-	µs

SWITCHING WAVEFORMS
Read While Write Operations

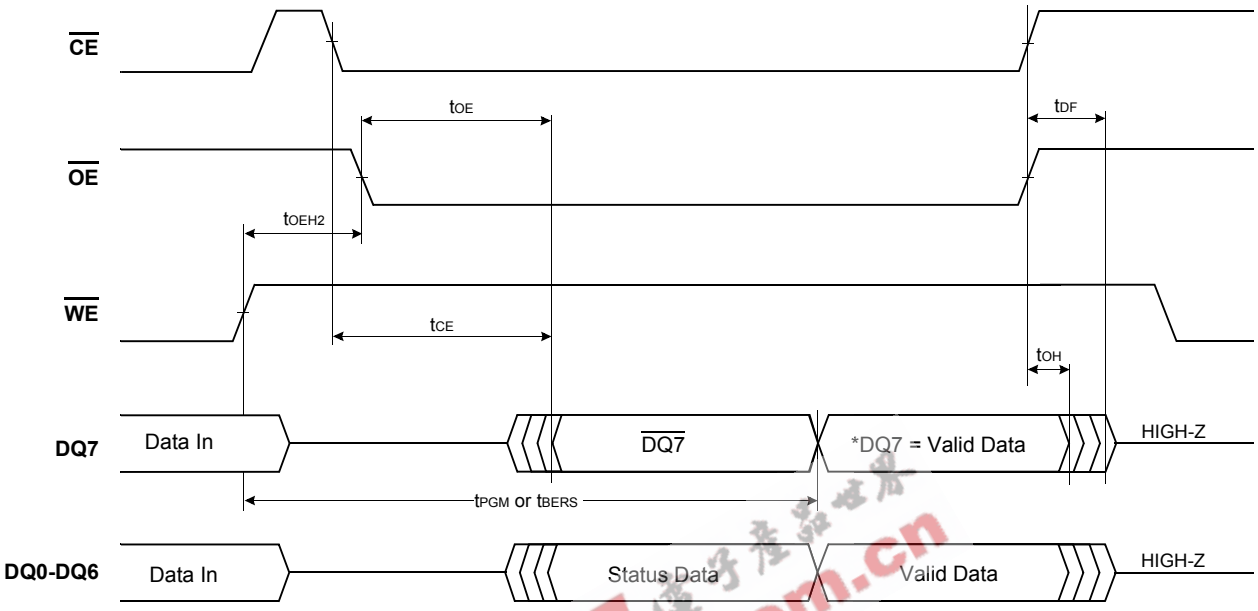


Note : This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2
PA = Program Address at one bank , RA = Read Address at the other bank, PD = Program Data In , RD = Read Data Out

Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	70	-	80	-	90	-	ns
Write Pulse Width	tWP	35	-	35	-	45	-	ns
Write Pulse Width High	tWPH	25	-	25	-	30	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Hold Time	tAH	45	-	45	-	45	-	ns
Data Setup Time	tDS	35	-	35	-	45	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	ns
Read Cycle Time	tRC	70	-	80	-	90	-	ns
Chip Enable Access Time	tCE	-	70	-	80	-	90	ns
Address Access Time	tAA	-	70	-	80	-	90	ns
Output Enable Access Time	tOE	-	25	-	25	-	35	ns
$\overline{OE}$ Setup Time	tOES	0	-	0	-	0	-	ns
$\overline{OE}$ Hold Time	tOEH2	10	-	10	-	10	-	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time	tDF	-	16	-	16	-	16	ns
Address Hold Time	tAHT	0	-	0	-	0	-	ns
$\overline{CE}$ High during toggle bit polling	tCEPH	20	-	20	-	20	-	ns

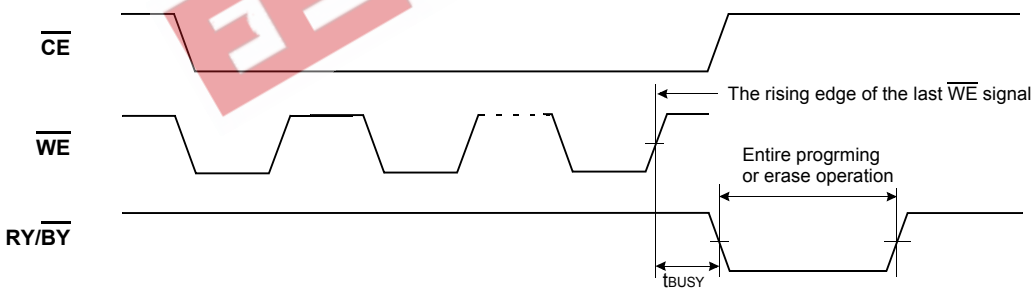
SWITCHING WAVEFORMS

Data Polling During Internal Routine Operation



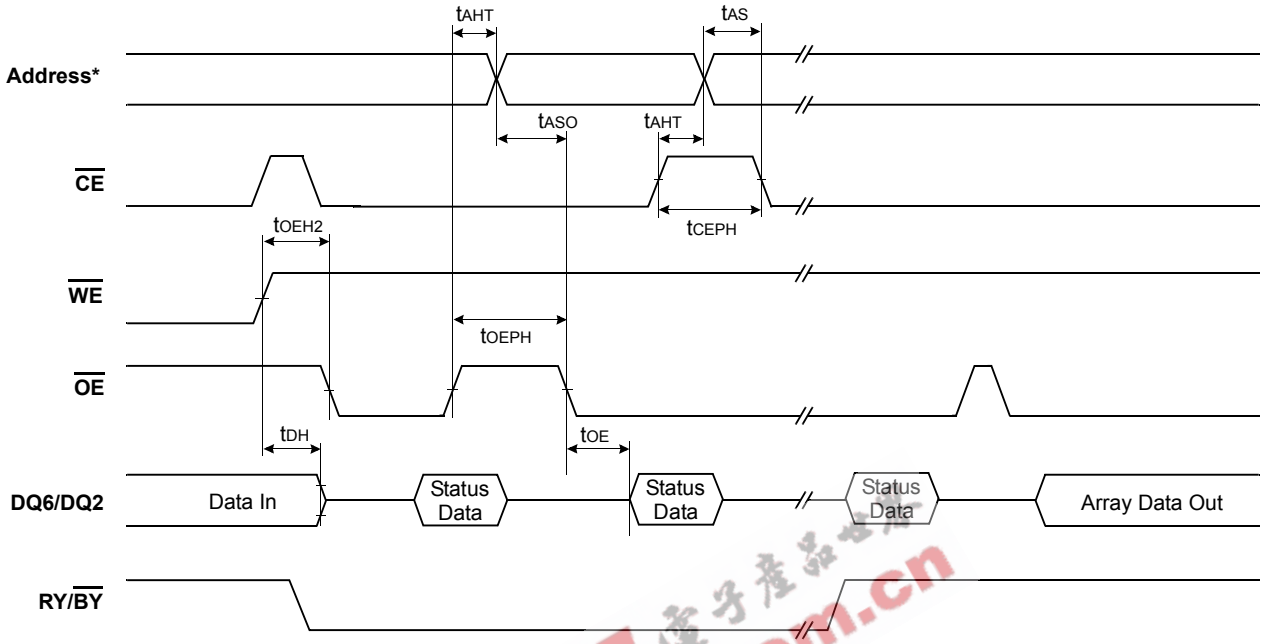
Note : *DQ7=Vaild Data (The device has completed the internal operation).

RY/BY Timing Diagram During Program/Erase Operation

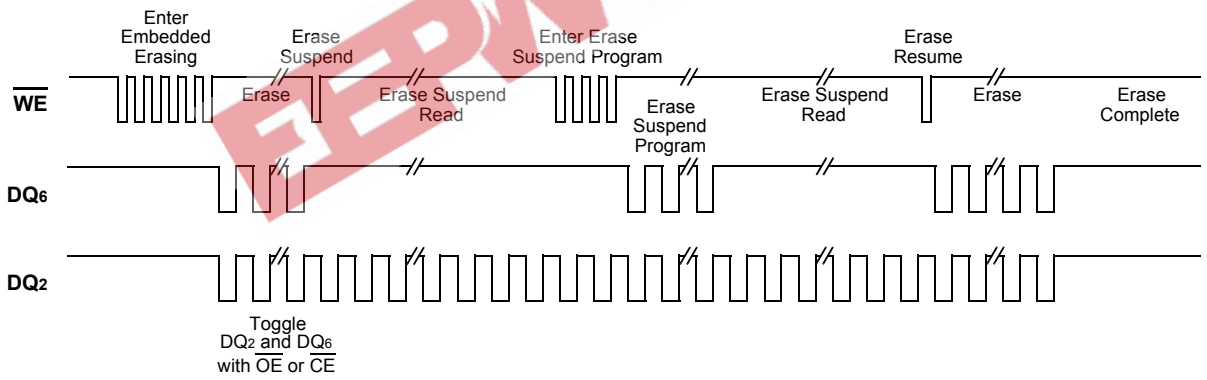


Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Program/Erase Valid to RY/BY Delay	tBUSY	90	-	90	-	90	-	ns
Chip Enable Access Time	tCE	-	70	-	80	-	90	ns
Output Enable Time	tOE	-	25	-	25	-	35	ns
CE & OE Disable Time	tDF	-	16	-	16	-	16	ns
Output Hold Time from Address, CE or OE	tOH	0	-	0	-	0	-	ns
OE Hold Time	tOEH2	10	-	10	-	10	-	ns

SWITCHING WAVEFORMS
Toggle Bit During Internal Routine Operation



Note : Address for the write operation must include a bank address (A19) where the data is written.

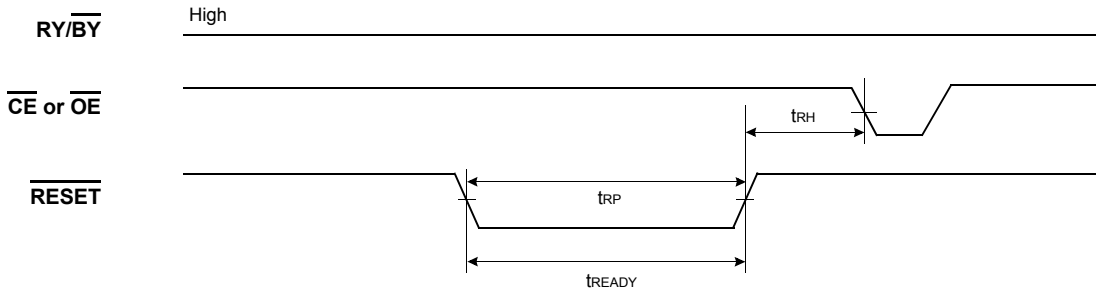


Note : DQ2 is read from the erase-suspended block.

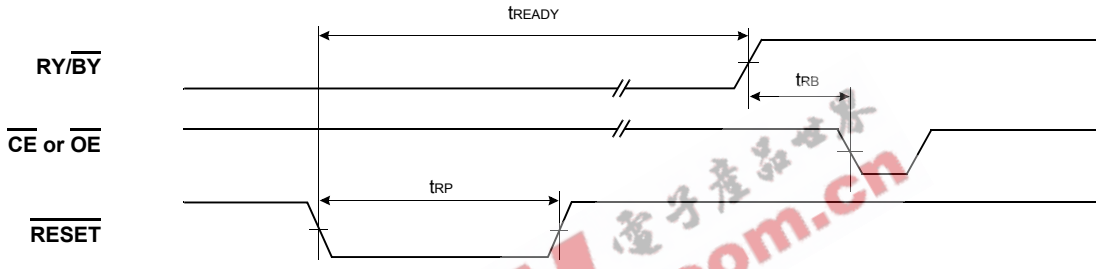
Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
Output Enable Access Time	tOE	-	25	-	25	-	35	ns
OE Hold Time	tOEH2	10	-	10	-	10	-	ns
Address Hold Time	tAHT	0	-	0	-	0	-	ns
Address Setup	tASO	55	-	55	-	55	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Data Hold Time	tDH	0	-	0	-	0	-	ns
CE High during toggle bit polling	tCEPH	20	-	20	-	20	-	ns
OE High during toggle bit polling	tOEPH	20	-	20	-	20	-	ns

SWITCHING WAVEFORMS

RESET Timing Diagram

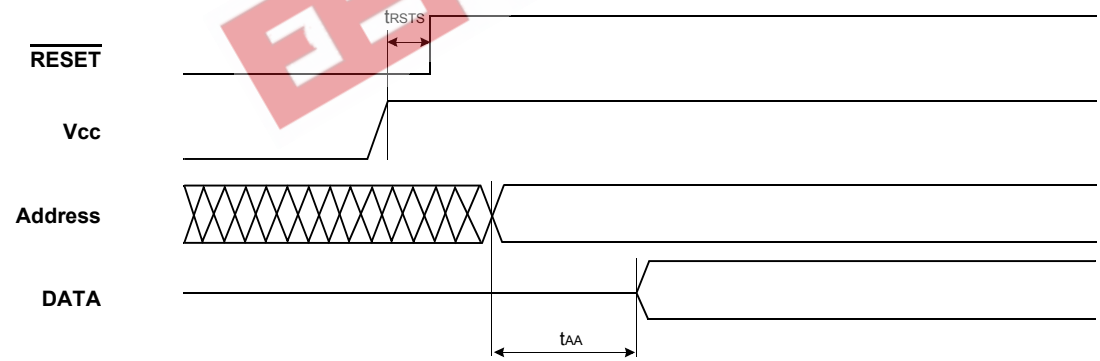


Reset Timings NOT during Internal Routine



Reset Timings during Internal Routine

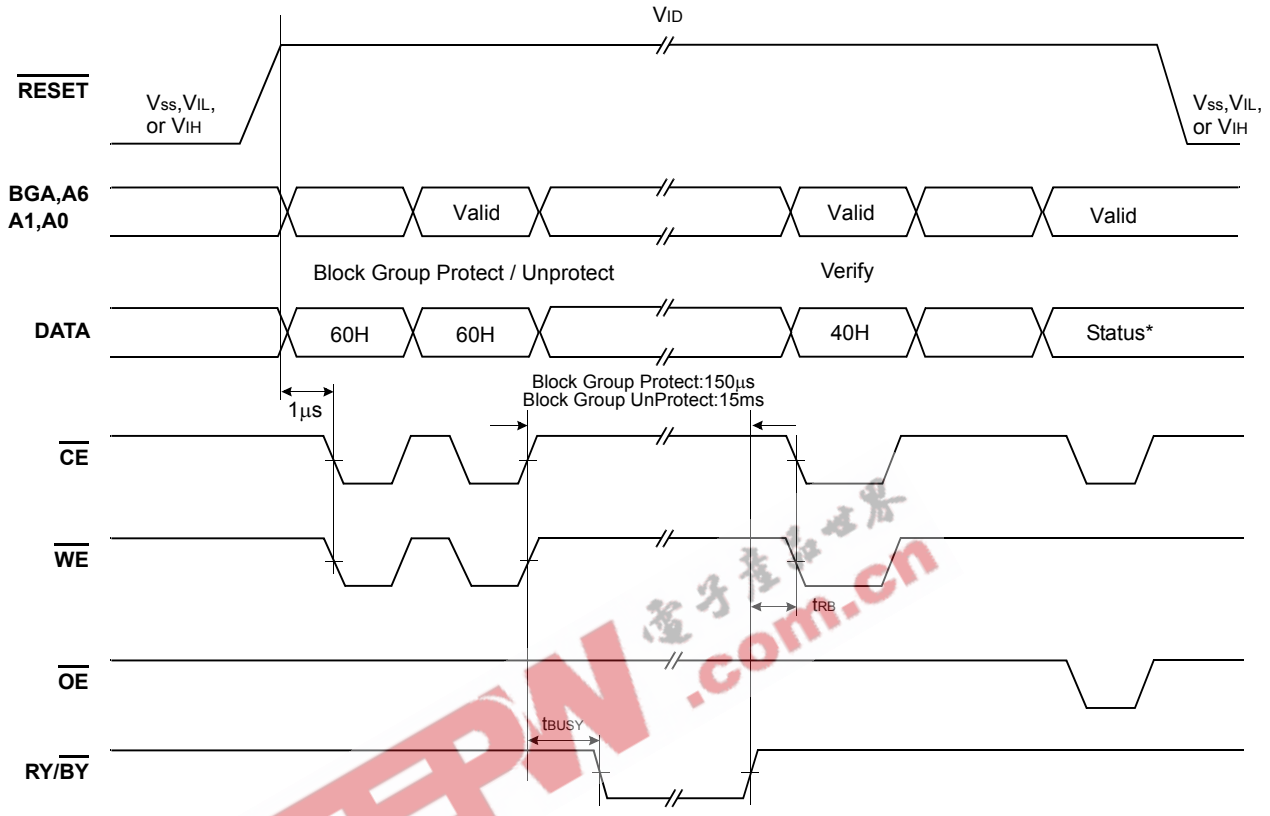
Power-up and RESET Timing Diagram



Parameter	Symbol	-7		-8		-9		Unit
		Min	Max	Min	Max	Min	Max	
RESET Pulse Width	tRP	500	-	500	-	500	-	ns
RESET Low to Valid Data (During Internal Routine)	tREADY	-	20	-	20	-	20	µs
RESET Low to Valid Data (Not during Internal Routine)	tREADY	-	500	-	500	-	500	ns
RESET High Time Before Read	tRH	50	-	50	-	50	-	ns
RY/BY Recovery Time	tRB	0	-	0	-	0	-	ns
RESET High to Address Valid	tRSTW	200	-	200	-	200	-	ns
RESET Low Set-up Time	tRSTS	500	-	500	-	500	-	ns

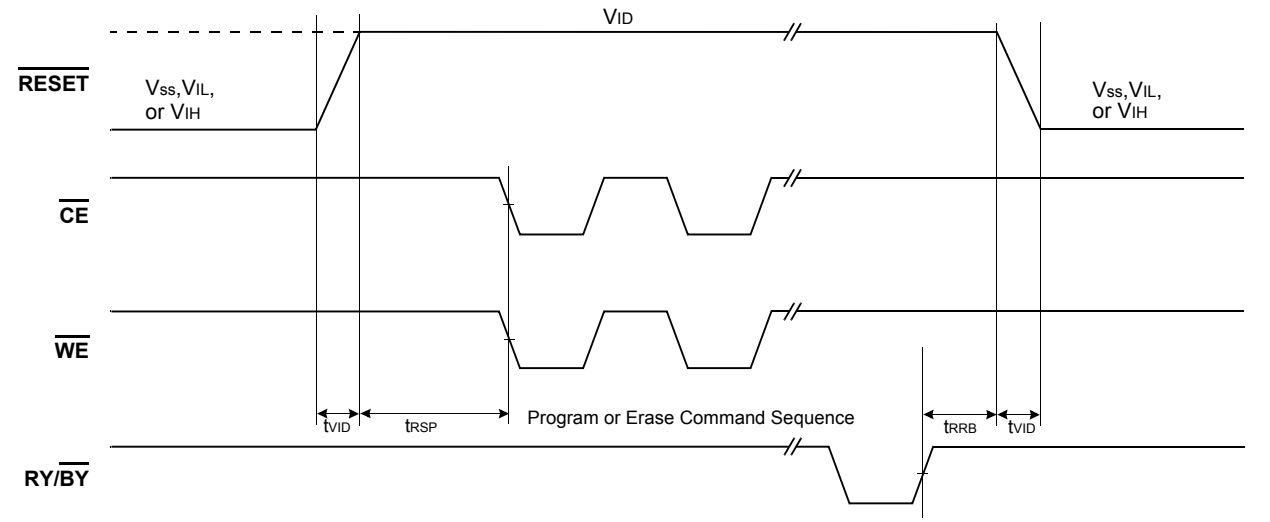
SWITCHING WAVEFORMS

Block Group Protect & Unprotect Operations



Notes : Block Group Protect (A6=V_{IL} , A1=V_{IH} , A0=V_{IL}) , Status=01H
Block Group Unprotect (A6=V_{IH} , A1=V_{IH}, A0=V_{IL}) , Status=00H
BGA = Block Group Address (A12 ~ A19)

Temporary Block Group Unprotect

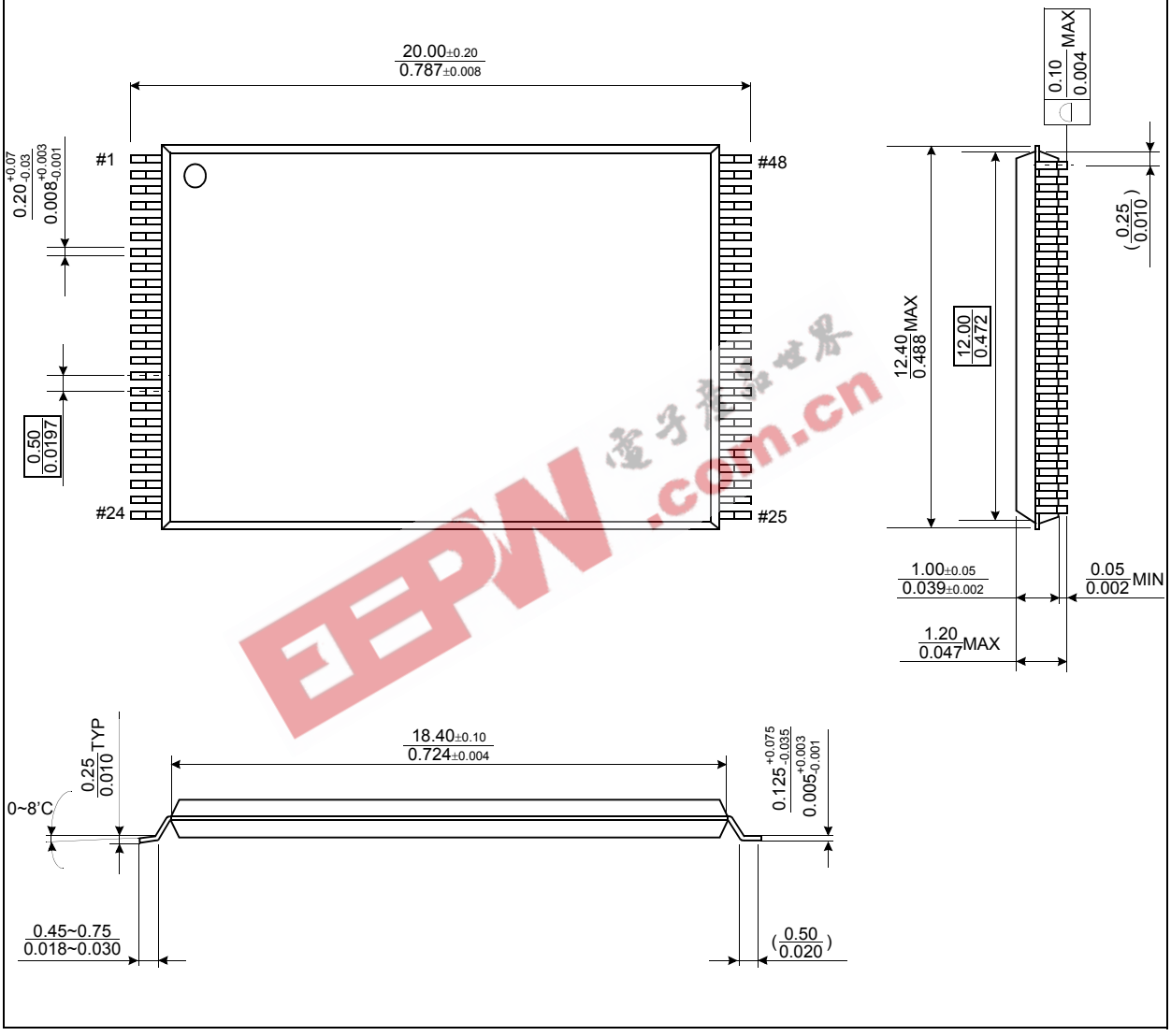


PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220F

Unit :mm/Inch



PACKAGE DIMENSIONS

48-Ball Fine Ball Grid Array Package (measured in millimeters)