

# KA3882E/KA3883E

## SMPS Controller

### Features

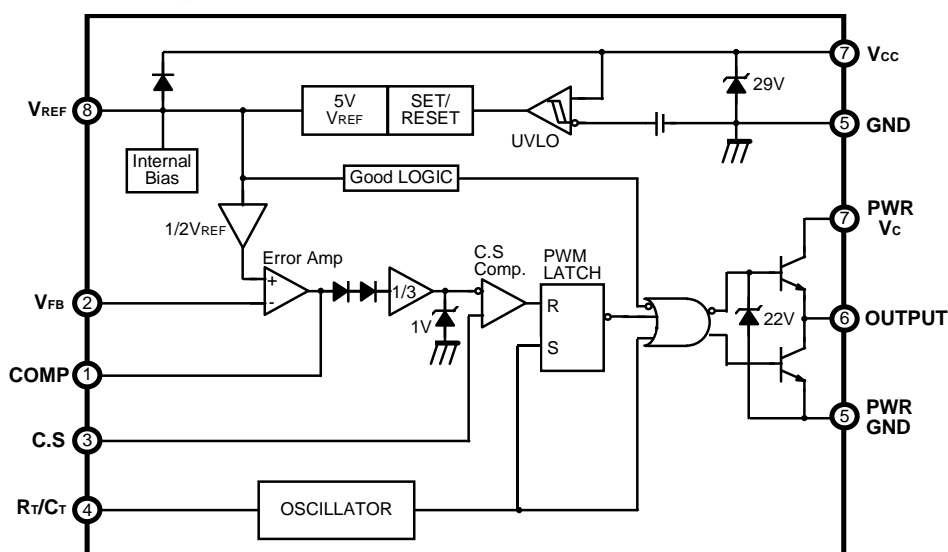
- Low start current 0.2mA (typ)
- Operating range up to 500kHz
- Cycle by cycle current limiting
- Under voltage lock out with hysteresis
- Short shutdown delay time: typ.100ns
- High current totem-pole output
- Output swing limiting: 22V

### Description

The KA3882E/KA3883E is a fixed PWM controller for Off-Line and DC to DC converter applications. The internal circuits include a UVLO, a low start-up current circuit, a temperature compensated reference, a high gain error amplifier, a current sensing comparator, and the high current totem-pole output for driving a POWER MOSFET. Also the KA3882E/KA3883E provides low start-up current below 0.3mA and short shutdown delay time typ. 100ns. The KA3882E has UVLO threshold of 16V(on) and 10V(off). The KA3883E is 8.4V(on) and 7.6V(off). The KA3882E and KA3883E can operate within 100% duty cycle.



### Internal Block Diagram



## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V <sub>CC</sub>	30	V
Output current	I <sub>O</sub>	+1	A
Analog inputs (pin2, 3)	V <sub>I(ANA)</sub>	-0.3 to 6.3	V
Error amp. output sink current	I <sub>SINK(EA)</sub>	10	mA
Power dissipation	P <sub>D</sub>	1	W
Thermal resistance, junction-to-air (Note4) 8-SOP 8-DIP	R <sub>θja</sub>	280 95	°C/W
Storage temperature	T <sub>stg</sub>	-65 ~ 150	°C

## Electrical Characteristics

(V<sub>CC</sub> = 15V, R<sub>T</sub> = 10kΩ, C<sub>T</sub> = 3.3nF, T<sub>A</sub> = 0°C to +70°C, Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>REFERENCE SECTION</b>						
Output voltage	V <sub>REF</sub>	T <sub>J</sub> = 25°C, I <sub>O</sub> = 1mA	4.9	5.0	5.1	V
Line regulation	R <sub>Line</sub>	V <sub>CC</sub> = 12V to 25V	-	6	20	mV
Load regulation	R <sub>LOAD</sub>	I <sub>O</sub> = 1mA to 20mA	-	6	25	mV
Output short circuit	I <sub>SC</sub>	T <sub>a</sub> = 25°C	-	-100	-180	mA
<b>OSILLATOR SECTION</b>						
Initial accuracy	F <sub>OSC</sub>	T <sub>J</sub> = 25°C	47	52	57	kHz
Voltage stability	ST <sub>V</sub>	V <sub>CC</sub> = 12V to 25V	-	0.2	1	%
Amplitude	V <sub>OSC</sub>	V <sub>PIN4</sub> , peak to peak	-	1.7	-	V
Discharge current	I <sub>DISCHG</sub>	T <sub>J</sub> = 25°C	7.8	8.3	8.8	mA
<b>CURRENT SENSE SECTION</b>						
Gain	G <sub>V</sub>	(Note2, 3)	2.85	3	3.15	V/V
Maximum input signal	V <sub>I(MAX)</sub>	V <sub>PIN1</sub> = 5V(Note2)	0.9	1.0	1.1	V
PSRR	PSRR	V <sub>CC</sub> = 12V to 25V (Note1, 2)	-	70	-	dB
Input bias current	I <sub>BIAS</sub>	V <sub>SENSE</sub> = 0V	-	-2	-10	uA
Delay to output	T <sub>D</sub>	V <sub>PIN3</sub> = 0 V to 2V (Note1)	-	100	200	ns

**Electrical Characteristics** (Continued)(V<sub>CC</sub> = 15V, R<sub>T</sub> = 10kΩ, C<sub>T</sub> = 3.3nF, T<sub>A</sub> = 0°C to +70°C, Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>ERROR AMPLIFIER SECTION</b>						
Input voltage	V <sub>I</sub>	V <sub>PIN1</sub> = 2.5V	2.42	2.50	2.58	V
Input bias current	I <sub>BIAS</sub>	V <sub>F</sub> B=0V	-	-0.3	- 2	μA
Open loop gain	G <sub>VO</sub>	V <sub>O</sub> = 2V to 4V (Note1)	65	90	-	dB
Unity gain bandwidth	GBW	T <sub>J</sub> = 25°C (Note1)	0.7	1	-	MHz
PSRR	PSRR	V <sub>CC</sub> = 12V to 25V (Note1)	60	70	-	dB
Output sink current	I <sub>SINK</sub>	V <sub>PIN2</sub> = 2.7V, V <sub>PIN1</sub> = 1.1V	2	6	-	mA
Output source current	I <sub>SOURCE</sub>	V <sub>PIN2</sub> = 2.3V, V <sub>PIN1</sub> = 5.0V	-0.5	-0.8	-	mA
Output high voltage	V <sub>OH</sub>	V <sub>PIN2</sub> = 2.3V, R <sub>1</sub> = 15kΩ to GND	5	6	-	V
Output low voltage	V <sub>OL</sub>	V <sub>PIN2</sub> = 2.7V, R <sub>1</sub> = 15kΩ to V <sub>ref</sub>	-	0.8	1.1	V
<b>OUTPUT SECTION</b>						
Output low level	V <sub>OL</sub>	I <sub>SINK</sub> = 20mA	-	0.1	0.4	V
		I <sub>SINK</sub> = 200mA	-	1.5	2.2	V
Output high level	V <sub>OH</sub>	I <sub>SOURCE</sub> = 20mA	13	13.5	-	V
		I <sub>SOURCE</sub> = 200mA	12	13.5	-	V
Rise time	t <sub>R</sub>	T <sub>J</sub> = 25°C, C <sub>1</sub> = 1nF (Note1)	-	40	100	ns
Fall time	t <sub>F</sub>	T <sub>J</sub> = 25°C, C <sub>1</sub> = 1nF (Note1)	-	40	100	ns
Output voltage swing limit	V <sub>OLIM</sub>	V <sub>CC</sub> = 27V, C <sub>1</sub> = 1nF	-	22	-	V
<b>UNDER VOLTAGE LOCKOUT SECTION</b>						
Start threshold	V <sub>TH</sub>	KA3882E	15	16	17	V
		KA3883E	7.8	8.4	9.0	V
Min. operating voltage ( after turn on )	V <sub>TL</sub>	KA3882E	9	10	11	V
		KA3883E	7.0	7.6	8.2	V
<b>PWM SECTION</b>						
Maximum duty cycle	D <sub>MAX</sub>	KA3882E/KA3883E	94	96	100	%
Minimum duty cycle	D <sub>MIN</sub>	-	-	-	0	%
<b>TOTAL STANDBY CURRENT</b>						
Start-up current	I <sub>ST</sub>	-	-	0.2	0.4	mA
Operating supply current	I <sub>CC</sub>	V <sub>PIN2</sub> = V <sub>PIN3</sub> = 0V	-	11	17	mA
V <sub>CC</sub> zener voltage	V <sub>Z</sub>	I <sub>CC</sub> = 25mA	-	29	-	V

\* Adjust V<sub>CC</sub> above the start threshold before setting at 15V**Notes :**

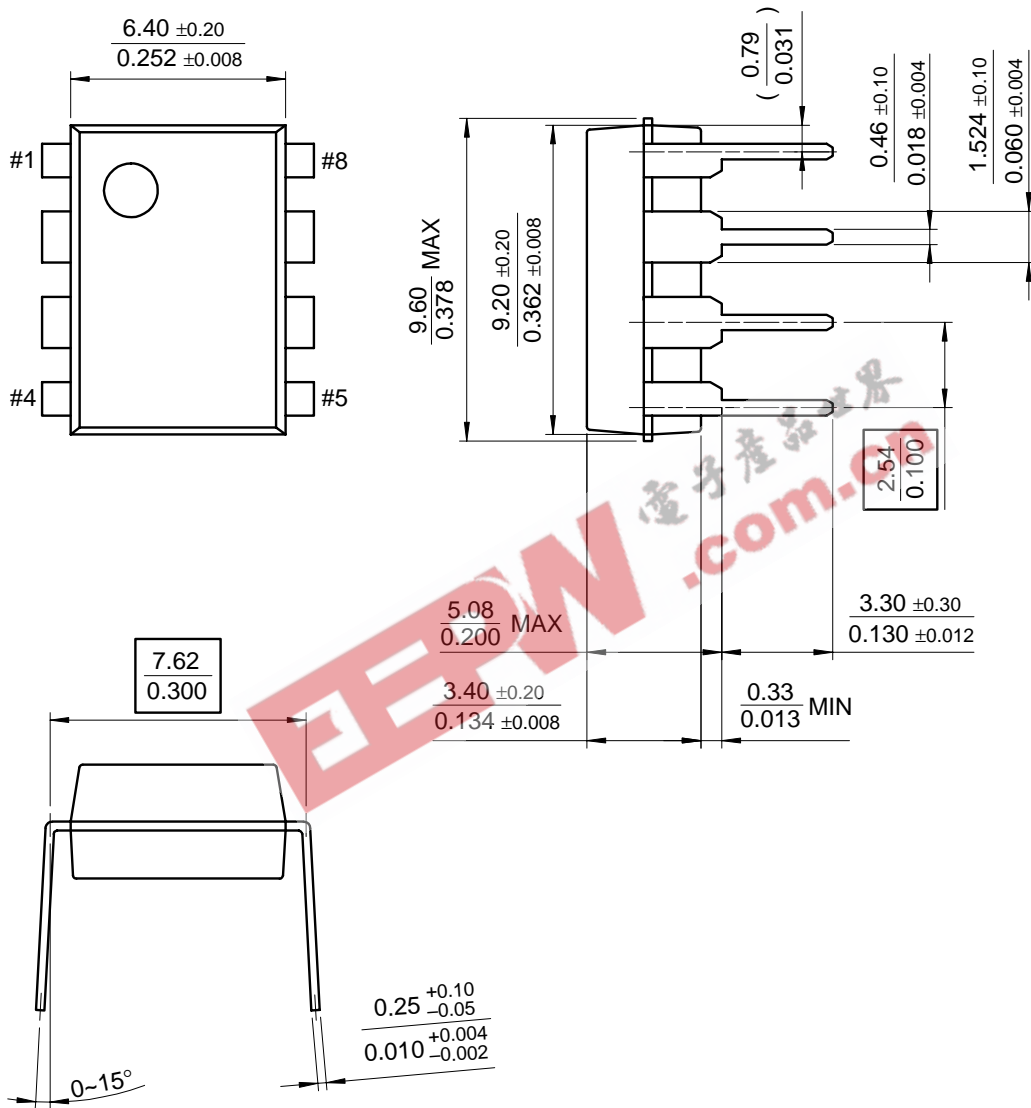
- These parameters, although guaranteed, are not 100% tested in production.
- Parameter measured at trip point of latch with V<sub>F</sub>B = 0V.
- Gain defined as:  $G_V = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$ ;  $0 \leq V_{SENSE} \leq 0.8V$
- Junction-to-air thermal resistance test environments.
  - PCB information ;  
Board thickness : 1.6mm , Board dimension : 76.2 X 114.3mm<sup>2</sup> , Ref. : EIA / JSED51-3 and EIA / JSED51-7
  - Board structure; Using the single layer PCB.

# Mechanical Dimensions

## Package

Dimensions in millimeters

### 8-DIP





## Ordering Information

Product Number	Package	Operating Temperature
KA3882E	8-DIP	0 ~ +70°C
KA3882ED	8-SOP	
KA3883E	8-DIP	
KA3883ED	8-SOP	

EEPW 电子产品世界  
.com.cn

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.