

Single-Chip Volume and Tone Control System



LC75341, 75341M

Overview

The LC75341 and LC75341M are electronic volume and tone control systems that provide volume, balance, a 2-band equalizer, and input switching functions that can be controlled from serially transferred data.

Functions

• Volume: 0 dB to -79 dB (in 1-dB steps) and $-\infty$, for a total of 81 settings.

The volume can be controlled independently in the left and right channels to implement a balance function.

- Bass boost: Up to +20 dB in 2-dB steps. Peaking characteristics.
- Treble: ±10 dB in 2-dB steps. Shelving characteristics.
- Selector: One of four sets of left/right inputs can be selected.
- Input gain: The input signal can be boosted by from 0 dB to +30 dB in 2-dB steps.

Features

- On-chip buffer amplifiers minimize the number of external components.
- Fabricated in a silicon gate CMOS process to minimize switching noise from internal switches.
- Built-in analog ground reference voltage generation circuit.
- All controls can be set from serially transferred data. Supports the CCB standard.

Package Dimensions

unit: mm

3067-DIP24S



unit: mm

3112-MFP24S



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Specifications

Absolute Maximum Ratings at Ta = 25°C, $V_{SS} = 0 V$

Parameter	Symbol	Pin	Cond	itions	Ratings	Unit
Maximum supply voltage	V _{DD} max	V _{DD}			11	V
Maximum input voltage	V _{IN} max	CE, DI, CL, L1 to L4, R1 to R4, LIN, RIN			V_{SS} – 0.3 to V_{DD} + 0.3	V
			Ta ≤ 75°C	LC75341	450	
Allowable power dissipation	Pdmax		Ta \leq 75°C with a PCB* LC75341M		450	mW
Operating temperature	Topr				-30 to +75	°C
Storage temperature	Tstg				-40 to +125	°C

Note: * Printed circuit board size: 76.1 × 114.3 × 1.6 mm, printed circuit board material: glass/epoxy resin

Allowable Operating Ranges at Ta = -30 to $+75^{\circ}$ C, V_{SS} = 0 V

Deremeter	Cumhal	Din	Conditions		Ratings		Linit
Parameter	Symbol	Pin	Conditions	min	typ	max	Offic
Supply voltage	V _{DD}	V _{DD}		5.0		10	V
High-level input voltage	VIH	CL, DI, CE		2.7		10	V
	V.		$7.5 \leq V_{DD} \leq 10.0$	V _{SS}		1.0	V
	۷IL		$5.0 \leq V_{DD} < 7.5$	Vss		0.8	v
Input voltage amplitude	V _{IN}	CE, DI, CL, L1 to L4, R1 to R4, LIN, RIN	-	V _{SS}		V_{DD}	Vp-р
Input pulse width	tøW	CL	3.15	1			μs
Setup time	tsetup	CL, DI, CE	3 S	1			μs
Hold time	thold	CL, DI, CE	2	1			μs
Operating frequency	fopg	CL	2			500	kHz

Electrical Characteristics at Ta = 25° C, V_{DD} = 9 V, V_{SS} = 0 V. Input Block

Parameter		Qumbol	Dia	Conditiono			Linit		
Faranielei		Symbol	- Fill	Conditions	min	typ	max	Offic	
Maximum input gain		Gin max				+30		dB	
Step resolution		Gstep				+2		dB	
Input resistance		Rin	L1, L2, L3, L4 R1, R2, R3, R4			50		kΩ	
Clipping level		Vcl	LSEL0, RSEL0	THD = 1.0%, f = 1 kHz		2.90		Vrms	
Output load resistance		RI	LSEL0, RSEL0		10			kΩ	

Volume Control Block

Deremeter	Sumbol	Din	Conditions		Linit		
Falameter	Symbol	FIII	Conditions	min	typ	max	
Input resistance	Rin	L _{IN} , R _{IN}			50		kΩ

Bass Band Equalizer Control Block

Paramotor	Symbol Din		Conditions		Linit		
Falanielei	Symbol	FIII	Conditions	min	typ	max	U.I.I.
Control range	Geq		max.boost	+18	+20	+22	dB
Step resolution	Estep			1	2	3	dB
Internal feedback resistance	Rfeed				66.6		kΩ

Treble Band Equalizer Control Block

Paramotor	Symbol Pin		Conditions		Linit		
Falanielei	Symbol	FIII	Conditions	min	typ	max	Onit
Control range	Geq		max.boost/cut	±8	±10	±12	dB
Step resolution	Estep			1	2	3	dB
Internal feedback resistance	Rfeed				51.7		kΩ

Overall Characteristics

Deremeter	Sumbol	Conditions			Linit		
Faranielei	Symbol	Conditions	min		max	Offic	
Total harmonic distortion	THD	V _{IN} = 1 Vrms, f = 1 kHz, all flat overall			0.01	%	
Crosstalk	СТ	V_{IN} = 1 Vrms, f = 1 kHz, Rg = 1 k Ω , all flat overall	80			dB	
Output noise voltage	V _N	All flat overall, 80 kHz, L.P.F		9.3		μV	
Maximum attenuation	Vomin	All flat overall, f = 1 kHz		-90		dB	
Current drain	I _{DD}	$V_{DD} - V_{SS} = +10 \text{ V}$		37		mA	
High-level input current	I _{IH}	CL, DI, CE: V _{IN} = 10 V			10	μA	
Low-level input current	I _{IL}	CL, DI, CE: V _{IN} = 0 V	-10			μA	

Pin Assignment



Equivalent Circuit



Control System Timing and Data Format

Applications control the LC75341 and LC75341M by applying the stipulated serial data to the CL, DI, and CE pins. This data consists of a total of 40 bits, of which 8 bits are the address and 32 bits are the data itself.



• Address code (B0 to A3)

The LC75341 and LC75341M have an 8-bit address code, and can be used together with other ICs that support the Sanyo CCB serial bus format.

Address code	B0	B1	B2	B3	A0	A1	A2	A3	
(LSB)	0	1	0	0	0	0	0	1	(82HEX)

• Control code allocation

Input switching control (L1, L2, L3, L4, R1, R2, R3, R4)

D0	D1	D2	D3	Operation
0	0	0	0	L1 (R1) ON
1	0	0	0	L2 (R2) ON
0	1	0	0	L3 (R3) ON
1	1	0	0	L4 (R4) ON
0	0	1	0	All switches off
1	0	1	0	All switches off
0	1	1	0	All switches off
1	1	1	0	All switches off

Input Gain Control

D4	D5	D6	D7	Operation
0	0	0	0	0 dB
1	0	0	0	+2 dB
0	1	0	0	+4 dB
1	1	0	0	+6 dB
0	0	1	0	+8 dB
1	0	1	0	+10 dB
0	1	1	0	+12 dB
1	1	1	0	+14 dB
0	0	0	1	+16 dB
1	0	0	1	+18 dB
0	1	0	1	+20 dB
1	1	0	1	+22 dB
0	0	1	1	+24 dB
1	0	1	1	+26 dB
0	1	1	1	+28 dB
1	1	1	1	+30 dB



Volume Control

D8	D9	D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	0	–1 dB
0	1	0	0	0	0	0	0	–2 dB
1	1	0	0	0	0	0	0	–3 dB
0	0	1	0	0	0	0	0	–4 dB
1	0	1	0	0	0	0	0	–5 dB
0	1	1	0	0	0	0	0	6 dB
1	1	1	0	0	0	0	0	-7 dB
0	0	0	1	0	0	0	0	-8 dB
1	0	0	1	0	0	0	0	-9 dB
0	1	0	1	0	0	0	0	-10 dB
1	1	0	1	0	0	0	0	–11 dB
0	0	1	1	0	0	0	0	-12 dB
1	0	1	1	0	0	0	0	-13 dB
0	1	1	1	0	0	0	0	-14 dB
1	1	1	1	0	0	0	0	-15 dB
0	0	0	0	1	0	0	0	-16 dB
1	0	0	0	1	0	0	0	-17 dB
0	1	0	0	1	0	0	0	-18 dB
1	1	0	0	1	0	0	0	-19 dB
0	0	1	0	1	0	0	0	-20 dB
1	0	1	0	1	0	0		-20 dB
0	1	1	0	1	0	0	0	-21 dB
1	1	1	0	1	0	0		-22 dB
0	0	0	1	1 2		0	0	-23 dB
1	0	0	1		0	0	0	-24 dB
0	1	0		1	0	0	0	-25 dB
1	1	0		1	0	0	0	-20 dB
0	0	1	1		0	0	0	-27 dB
1	0	1		1	0	0	0	-20 dB
0	1		1	1	0	0	0	-29 dB
1	1	1	1	1	0	0	0	-31 dB
0	0	0	0	0	1	0	0	-32 dB
1	0	0	0	0	1	0	0	-32 dB
0	1	0	0	0	1	0	0	-30 dB
1	1	0	0	0	1	0	0	_35 dB
0	0	1	0	0	1	0	0	_36 dB
1	0	1	0	0	1	0	0	_37 dB
0	1	1	0	0	1	0	0	_38 4B
1	1	1	0	0	1	0	0	_30 dB
0	0	0	1	0	1	0	0	_39 UD
1	0	0	1	0	1	0	0	-40 0B
1	0	0	1	0	1	0	0	-41 UB
0	1	0	1	0	1	0	0	-42 UB
1		1	1	0	1	0	0	-43 UD
U	0			0	1	0	0	-44 0B
1	0		1	U	1	0	0	-45 GB
U	1		1	U	1	0	0	-40 0B
1	1	1	1	U	1	U	U	-47 dB
0	0		U	1	1	0	U	-48 dB
1	0	0	U	1	1	U	U	-49 aB
0	1	0	0	1	1	0	0	–50 dB

Volume Control

D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	1	0	0	1	1	0	0	–51 dB
0	0	1	0	1	1	0	0	–52 dB
1	0	1	0	1	1	0	0	–53 dB
0	1	1	0	1	1	0	0	–54 dB
1	1	1	0	1	1	0	0	–55 dB
0	0	0	1	1	1	0	0	–56 dB
1	0	0	1	1	1	0	0	–57 dB
0	1	0	1	1	1	0	0	–58 dB
1	1	0	1	1	1	0	0	–59 dB
0	0	1	1	1	1	0	0	–60 dB
1	0	1	1	1	1	0	0	–61 dB
0	1	1	1	1	1	0	0	–62 dB
1	1	1	1	1	1	0	0	–63 dB
0	0	0	0	0	0	1	0	–64 dB
1	0	0	0	0	0	1	0	–65 dB
0	1	0	0	0	0	1	0	–66 dB
1	1	0	0	0	0	1	0	–67 dB
0	0	1	0	0	0	1	0	–68 dB
1	0	1	0	0	0	1	0	–69 dB
0	1	1	0	0	0	1	0	–70 dB
1	1	1	0	0	0	1	0	–71 dB
0	0	0	1	0	0	1	0	–72 dB
1	0	0	1	0	0 引	a (1	0	–73 dB
0	1	0	1	0	0	۳ 1	0	-74 dB
1	1	0	1	0	0	1	0	–75 dB
0	0	1	1	0	0	1	0	–76 dB
1	0	1	_ 1	0	0	1	0	–77 dB
0	1	1	1	0	0	1	0	–78 dB
1	1	1	1	0	0	1	0	–79 dB
0	0	0	0	1	0	1	0	–∞ dB

Treble Control

D16	D17	D18	D19	Operation
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	4 dB
1	1	0	1	6 dB
0	0	1	1	–8 dB
1	0	1	1	–10 dB

Bass Control

D20	D21	D22	D23	D24	D25	Operation
0	1	0	1	0	0	+20 dB
1	0	0	1	0	0	+18 dB
0	0	0	1	0	0	+16 dB
1	1	1	0	0	0	+14 dB
0	1	1	0	0	0	+12 dB
1	0	1	0	0	0	+10 dB
0	0	1	0	0	0	+8 dB
1	1	0	0	0	0	+6 dB
0	1	0	0	0	0	+4 dB
1	0	1	0	0	0	+2 dB
0	0	0	0	0	0	0 dB

Channel Selection

D26	D27	Operation	
0	0		
1	0	RCH	
0	1	LCH	
1	1	Left and right together	

Test Mode



Pin Functions

Pin No.	Pin	Description	Notes
40			
12	LI		
11	L2		
10	L3		k t
9	L4	Input signal connections	VDD + 🖂
13	R1		s S S S S S S S S S S S S S S S S S S S
14	R2		Ln I B SELO
15	R3		
16	R4		
			Rn \blacksquare
			• vrei ///
8	LSEL0		///
17	RSFI 0	Input selector outputs	
	NOLLO		
			VDD
			o VDD
5	LBASS	• Connections for the resistors and canacitors that form the bass hand	
20	RBASS	filters.	
20			
		3, 19, 1	777
		1 St 1	<u> </u>
		3 T* _ C	
			VDD
			Ŷ Ĺ _{RSI}
4	LOUT	• These pins are used both as the connections for the resistors and	BASS 🛓 🏾 🛓
21	ROUT	capacitors that form the bass band filters and as the outputs from the	
21		bass/treble circuits.	▲
			///
			VDD
			עעי
6	LTRE		
19	RTRF	Connections for the capacitors that form the treble band filters.	
10	ittine_		
			<i></i>
			UDD
			עעי א
			▲
7	LIN	• Volume control and equalizer input	W••••
18	RIN		
			≶ <u></u>
			///
			ץ VDD
		analog signal ground.	
22	Vref	Applications must connect a capacitor of about 10 uE between this pin	
		and V_{SS} to exclude power supply ripple.	
			│
			Vref 777
L			

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Pin No.	Pin	Description	Notes
3	V _{SS}	• Ground	
23	V _{DD}	Power supply	
2	CE	 Chip enable Data is written to the internal latch when this pin goes from high to low. The internal analog switches operate at this point. Data transfer is enabled when this pin is high. 	VDD Z
1 24	DI CL	Serial data and clock inputs used for IC control.	↓T 777

Internal Equivalent Circuits

• Selector block equivalent circuit



• Treble and bass band block internal equivalent circuit



Set switches SW1 and SW3 to the on position for boost, and set switches SW2 and SW4 to the on position for cut. For a flat (0 dB) response, set the 0dBSW, SW2, and SW3 switches on.

• Volume block internal equivalent circuit



Test Circuits

• Total harmonic distortion



Units (resistance: Ω , capacitnace: F)

• Output noise voltage



• Crosstalk



Bass Band Circuit

This section presents the equivalent circuit and the calculations for the external capacitors and resistors used to achieve a center frequency of 100 Hz.

· Bass band equivalent circuit



• Sample calculation

Specifications Center frequency: f0 = 100 HzGain at maximum boost: G = 20 dB Let R1 = 0, $R2 = 66.6 \text{ K}\Omega$, and C1 = C2 = C. ·Com.cn

(1) Determine R2 from the fact that G = 20 dB.

$$G_{+20\text{dB}} = 20 \times LOG_{10} \left(1 + \frac{R^2}{2R^3}\right)$$
$$R3 = \frac{R^2}{2 \left(10^{G+20\text{dB}/20} - 1\right)} = \frac{66000}{2 \times (10 - 1)} \neq 3.7 \, k\Omega$$

(2) Determine C from the fact that the center frequency f0 = 100 Hz.

$$f0 = \frac{1}{2\pi\sqrt{R3R2C1C2}}$$

$$C = \frac{1}{2\pi f \, 0 \sqrt{R3R2}} = \frac{1}{2\pi \times 100 \sqrt{66000 \times 3700}} \neq 0.1 \, \mu F$$

(3) Determine Q.

$$Q = \frac{R3R2}{2R3} \bullet \frac{1}{\sqrt{R3R2}} \neq 2.1$$

• Treble band circuit

The treble band circuit provides shelving characteristics.

This section presents the equivalent circuit in boost mode and the formulas used to calculate the external component values.



• Sample calculation Specifications - Set frequency: f = 26,000 Hz Gain at maximum boost: $G_{+10dB} = 10$ dB Let R1 = 16.240 k Ω , R2 = 35.461 K Ω ,

Substitute the above constants into the following formulas.

$$G = 20 \times LOG_{10} \left(1 + \frac{R2}{\sqrt{R1^2 + (1 / \omega C)^2}} \right)$$
$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{G/20} - 1}\right) - R1^2}}$$
$$= \frac{1}{2\pi 26000 \sqrt{\left(\frac{35461}{3.16 - 1}\right)^2 - 16240^2}} \neq 2700 \ (pF)$$

Usage Notes

- When power is first applied, the states of the internal analog switches will be undefined. Applications must provide external muting until the control data has been transferred and the switches set to appropriate states.
- Applications should transfer both the left and right channel initial settings data before releasing the muting function when initializing this IC after first applying power.
- Applications should cover the CL, DI, and CE pin lines with the ground pattern, or should use shielded cables for these lines to prevent the high-frequency digital signals transmitted over these lines from entering analog signal system.
- When the oscillation occurs, connect a resistor of at least 200 Ω to LOUT and ROUT pins.

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