Ordering number : EN2663A

CMOS LSI

SANYO No.2663A

LC7936A, 7936B

32-Bit PPC LED Erasing Head Driver

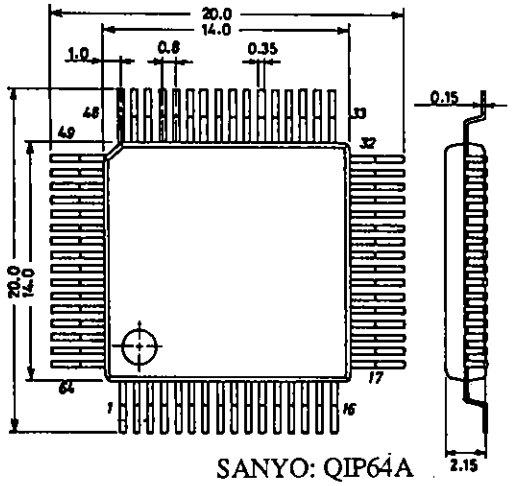
Features

- High-speed, high-voltage silicon gate CMOS device
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock signal (CLOCK).
- 32-bit latch data is changed on the negative transition of the $\overline{\text{LATCH}}$ pad signal and is held on the positive transition.
- The $\overline{\text{STROBE}}$ pad signal, BEO pad signal can be used to exercise on/off control of the output driver.
- All output drivers can be turned on by setting 32-bit latch regardless of shift register data. (TEST=Hi, $\overline{\text{STROBE}}$=Lo, BEO=Hi)
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads)
- Maximum ratings of driver output: V_O=15V, I_{OL}=30mA
- Logic unit operating voltage: V_{DD}=4.5V to 5.5V

Absolute Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{DD}		-0.3 to +7.0	V
Input Voltage	V_I		-0.3 to V_{DD}+0.3	V
Output Voltage	V_O (1)	S_{OUT} output	-0.3 to V_{DD}+0.3	V
	V_O (2)	D1 to D32 output Output Tr off	15	V
Output Circuit	I_O	D1 to D32 output, per output	30	mA
Allowable Power Dissipation	Pd max	QIP-64 package at 70°C	450	mW
Operating Temperature	Topr	QIP-64 package	0 to +70	°C
Storage Temperature	Tstg	QIP-64 package	-35 to +125	°C

Package Dimensions 3057-Q64AIC
(unit: mm)
LC7936A



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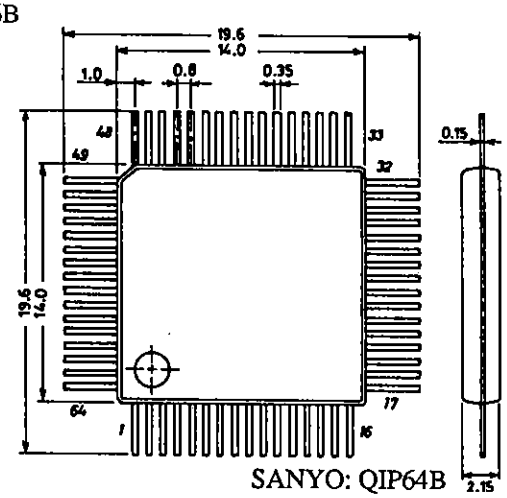
Package Dimensions 3026B-Q64BIC
(unit: mm)
LC7936B



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Allowable Operating Conditions at Ta=0 to +70°C

		Pin Name	min	typ	max	unit
Supply Voltage	V_{DD}	V_{DD}	4.5		5.5	V
"H"-Level Input Voltage	V_{IH}	S_{IN}, CLOCK, $\overline{LATCH}$ BEO, $\overline{STROBE}$, LED-check (TEST)	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	V_{IL}	S_{IN}, CLOCK, $\overline{LATCH}$, BEO, $\overline{STROBE}$, LED-check (TEST)	V_{SS} (L)		0.2V_{DD}	V
Clock Frequency	f_{CLK}	CLOCK Duty: 50%			5.0	MHz
Clock Pulse Width	$t_{W\phi}$	CLOCK	75			ns
Clock Rise/Fall Time	t_r, t_f	CLOCK			200	ns
Data Setup Time	t_{DS}	S_{IN}, CLOCK	100			ns
Data Hold Time	t_{DH}	S_{IN}, CLOCK	50			ns
Latch Pulse Width	t_{WL}	$\overline{LATCH}$	100			ns

Electrical Characteristics at Ta=25°C

		Pin Name		min	typ	max	unit
"H"-Level Input Current	I_{IH} (1)	S_{IN}, CLOCK $\overline{LATCH}$				10	μA
"H"-Level Input Current	I_{IH} (2)	BEO, LED-check (TEST)		12		72	μA
"L"-Level Input Current	I_{IL} (1)	S_{IN}, CLOCK $\overline{LATCH}$		-10			μA
"L"-Level Input Current	I_{IL} (2)	$\overline{STROBE}$		-72		-12	μA
"H"-Level Output Voltage	V_{OH}	S_{OUT}	V_{DD}=5V, I_{OH}=-0.5mA	V_{DD}-0.5			V
"L"-Level Output Voltage	V_{OL} (1)	S_{OUT}	V_{DD}=5V, I_{OL}=0.5mA			0.5	V
"L"-Level Output Voltage	V_{OL} (2)	D1 to D32	V_{DD}=5V, I_{OL}=30 mA			0.5	V
Output Off-State Leakage Current	I_{OFF}	D1 to D32	V_O=15V			20	μA
Input Capacitance	C_{IN}		CLOCK		5.0		pF
Operating Current Dissipation	I_{DD}	V_{DD}	V_{DD}=5V, f_{CLK}=5MHz, all outputs: no load			5	mA

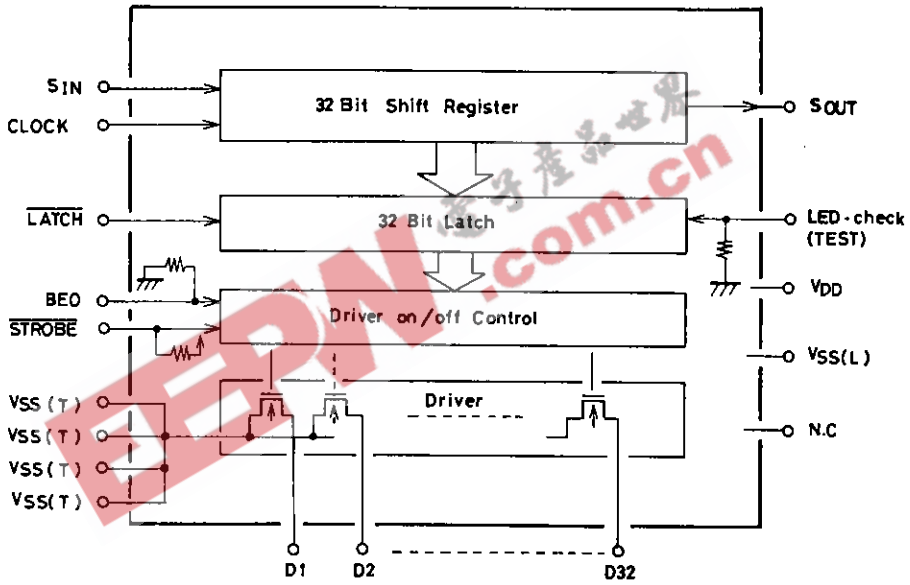
Switching Characteristics at Ta=25°C

		Pin Name		min	typ	max	unit
Clock Latch Delay Width	t_{CL}	CLOCK, $\overline{LATCH}$	V_{DD}=5V	100			ns
Latch Clock Delay Width	t_{LC}	CLOCK, $\overline{LATCH}$	V_{DD}=5V	0			ns
"H"-Level Output Propagation Delay Time	t_{PLH} (1)	$\overline{LATCH}$, D1 to D32	V_{DD}=5V, Dn: R_L=1.0kΩ CL=15pF			400	ns
	t_{PLH} (2)	BEO, $\overline{STROBE}$	V_{DD}=5V, Dn: R_L=1.0kΩ CL=15pF			300	ns
	t_{PLH} (3)	CLOCK, S_{OUT}	V_{DD}=5V, S_{OUT}: C_L=15pF			200	ns
"L"-Level Output Propagation Delay Time	t_{PHL} (1)	$\overline{LATCH}$, D1 to D32	V_{DD}=5V, Dn: R_L=1.0kΩ C_L=15pF			200	ns
	t_{PHL} (2)	BEO, $\overline{STROBE}$ D1 to D32	V_{DD}=5V, Dn: R_L=1.0kΩ C_L=15pF			100	ns
	t_{PHL} (3)	CLOCK, S_{OUT}	V_{DD}=5V, S_{OUT}: C_L=15pF			200	ns

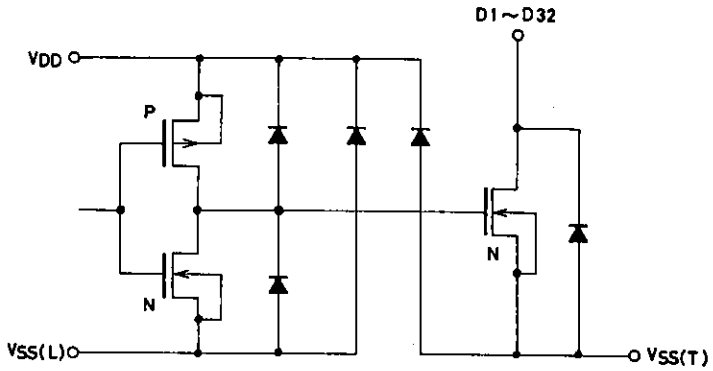
LED Driver On/Off Truth Table

Latch Data (Q)	BEO	$\overline{\text{STROBE}}$	LED Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON LED on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

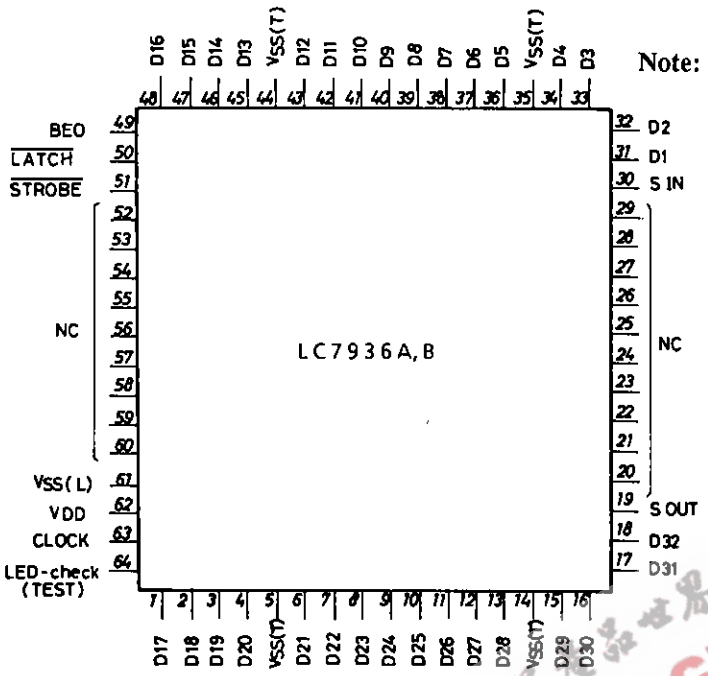
Equivalent Circuit Block Diagram



Output Driver Section Equivalent Circuit

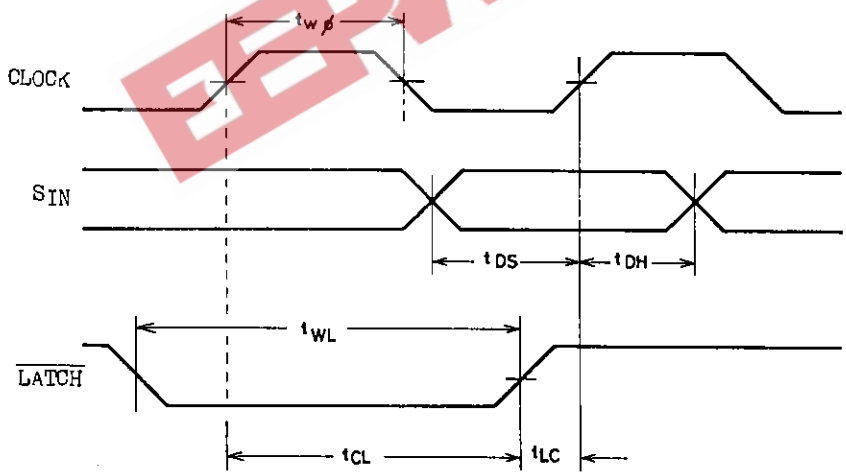


Pin Assignment



Note: Pins 24, 25 of NC pins are connected to the substrate (=V_{DD}) and must be kept open. Other NC pins must be also kept open. When the LED-check (TEST) pin is not in use, it must not be kept open, but must be connected to GND.

Input Data Timing Chart



Output Data Timing Chart