

SANYO

No.2663A

LC7936A, 7936B**32-Bit PPC LED Erasing Head Driver****Features**

- High-speed, high-voltage silicon gate CMOS device
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock signal (CLOCK).
- 32-bit latch data is changed on the negative transition of the LATCH pad signal and is held on the positive transition.
- The STROBE pad signal, BEO pad signal can be used to exercise on/off control of the output driver.
- All output drivers can be turned on by setting 32-bit latch regardless of shift register data. (TEST=Hi, STROBE=Lo, BEO=Hi)
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads)
- Maximum ratings of driver output: $V_O=15V$, $I_{OL}=30mA$
- Logic unit operating voltage: $V_{DD}=4.5V$ to $5.5V$

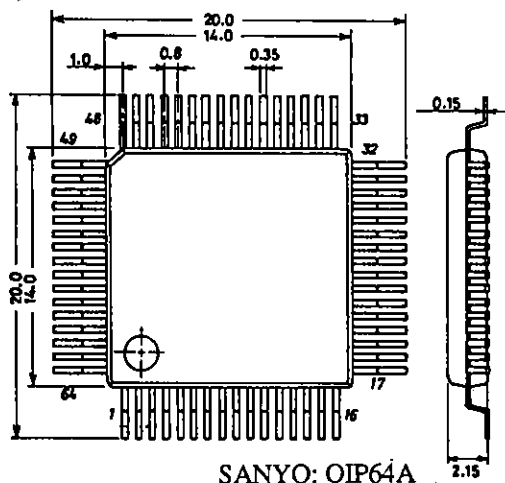
Absolute Maximum Ratings at $T_a=25^\circ C$

			unit
Maximum Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to $V_{DD}+0.3$	V
Output Voltage	V_O (1)	S_{OUT} output	-0.3 to $V_{DD}+0.3$ V
	V_O (2)	D1 to D32 output	15 V
Output Circuit	I_O	Output Tr off	
		D1 to D32 output, per output	30 mA
Allowable Power Dissipation	P_d max	QIP-64 package at $70^\circ C$	450 mW
Operating Temperature	T_{opr}	QIP-64 package	0 to +70 $^\circ C$
Storage Temperature	T_{stg}	QIP-64 package	-35 to +125 $^\circ C$

Package Dimensions 3057-Q64AIC

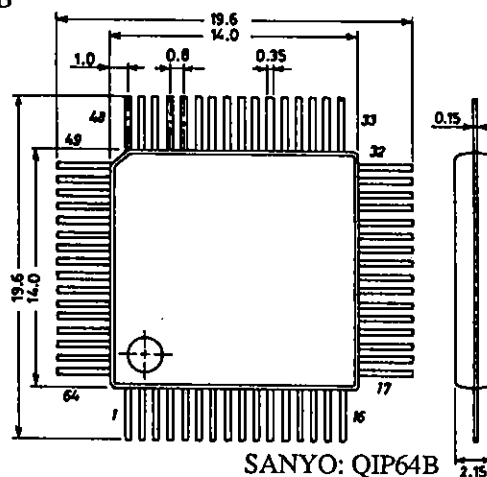
(unit: mm)

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**Package Dimensions 3026B-Q64BIC**

(unit: mm)

LC7936B



Allowable Operating Conditions at Ta=0 to +70°C

		Pin Name	min	typ	max	unit
Supply Voltage	V _{DD}	V _{DD}	4.5		5.5	V
"H"-Level Input Voltage	V _{IH}	S _{IN} , CLOCK, $\overline{\text{LATCH}}$ BEO, $\overline{\text{STROBE}}$, LED-check (TEST)	0.8V _{DD}		V _{DD}	V
"L"-Level Input Voltage	V _{IL}	S _{IN} , CLOCK, $\overline{\text{LATCH}}$, BEO, $\overline{\text{STROBE}}$, LED-check (TEST)	V _{SS} (L)		0.2V _{DD}	V
Clock Frequency	f _{CLK}	CLOCK Duty: 50%			5.0	MHz
Clock Pulse Width	t _w	CLOCK	75			ns
Clock Rise/Fall Time	t _r , t _f	CLOCK			200	ns
Data Setup Time	t _{DS}	S _{IN} , CLOCK	100			ns
Data Hold Time	t _{DH}	S _{IN} , CLOCK	50			ns
Latch Pulse Width	t _{wL}	$\overline{\text{LATCH}}$	100			ns

Electrical Characteristics at Ta=25°C

		Pin Name	min	typ	max	unit
"H"-Level Input Current	I _{IH} (1)	S _{IN} , CLOCK $\overline{\text{LATCH}}$			10	μA
"H"-Level Input Current	I _{IH} (2)	BEO, LED-check (TEST)	12		72	μA
"L"-Level Input Current	I _{IL} (1)	S _{IN} , CLOCK $\overline{\text{LATCH}}$	-10			μA
"L"-Level Input Current	I _{IL} (2)	$\overline{\text{STROBE}}$	-72		-12	μA
"H"-Level Output Voltage	V _{OH}	S _{OUT}	V _{DD} =5V, I _{OH} =-0.5mA	V _{DD} -0.5		V
"L"-Level Output Voltage	V _{OL} (1)	S _{OUT}	V _{DD} =5V, I _{OL} =0.5mA		0.5	V
"L"-Level Output Voltage	V _{OL} (2)	D1 to D32	V _{DD} =5V, I _{OL} =30 mA		0.5	V
Output Off-State Leakage Current	I _{OFF}	D1 to D32	V _O =15V		20	μA
Input Capacitance	C _{IN}	CLOCK		5.0		pF
Operating Current Dissipation	I _{DD}	V _{DD}	V _{DD} =5V, f _{CLK} =5MHz, all outputs: no load		5	mA

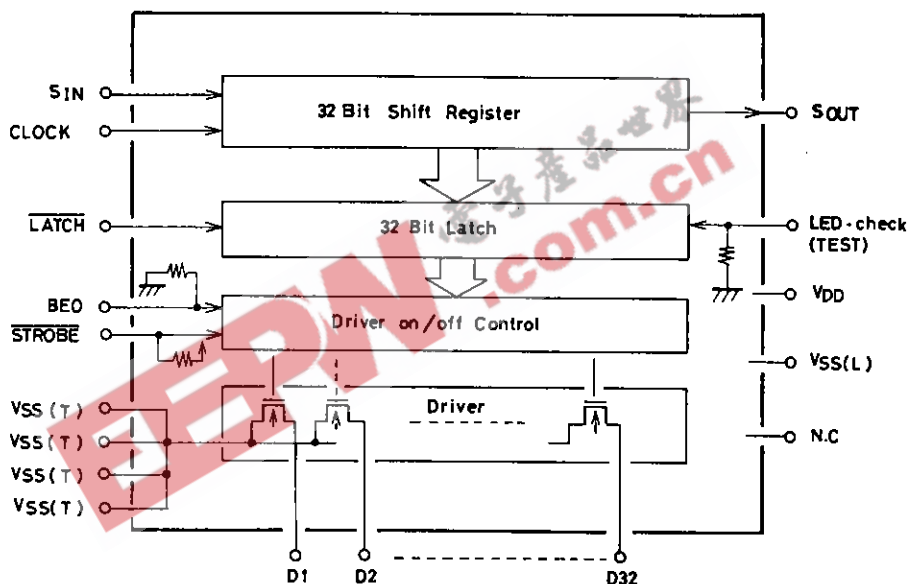
Switching Characteristics at Ta=25°C

		Pin Name	min	typ	max	unit
Clock Latch Delay Width	t _{CL}	CLOCK, $\overline{\text{LATCH}}$	V _{DD} =5V	100		ns
Latch Clock Delay Width	t _{LC}	CLOCK, $\overline{\text{LATCH}}$	V _{DD} =5V	0		ns
"H"-Level Output Propagation Delay Time	t _{PLH} (1)	$\overline{\text{LATCH}}$, D1 to D32	V _{DD} =5V, Dn: R _L =1.0kΩ CL=15pF		400	ns
	t _{PLH} (2)	BEO, $\overline{\text{STROBE}}$	V _{DD} =5V, Dn: R _L =1.0kΩ CL=15pF		300	ns
	t _{PLH} (3)	CLOCK, S _{OUT}	V _{DD} =5V, S _{OUT} : C _L =15pF		200	ns
"L"-Level Output Propagation Delay Time	t _{PHL} (1)	$\overline{\text{LATCH}}$, D1 to D32	V _{DD} =5V, Dn: R _L =1.0kΩ C _L =15pF		200	ns
	t _{PHL} (2)	BEO, $\overline{\text{STROBE}}$ D1 to D32	V _{DD} =5V, Dn: R _L =1.0kΩ C _L =15pF		100	ns
	t _{PHL} (3)	CLOCK, S _{OUT}	V _{DD} =5V, S _{OUT} : C _L =15pF		200	ns

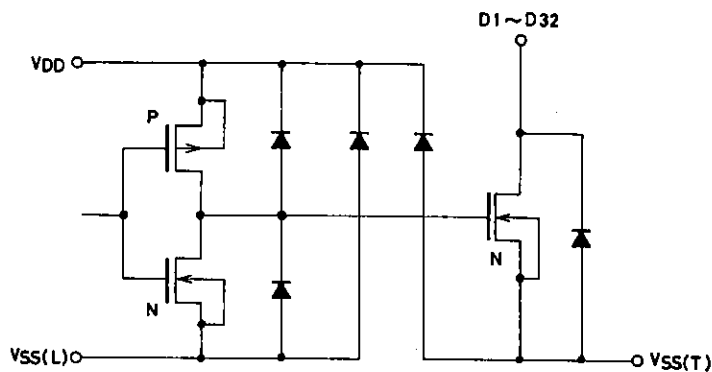
LED Driver On/Off Truth Table

Latch Data (Q)	BEO	$\overline{\text{STROBE}}$	LED Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON LED on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

Equivalent Circuit Block Diagram

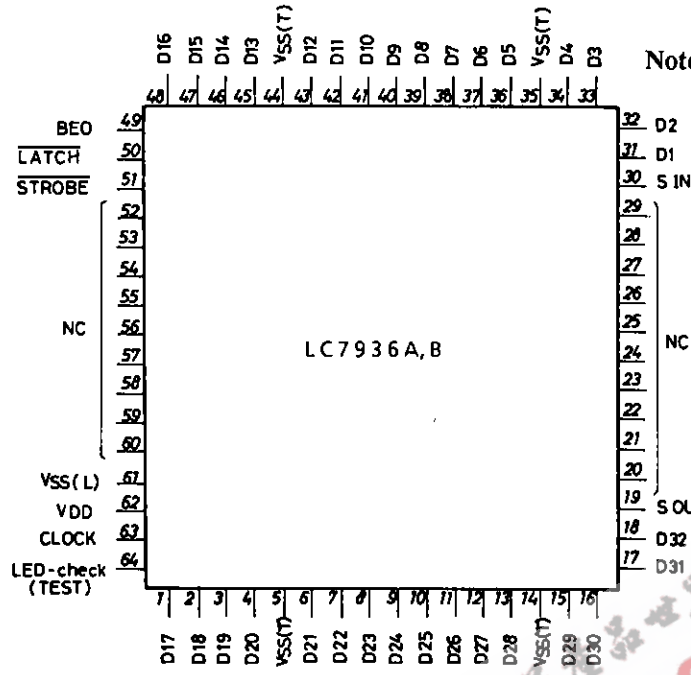


Output Driver Section Equivalent Circuit



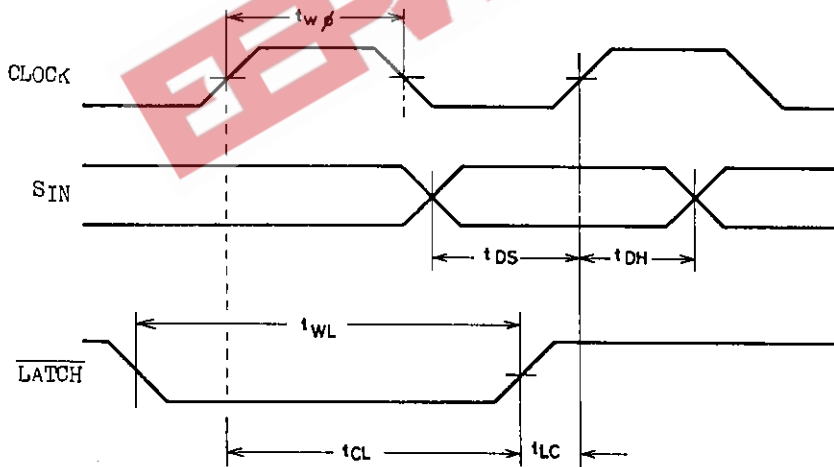
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Pin Assignment

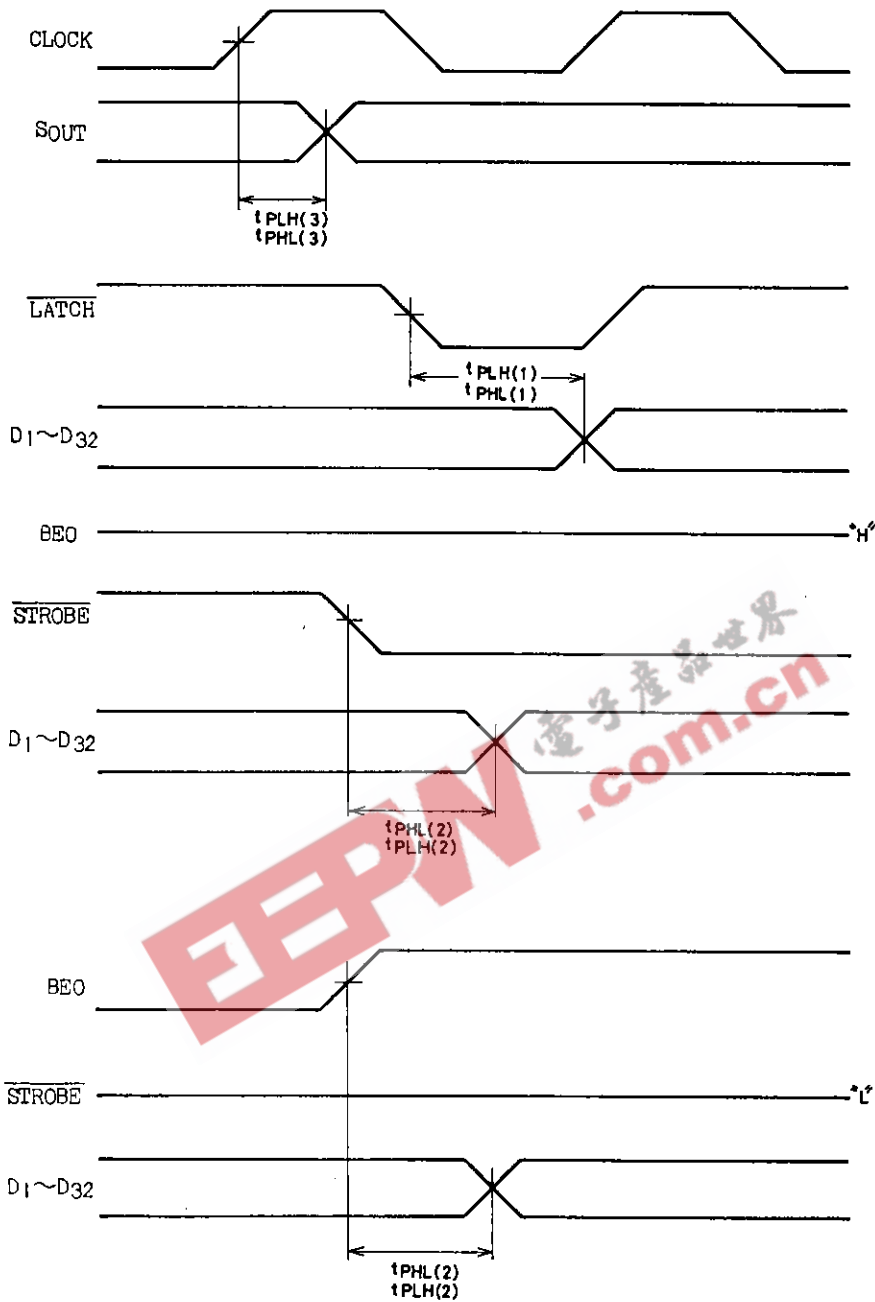


Note: Pins 24, 25 of NC pins are connected to the substrate ($=V_{DD}$) and must be kept open. Other NC pins must be also kept open. When the LED-check (TEST) pin is not in use, it must not be kept open, but must be connected to GND.

Input Data Timing Chart



Output Data Timing Chart



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