

SANYO

No. 3725

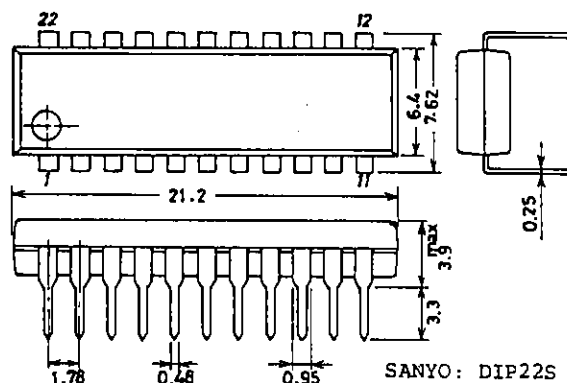
LC7470**Character and Pattern Display Control IC****Overview**

Character and pattern display control IC for TV screen

A character dot configuration is 12 x 18. The IC has 64 internal character ROMs and displays up to 288 characters (24 characters x 12 lines) on a TV screen. It can be controlled by a microcomputer.

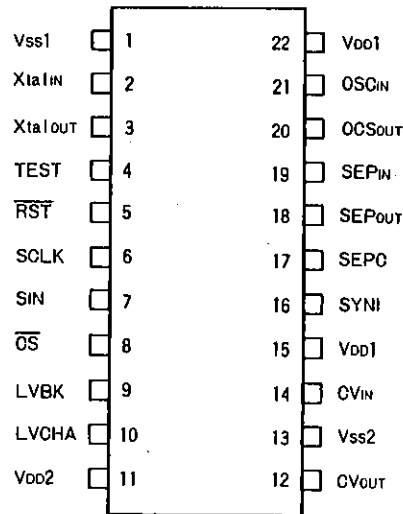
Functions and Applications

- | | |
|--|---|
| (1) Screen Display Mode | 24 characters x 12 lines |
| (2) Number of display characters | 288 characters (MAX.) |
| (3) Display control ROM (line ROM) | 64 lines (line control: 24-character line) |
| (4) Display RAM | 176 characters (used for specifying variable characters) |
| (5) Character configuration | 12 (horizontal) x 18 (vertical) dots |
| (6) Number of character types | 64 types |
| (7) Character size | Horizontal direction: 4, Vertical direction: 4 |
| (8) Display start position | Horizontal direction: 64, Vertical direction: 64 |
| (9) Blinking mode | Character blinking |
| (10) Display ON/OFF mode | ON/OFF cycle: 1.0 second and 0.5 second. Duty cycle: 25%, 50% and 75% |
| (11) Blanking mode | Entire font area (12 x 18 dots) |
| (12) Background colors | 4 (at internal SYNC. operation mode) |
| (13) External control input | Serial data input |
| (14) Synchronous signal | Selectable: Internal and External |
| (15) Internal SYNC. separation circuit available | |
| (16) Video output | NTSC-format composite output |
| (17) Superimpose function | Superimposes character output on composite video output |

Package Dimensions DIP-22S
(unit: mm)

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Pin Assignment



Absolute Maximum Ratings

Characteristics	Symbol	Condition	Ratings		unit
			min	max	
Supply Voltage	VDD	VDD1, VDD2	VSS-0.3	VSS+7.0	V
Input Voltage	VIN	All input pins	VSS-0.3	VDD1+0.3	V
Output Voltage	VOUT		VSS-0.3	VDD1+0.3	V
Maximum Current Dissipation	Pd max	Ta=25°C		300	mW
Operating Temperature	Topg		-30	+70	°C
Storage Temperature	Tstg		-40	+125	°C

Recommended Operating Conditions at Ta=-30 to +70 °C

Characteristics	Symbol	Condition	Ratings			unit
			min	typ	max	
Supply Voltage	VDD1	Pin VDD1	4.5	5.0	5.5	V
	VDD2	Pin VDD2	4.5	5.0	1.27VDD1	V
'H' Level Input Voltage	VIH2	Pins \overline{CS} , SIN, \overline{RST} , SCLK	0.8VDD1		VDD1+0.3	V
'L' Level Input Voltage	VIL2	Pins \overline{CS} , SIN, \overline{RST} , SCLK	VSS-0.3		0.2VDD1	V
Composite Video Input Voltage	VIN1	CVIN		2VP-P		V
	VIN2	Pin SYNI		2VP-P	2.5VP-P	
Oscillation Frequency	FOSC1	Xtal oscillation pin (at 4fosc)		14.31		MHz
	FOSC2	Xtal oscillation pin (at 2fosc)		7.16		MHz
	FOSC3	LC oscillation pin		7		MHz

Electrical characteristics (Ta=-30 °C to +70 °C, and VDD = 5V unless other noted)

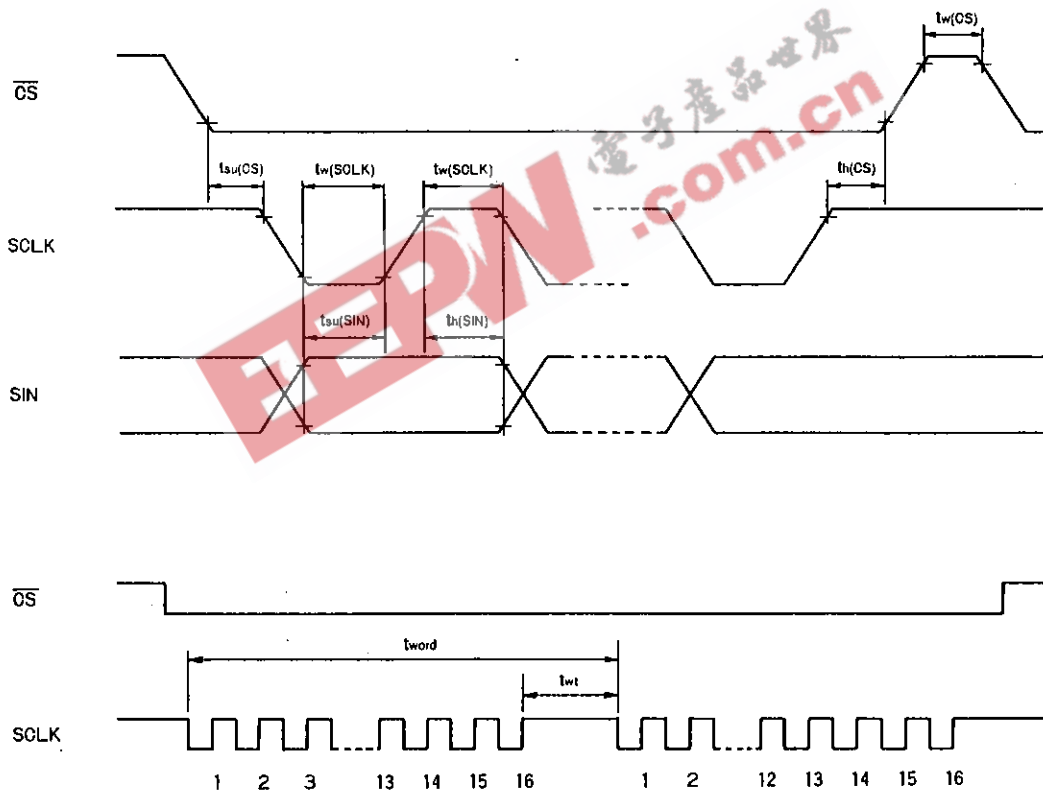
Characteristics	Symbol	Pin	Condition	Ratings			unit
				min	typ	max	
Output-off Leakage Current	Ileak	CVOUT			10	μA	
'H' Level Output Voltage	VIH1	SEPOUT	VDD=4.5V IOH=1.0mA	3.5		V	
'L' Level Output Voltage	VIL1	SEPOUT	VDD=4.5V IOL=1.0mA		1.0	V	
Input Current	IiH	\overline{CS} , SIN, \overline{RST} , SCLK, SEPIN	VIN=VDD		1	μA	
	IiL	OSCIN	VIN=VSS	-1		μA	
Operating Current Dissipation	IDD				15	mA	

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Timing Characteristics at $T_a = -30$ to $+70$ °C, $V_{DD} = 5 \pm 0.5V$

Characteristics	Symbol	Condition	Ratings			unit
			min	typ	max	
Minimum Input Pulse Width	$t_w(\text{SCLK})$	SCLK	200			ns
	$t_w(\text{CS})$	$\overline{\text{CS}}$ (CS="H" level period)	1			μs
Data Setup Time	$t_{su}(\text{CS})$	$\overline{\text{CS}}$	200			ns
	$t_{su}(\text{SIN})$	SIN	200			ns
Data Hold Time	$t_h(\text{CS})$	$\overline{\text{CS}}$	2			μs
	$t_h(\text{SIN})$	SIN	200			ns
1-Word Write Period	t_{word}	16-bit data write period	10			μs
	t_{wt}	RAM data write period	1			μs

Serial Data Input Timings



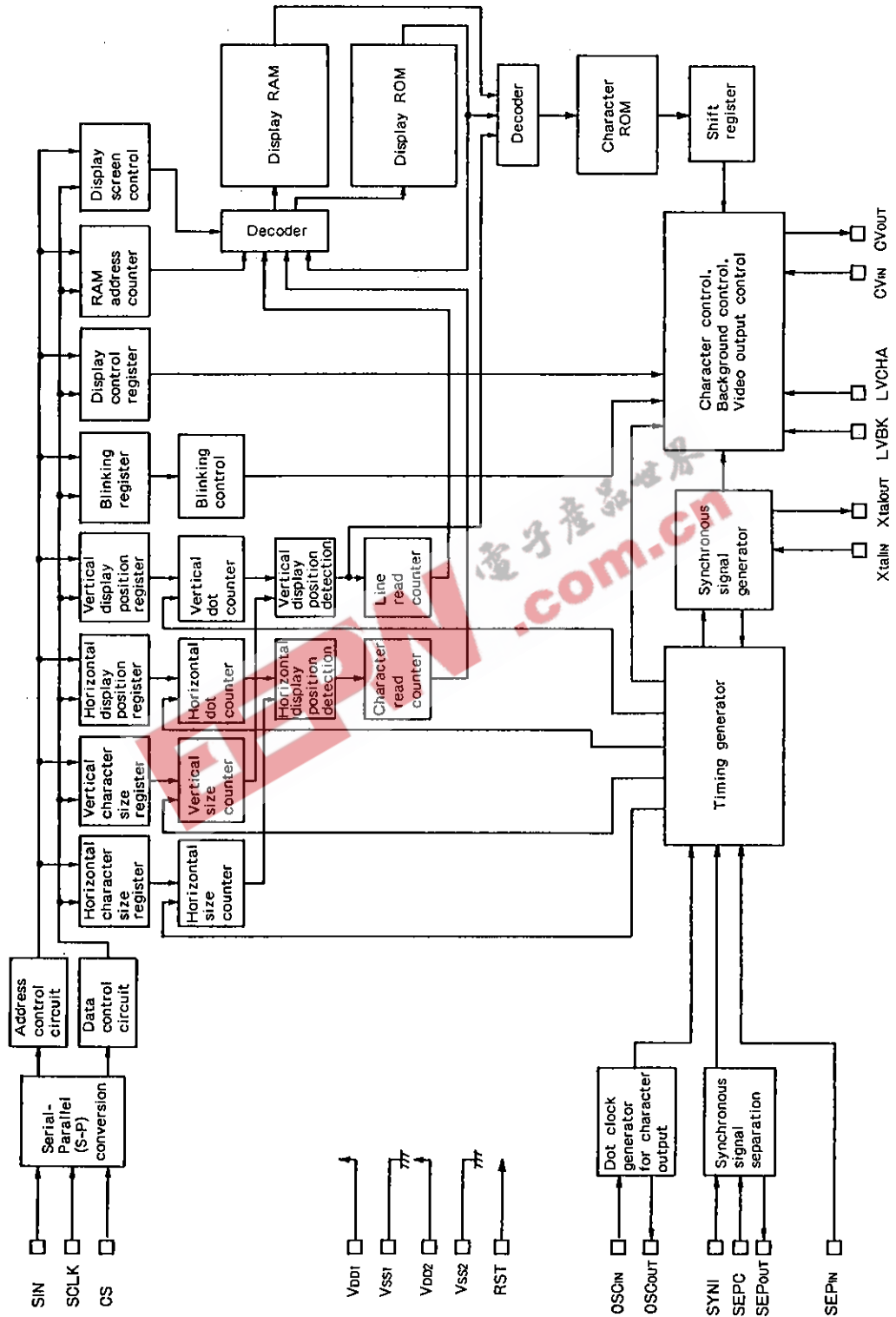
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Pin Description

Pin No.	Pin Symbol	Pin Name	Functions
1	VSS1	Ground pin	GND pin (digital grounding)
2	XtalIN	Xtal oscillation pin	Oscillation pins for connecting a crystal oscillator and capacitor to generate internal synchronous signals.
3	XtalOUT		
4	TEST	Test pin	Test output pin
5	RST	Reset input pin	System reset input pin
6	SCLK	Clock Input pin	Clock Input pin for serial data input
7	SIN	Data Input pin	Serial data Input pin. Serial 16-bit data input is supported.
8	\overline{CS}	Enable input pin	Enable Input pin for serial data input. If this pin becomes active (active low), the serial data input is enabled.
9	LVBK	Input pin for blank level adjustment	Level input pin for adjusting blank levels.
10	LVCHA	Input pin for character level adjustment	Level input pin for adjusting character levels.
11	VDD2	Power supply pin	Power supply pin for adjusting composite video signal levels (analog power supply)
12	CVOUT	Video signal output pin	Output pin for composite video signal
13	VSS2	Ground pin	GND pin (analog grounding)
14	CVIN	Video signal input pin	Input pin for composite video signal
15	VDD1	Supply voltage pin	Supply voltage pin (+5V)
16	SYNI	Synchronous signal separation circuit input pin	Input pin for synchronous signal separation circuit
17	SEPC	Synchronous signal separation circuit adjustment pin	Adjustment pin for synchronous signal separation circuit (A capacitor is connected to this pin.)
18	SEPOUT	Composite synchronous signal output pin	Composite synchronous signal output pin for synchronous signal separation circuit
19	SEPIN	Vertical synchronous signal input pin	Vertical synchronous signal input pin. The input signal to this pin is generated by integrating the output signal from the SEPOUT pin. Add an integral circuit between the SEPOUT pin and the SEPIN pin.
20	OSCOU	LC oscillation pin	Oscillation pins for connecting a coil and capacitor to generate character output dot clocks.
21	OSCI		
22	VDD1	Supply voltage pin (+5V)	Supply voltage (+5V)

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System Block Diagram



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Display Screen

The maximum display screen consists of horizontal 24 characters and vertical 12 lines. The number of display characters is 288 (MAX.). The display characters can consist of display line ROM (12 lines) data and display RAM (176 characters).

- Fixed characters can be specified by making an access to the display line ROM.
- Variable characters can be generated by programming the display RAM.

		← 24 characters →																							
12 lines	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	
	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	
	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	
	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	
	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	
	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	
	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	
	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	
	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	
	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	

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Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.

Address range from 0D (000h) to 175D (0AFh) used as the display RAM.

Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 2px;">Blinking</div> <div style="border: 1px solid black; padding: 2px;">Character code</div> </div> Display RAM area
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the first line
177 (0B1h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the second line
178 (0B2h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the third line
179 (0B3h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the fourth line
180 (0B4h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the fifth line
181 (0B5h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the sixth line
182 (0B6h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the seventh line
183 (0B7h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the eighth line
184 (0B8h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the ninth line
185 (0B9h)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the tenth line
186 (0BAh)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the eleventh line
187 (0BBh)	0	0	0	0	—	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification, First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position, Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position, Vertical character size.
190 (0BEh)	0	0	0	0	INT / NON	—	—	OSC STP	DSP ON	—	SYS RST	—	—	—	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TST MOD	—	—	BLK 1	BLK 0	—	BLINK 2	BLINK 1	BLINK 0	EX	—	BCOL	Control register

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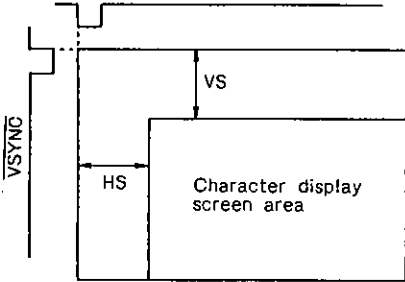
(1) Address 188D (0BCH)

DA 0~C	Register Name	Contents		Remarks									
		Status	Function										
0	HP0 (LSB)	0	If a horizontal display start position is defined as the HS, the HS can be calculated as follows: $HS = Tc \times (4 \sum_{n=0}^5 2^n HP_n)$ Tc: Oscillation cycle of the OSCIN-OSCOU oscillation circuit during operation.	The horizontal display start position is speci- fied by using six bits HP5 to HP0. The LSB (HP0) has a bit weight of 4Tc.									
		1											
1	HP1	0											
		1											
2	HP2	0											
		1											
3	HP3	0											
		1											
4	HP4	0											
		1											
5	HP5 (MSB)	0											
		1											
6	HSZ10	0	<table border="1"> <tr> <td>HSZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ11</td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ10	0	1	HSZ11	0	1Tc/1 dot		1	2Tc/1 dot	Horizontal character size for the first line
		HSZ10	0	1									
HSZ11	0	1Tc/1 dot											
	1	2Tc/1 dot											
1	<table border="1"> <tr> <td>HSZ11</td> <td>0</td> <td>1</td> </tr> <tr> <td></td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ11	0	1		0	1Tc/1 dot		1	2Tc/1 dot			
HSZ11	0	1											
	0	1Tc/1 dot											
	1	2Tc/1 dot											
7	HSZ11	0	<table border="1"> <tr> <td>HSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ21</td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ20	0	1	HSZ21	0	1Tc/1 dot		1	2Tc/1 dot	Horizontal character size for the second line
		HSZ20	0	1									
HSZ21	0	1Tc/1 dot											
	1	2Tc/1 dot											
1	<table border="1"> <tr> <td>HSZ21</td> <td>0</td> <td>1</td> </tr> <tr> <td></td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ21	0	1		0	1Tc/1 dot		1	2Tc/1 dot			
HSZ21	0	1											
	0	1Tc/1 dot											
	1	2Tc/1 dot											
A	HSZ30	0	<table border="1"> <tr> <td>HSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ31</td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ30	0	1	HSZ31	0	1Tc/1 dot		1	2Tc/1 dot	Horizontal character size for lines third to twelfth
		HSZ30	0	1									
HSZ31	0	1Tc/1 dot											
	1	2Tc/1 dot											
1	<table border="1"> <tr> <td>HSZ31</td> <td>0</td> <td>1</td> </tr> <tr> <td></td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ31	0	1		0	1Tc/1 dot		1	2Tc/1 dot			
HSZ31	0	1											
	0	1Tc/1 dot											
	1	2Tc/1 dot											
B	HSZ31	0	<table border="1"> <tr> <td>HSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ31</td> <td>0</td> <td>1Tc/1 dot</td> </tr> <tr> <td></td> <td>1</td> <td>2Tc/1 dot</td> </tr> </table>	HSZ30	0	1	HSZ31	0	1Tc/1 dot		1	2Tc/1 dot	
		HSZ30	0	1									
HSZ31	0	1Tc/1 dot											
	1	2Tc/1 dot											
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HSZ31	0	1											
	0	1Tc/1 dot											
	1	2Tc/1 dot											
C	—	0											
		1											

*: If the \overline{RST} pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

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(2) Address 189D (0BDH)

DA 0~C	Register Name	Contents		Remarks									
		Status	Function										
0	VP0 (LSB)	0	If a vertical display start position is defined as the VS, the VS can be calculated as follows: $VS = H \times (4 \sum_{n=0}^5 2^n VP_n)$ H: Horizontal synchronization pulse cycle HSYNC 	The vertical display start position is specified by using six bits VP5 to VP0. The LSB (VP0) has a bit weight of 4H.									
		1											
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5 (MSB)	0											
		1											
6	VSZ10	0	<table border="1"> <tr> <td>VSZ11 \ VSZ10</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1Tc/1 dot</td> <td>2Tc/1 dot</td> </tr> <tr> <td>1</td> <td>3Tc/1 dot</td> <td>4Tc/1 dot</td> </tr> </table>	VSZ11 \ VSZ10	0	0	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for the first line
		VSZ11 \ VSZ10	0	0									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
7	VSZ11	0	<table border="1"> <tr> <td>VSZ21 \ VSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1Tc/1 dot</td> <td>2Tc/1 dot</td> </tr> <tr> <td>1</td> <td>3Tc/1 dot</td> <td>4Tc/1 dot</td> </tr> </table>	VSZ21 \ VSZ20	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for the second line
		VSZ21 \ VSZ20	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
8	VSZ20	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1Tc/1 dot</td> <td>2Tc/1 dot</td> </tr> <tr> <td>1</td> <td>3Tc/1 dot</td> <td>4Tc/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	Vertical character size for lines third to twelfth
		VSZ31 \ VSZ30	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
A	VSZ30	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1Tc/1 dot</td> <td>2Tc/1 dot</td> </tr> <tr> <td>1</td> <td>3Tc/1 dot</td> <td>4Tc/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	
		VSZ31 \ VSZ30	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
B	VSZ31	0	<table border="1"> <tr> <td>VSZ31 \ VSZ30</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1Tc/1 dot</td> <td>2Tc/1 dot</td> </tr> <tr> <td>1</td> <td>3Tc/1 dot</td> <td>4Tc/1 dot</td> </tr> </table>	VSZ31 \ VSZ30	0	1	0	1Tc/1 dot	2Tc/1 dot	1	3Tc/1 dot	4Tc/1 dot	
		VSZ31 \ VSZ30	0	1									
0	1Tc/1 dot	2Tc/1 dot											
1	3Tc/1 dot	4Tc/1 dot											
1													
C	-	0											
		1											

*: If the \overline{RST} pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

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(3) Address 190D (0BEH)

DA 0~C	Register Name	Contents			Remarks
		Status	Function		
0	PHASE0	0	PHASE1	PHASE0	Background color
		1			
1	PHASE1	0	PHASE0	Background color	Background color
		1			
2	—	0			
		1			
3	—	0			
		1			
4	—	0			
		1			
5	SYSRST	0			With CS pin level = 'L', the LSI is reset. If the pin level changes to 'H', the LSI reset will be released.
		1	All the registers are reset and the display mode is inactivated.		
6	—	0			
		1			
7	DSPON	0	Character OFF		
		1	Character ON		
8	OSCSTP	0	The oscillation circuit does not enter a stop state if the display mode is inactivated.		To stop the crystal oscillation circuit and LC oscillation circuit.
		1	The oscillation circuit enters the stop state if the display mode is inactivated.		
9	—	0			
		1			
A	—	0			
		1			
B	INT/ NON	0	Interlace (262.5H/1 field)		Display operation mode selection: interlace and non-interlace
		1	Non-interlace (263H/1 field)		
C	—	0			
		1			

*: If the RST pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

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(4) Address 191D (0BFH)

DA 0~C	Register Name	Contents		Remarks																
		Status	Function																	
0	BCOL	0	Active background coloring (available only in internal synchronization mode)																	
		1	Inactive background coloring (background level adjustable only)																	
1	—	0																		
		1																		
2	EX	0	External synchronization	HSYNC and VSYNC signals selection: internal and external.																
		1	Internal synchronization																	
3	BLINK0	0	<table border="1" style="display: inline-table;"> <tr> <td></td> <td>BLINK0</td> <td>0</td> <td>1</td> </tr> <tr> <td>BLINK1</td> <td></td> <td>Blinking OFF mode</td> <td>Duty: 25%</td> </tr> <tr> <td>0</td> <td></td> <td>Duty: 50%</td> <td>Duty: 75%</td> </tr> <tr> <td>1</td> <td></td> <td></td> <td></td> </tr> </table>		BLINK0	0	1	BLINK1		Blinking OFF mode	Duty: 25%	0		Duty: 50%	Duty: 75%	1				Duty ratio control for blinking mode
				BLINK0	0	1														
BLINK1		Blinking OFF mode		Duty: 25%																
0		Duty: 50%		Duty: 75%																
1																				
1																				
4	BLINK1	0																		
		1																		
5	BLINK2	0	Blinking cycle: 1 second	Blinking cycle control																
		1	Blinking cycle: 0.5 seconds																	
6	—	0																		
		1																		
7	BLK0	0	<table border="1" style="display: inline-table;"> <tr> <td></td> <td>BLK0</td> <td>0</td> <td>1</td> </tr> <tr> <td>BLK1</td> <td></td> <td>Blanking OFF mode</td> <td>Character size</td> </tr> <tr> <td>0</td> <td></td> <td>Partial screen size</td> <td>Entire screen size</td> </tr> <tr> <td>1</td> <td></td> <td></td> <td></td> </tr> </table>		BLK0	0	1	BLK1		Blanking OFF mode	Character size	0		Partial screen size	Entire screen size	1				Blanking size control
				BLK0	0	1														
BLK1		Blanking OFF mode		Character size																
0		Partial screen size		Entire screen size																
1																				
1																				
8	BLK1	0																		
		1																		
9	—	0																		
		1																		
A	—	0																		
		1																		
B	TSTMOD	0	Normal operation	Should be fixed to "0".																
		1	Test mode																	
C	—	0																		
		1																		

*: If the \overline{RST} pin becomes active (the LSI is reset), the contents of all the registers will be set to "0".

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Memory Configuration (display line ROM)

The display line ROM address range is from 0D (000H) to 1535D (5FFH).
Data consists of 7 bits.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
0000 (000h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the first line
0023 (017h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the first line
0024 (018h)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the second line
									ROM/RAM		Character code						
1535 (5FFh)	0	0	0	0	0	0	0	0	ROM/RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the sixty-fourth line

DA 0~8	Register Name	Contents		Remarks					
		Status	Function						
0	ADR0	0	Used to specify the desired character ROM address.						
		1	To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'.						
1	ADR1	0	To access the character ROM, addresses 0D (000) to 63D (3FH) can be used.						
		1			Set bit 6 (ADR6) to '0'.				
2	ADR2	0			Set bit 6 (ADR6) to '0'.				
		1							
3	ADR3	0							
		1							
4	ADR4	0							
		1							
5	ADR5	0							
		1							
6	ADR6	0							
		1							
7	ROM/RAM	0		Direct read access to the character ROM					
		1		Read access to the character ROM through the display RAM.					

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Display Line ROM: Line Address Table

Line No.	Address No.	Line No.	Address No.
1st line	00HEX (0000)	33rd line	300HEX (0768)
2nd line	18HEX (0024)	34th line	318HEX (0792)
3rd line	30HEX (0048)	35th line	330HEX (0816)
4th line	48HEX (0072)	36th line	348HEX (0840)
5th line	60HEX (0096)	37th line	360HEX (0864)
6th line	78HEX (0120)	38th line	378HEX (0888)
7th line	90HEX (0144)	39th line	390HEX (0912)
8th line	A8HEX (0168)	40th line	3A8HEX (0936)
9th line	C0HEX (0192)	41st line	3C0HEX (0960)
10th line	D8HEX (0216)	42nd line	3D8HEX (0984)
11st line	F0HEX (0240)	43rd line	3F0HEX (1008)
12th line	108HEX (0264)	44th line	408HEX (1032)
13th line	120HEX (0288)	45th line	420HEX (1056)
14th line	138HEX (0312)	46th line	438HEX (1080)
15th line	150HEX (0336)	47th line	450HEX (1104)
16th line	168HEX (0360)	48th line	468HEX (1128)
17th line	180HEX (0384)	49th line	480HEX (1152)
18th line	198HEX (0408)	50th line	498HEX (1176)
19th line	1B0HEX (0432)	51st line	4B0HEX (1200)
20th line	1C8HEX (0456)	52nd line	4C8HEX (1224)
21st line	1E0HEX (0480)	53rd line	4E0HEX (1248)
22nd line	1F8HEX (0504)	54th line	4F8HEX (1272)
23rd line	210HEX (0528)	55th line	510HEX (1296)
24th line	228HEX (0552)	56th line	528HEX (1320)
25th line	240HEX (0576)	57th line	540HEX (1344)
26th line	258HEX (0600)	58th line	558HEX (1368)
27th line	270HEX (0624)	59th line	570HEX (1392)
28th line	288HEX (0648)	60th line	588HEX (1416)
29th line	2A0HEX (0672)	61st line	5A0HEX (1440)
30th line	2B8HEX (0696)	62nd line	5B8HEX (1464)
31st line	2D0HEX (0720)	63rd line	5D0HEX (1488)
32nd line	2E8HEX (0744)	64th line	5E8HEX (1512)

Sample Display Screen

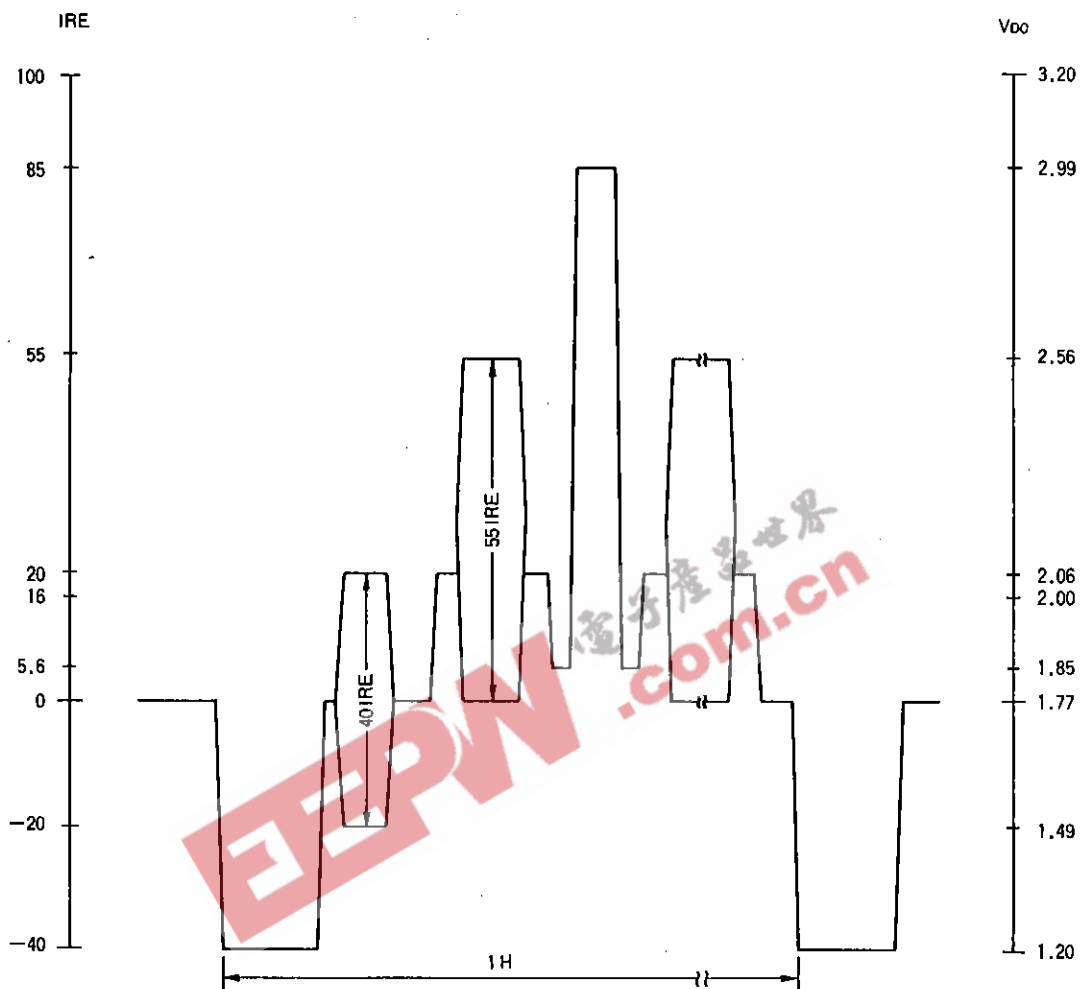
Twelve display lines of the display 64-line ROM are specified.
 Variable characters are prepared in the display control RAM.
 The display RAM address area is automatically allocated to addresses from 0D (000H) to 175D (AFH) in the display order.

- The display characters indicated by bold lines are specified through the display RAM access.
- The display characters indicated by slender lines are specified directly through the display ROM access.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24																																																																																																																																																																																																																																																								
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 0Fh	RAM 000 00h	RAM 001 01h	RAM 002 02h	RAM 003 03h	RAM 004 04h	RAM 005 05h	RAM 006 06h	RAM 007 07h	RAM 008 08h	RAM 009 09h	RAM 010 0Ah	RAM 011 0Bh	RAM 012 0Ch	RAM 013 0Dh	RAM 014 0Eh	RAM 015 0Fh																																																																																																																																																																																																																																																
2	ROM 024 18h	ROM 025 19h	ROM 026 1Ah	ROM 027 1Bh	ROM 028 1Ch	ROM 029 1Dh	ROM 030 1Eh	ROM 031 1Fh	ROM 032 20h	ROM 033 21h	ROM 034 22h	ROM 035 23h	ROM 036 24h	ROM 037 25h	ROM 038 26h	ROM 039 27h	RAM 040 28h	RAM 041 29h	RAM 042 2Ah	RAM 043 2Bh	RAM 044 2Ch	RAM 045 2Dh	RAM 046 2Eh	RAM 047 2Fh	RAM 048 30h	RAM 049 31h	RAM 050 32h	RAM 051 33h	RAM 052 34h	RAM 053 35h	RAM 054 36h	RAM 055 37h	RAM 056 38h	RAM 057 39h	RAM 058 3Ah	RAM 059 3Bh	RAM 060 3Ch	RAM 061 3Dh	RAM 062 3Eh	RAM 063 3Fh	RAM 064 40h	RAM 065 41h	RAM 066 42h	RAM 067 43h	RAM 068 44h	RAM 069 45h	RAM 070 46h	RAM 071 47h	RAM 072 48h	RAM 073 49h	RAM 074 4Ah	RAM 075 4Bh	RAM 076 4Ch	RAM 077 4Dh	RAM 078 4Eh	RAM 079 4Fh	RAM 080 50h	RAM 081 51h	RAM 082 52h	RAM 083 53h	RAM 084 54h	RAM 085 55h	RAM 086 56h	RAM 087 57h	RAM 088 58h	RAM 089 59h	RAM 090 5Ah	RAM 091 5Bh	RAM 092 5Ch	RAM 093 5Dh	RAM 094 5Eh	RAM 095 5Fh	RAM 096 60h	RAM 097 61h	RAM 098 62h	RAM 099 63h	RAM 100 64h	RAM 101 65h	RAM 102 66h	RAM 103 67h	RAM 104 68h	RAM 105 69h	RAM 106 6Ah	RAM 107 6Bh	RAM 108 6Ch	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh	RAM 112 70h	RAM 113 71h	RAM 114 72h	RAM 115 73h	RAM 116 74h	RAM 117 75h	RAM 118 76h	RAM 119 77h	RAM 120 78h	RAM 121 79h	RAM 122 7Ah	RAM 123 7Bh	RAM 124 7Ch	RAM 125 7Dh	RAM 126 7Eh	RAM 127 7Fh	RAM 128 80h	RAM 129 81h	RAM 130 82h	RAM 131 83h	RAM 132 84h	RAM 133 85h	RAM 134 86h	RAM 135 87h	RAM 136 88h	RAM 137 89h	RAM 138 8Ah	RAM 139 8Bh	RAM 140 8Ch	RAM 141 8Dh	RAM 142 8Eh	RAM 143 8Fh	RAM 144 90h	RAM 145 91h	RAM 146 92h	RAM 147 93h	RAM 148 94h	RAM 149 95h	RAM 150 96h	RAM 151 97h	RAM 152 98h	RAM 153 99h	RAM 154 9Ah	RAM 155 9Bh	RAM 156 9Ch	RAM 157 9Dh	RAM 158 9Eh	RAM 159 9Fh	RAM 160 A0h	RAM 161 A1h	RAM 162 A2h	RAM 163 A3h	RAM 164 A4h	RAM 165 A5h	RAM 166 A6h	RAM 167 A7h	RAM 168 A8h	RAM 169 A9h	RAM 170 AAh	RAM 171 ABh	RAM 172 ACh	RAM 173 ADh	RAM 174 AEh	RAM 175 AFh																																																																																																																								
3	RAM 080 50h	RAM 081 51h	RAM 082 52h	RAM 083 53h	RAM 084 54h	RAM 085 55h	RAM 086 56h	RAM 087 57h	RAM 088 58h	RAM 089 59h	RAM 090 5Ah	RAM 091 5Bh	RAM 092 5Ch	RAM 093 5Dh	RAM 094 5Eh	RAM 095 5Fh	RAM 096 60h	RAM 097 61h	RAM 098 62h	RAM 099 63h	RAM 100 64h	RAM 101 65h	RAM 102 66h	RAM 103 67h	RAM 104 68h	RAM 105 69h	RAM 106 6Ah	RAM 107 6Bh	RAM 108 6Ch	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh	RAM 112 70h	RAM 113 71h	RAM 114 72h	RAM 115 73h	RAM 116 74h	RAM 117 75h	RAM 118 76h	RAM 119 77h	RAM 120 78h	RAM 121 79h	RAM 122 7Ah	RAM 123 7Bh	RAM 124 7Ch	RAM 125 7Dh	RAM 126 7Eh	RAM 127 7Fh	RAM 128 80h	RAM 129 81h	RAM 130 82h	RAM 131 83h	RAM 132 84h	RAM 133 85h	RAM 134 86h	RAM 135 87h	RAM 136 88h	RAM 137 89h	RAM 138 8Ah	RAM 139 8Bh	RAM 140 8Ch	RAM 141 8Dh	RAM 142 8Eh	RAM 143 8Fh	RAM 144 90h	RAM 145 91h	RAM 146 92h	RAM 147 93h	RAM 148 94h	RAM 149 95h	RAM 150 96h	RAM 151 97h	RAM 152 98h	RAM 153 99h	RAM 154 9Ah	RAM 155 9Bh	RAM 156 9Ch	RAM 157 9Dh	RAM 158 9Eh	RAM 159 9Fh	RAM 160 A0h	RAM 161 A1h	RAM 162 A2h	RAM 163 A3h	RAM 164 A4h	RAM 165 A5h	RAM 166 A6h	RAM 167 A7h	RAM 168 A8h	RAM 169 A9h	RAM 170 AAh	RAM 171 ABh	RAM 172 ACh	RAM 173 ADh	RAM 174 AEh	RAM 175 AFh																																																																																																																																																																																
4	RAM 160 A0h	RAM 161 A1h	RAM 162 A2h	RAM 163 A3h	RAM 164 A4h	RAM 165 A5h	RAM 166 A6h	RAM 167 A7h	RAM 168 A8h	RAM 169 A9h	RAM 170 AAh	RAM 171 ABh	RAM 172 ACh	RAM 173 ADh	RAM 174 AEh	RAM 175 AFh	RAM 176 B0h	RAM 177 B1h	RAM 178 B2h	RAM 179 B3h	RAM 180 B4h	RAM 181 B5h	RAM 182 B6h	RAM 183 B7h	RAM 184 B8h	RAM 185 B9h	RAM 186 BAh	RAM 187 B Bh	RAM 188 BCh	RAM 189 BDh	RAM 190 BEh	RAM 191 BFh	RAM 192 C0h	RAM 193 C1h	RAM 194 C2h	RAM 195 C3h	RAM 196 C4h	RAM 197 C5h	RAM 198 C6h	RAM 199 C7h	RAM 200 C8h	RAM 201 C9h	RAM 202 CAh	RAM 203 C Bh	RAM 204 CCh	RAM 205 CDh	RAM 206 CEh	RAM 207 CFh	RAM 208 D0h	RAM 209 D1h	RAM 210 D2h	RAM 211 D3h	RAM 212 D4h	RAM 213 D5h	RAM 214 D6h	RAM 215 D7h	RAM 216 D8h	RAM 217 D9h	RAM 218 DAh	RAM 219 DBh	RAM 220 DCh	RAM 221 DDh	RAM 222 DEh	RAM 223 DFh	RAM 224 E0h	RAM 225 E1h	RAM 226 E2h	RAM 227 E3h	RAM 228 E4h	RAM 229 E5h	RAM 230 E6h	RAM 231 E7h	RAM 232 E8h	RAM 233 E9h	RAM 234 EAh	RAM 235 EBh	RAM 236 ECh	RAM 237 EDh	RAM 238 EEh	RAM 239 EFh	RAM 240 F0h	RAM 241 F1h	RAM 242 F2h	RAM 243 F3h	RAM 244 F4h	RAM 245 F5h	RAM 246 F6h	RAM 247 F7h	RAM 248 F8h	RAM 249 F9h	RAM 250 FAh	RAM 251 FBh	RAM 252 FCh	RAM 253 FDh	RAM 254 FEh	RAM 255 FFh																																																																																																																																																																																
5	RAM 240 F0h	RAM 241 F1h	RAM 242 F2h	RAM 243 F3h	RAM 244 F4h	RAM 245 F5h	RAM 246 F6h	RAM 247 F7h	RAM 248 F8h	RAM 249 F9h	RAM 250 FAh	RAM 251 FBh	RAM 252 FCh	RAM 253 FDh	RAM 254 FEh	RAM 255 FFh	RAM 256 00h	RAM 257 01h	RAM 258 02h	RAM 259 03h	RAM 260 04h	RAM 261 05h	RAM 262 06h	RAM 263 07h	RAM 264 08h	RAM 265 09h	RAM 266 0Ah	RAM 267 0Bh	RAM 268 0Ch	RAM 269 0Dh	RAM 270 0Eh	RAM 271 0Fh	RAM 272 10h	RAM 273 11h	RAM 274 12h	RAM 275 13h	RAM 276 14h	RAM 277 15h	RAM 278 16h	RAM 279 17h	RAM 280 18h	RAM 281 19h	RAM 282 1Ah	RAM 283 1Bh	RAM 284 1Ch	RAM 285 1Dh	RAM 286 1Eh	RAM 287 1Fh	RAM 288 20h	RAM 289 21h	RAM 290 22h	RAM 291 23h	RAM 292 24h	RAM 293 25h	RAM 294 26h	RAM 295 27h	RAM 296 28h	RAM 297 29h	RAM 298 2Ah	RAM 299 2Bh	RAM 300 2Ch	RAM 301 2Dh	RAM 302 2Eh	RAM 303 2Fh	RAM 304 30h	RAM 305 31h	RAM 306 32h	RAM 307 33h	RAM 308 34h	RAM 309 35h	RAM 310 36h	RAM 311 37h	RAM 312 38h	RAM 313 39h	RAM 314 3Ah	RAM 315 3Bh	RAM 316 3Ch	RAM 317 3Dh	RAM 318 3Eh	RAM 319 3Fh	RAM 320 40h	RAM 321 41h	RAM 322 42h	RAM 323 43h	RAM 324 44h	RAM 325 45h	RAM 326 46h	RAM 327 47h	RAM 328 48h	RAM 329 49h	RAM 330 4Ah	RAM 331 4Bh	RAM 332 4Ch	RAM 333 4Dh	RAM 334 4Eh	RAM 335 4Fh	RAM 336 50h	RAM 337 51h	RAM 338 52h	RAM 339 53h	RAM 340 54h	RAM 341 55h	RAM 342 56h	RAM 343 57h	RAM 344 58h	RAM 345 59h	RAM 346 5Ah	RAM 347 5Bh	RAM 348 5Ch	RAM 349 5Dh	RAM 350 5Eh	RAM 351 5Fh	RAM 352 60h	RAM 353 61h	RAM 354 62h	RAM 355 63h	RAM 356 64h	RAM 357 65h	RAM 358 66h	RAM 359 67h	RAM 360 68h	RAM 361 69h	RAM 362 6Ah	RAM 363 6Bh	RAM 364 6Ch	RAM 365 6Dh	RAM 366 6Eh	RAM 367 6Fh	RAM 368 70h	RAM 369 71h	RAM 370 72h	RAM 371 73h	RAM 372 74h	RAM 373 75h	RAM 374 76h	RAM 375 77h	RAM 376 78h	RAM 377 79h	RAM 378 7Ah	RAM 379 7Bh	RAM 380 7Ch	RAM 381 7Dh	RAM 382 7Eh	RAM 383 7Fh	RAM 384 80h	RAM 385 81h	RAM 386 82h	RAM 387 83h	RAM 388 84h	RAM 389 85h	RAM 390 86h	RAM 391 87h	RAM 392 88h	RAM 393 89h	RAM 394 8Ah	RAM 395 8Bh	RAM 396 8Ch	RAM 397 8Dh	RAM 398 8Eh	RAM 399 8Fh	RAM 400 90h	RAM 401 91h	RAM 402 92h	RAM 403 93h	RAM 404 94h	RAM 405 95h	RAM 406 96h	RAM 407 97h	RAM 408 98h	RAM 409 99h	RAM 410 9Ah	RAM 411 9Bh	RAM 412 9Ch	RAM 413 9Dh	RAM 414 9Eh	RAM 415 9Fh	RAM 416 A0h	RAM 417 A1h	RAM 418 A2h	RAM 419 A3h	RAM 420 A4h	RAM 421 A5h	RAM 422 A6h	RAM 423 A7h	RAM 424 A8h	RAM 425 A9h	RAM 426 AAh	RAM 427 ABh	RAM 428 ACh	RAM 429 ADh	RAM 430 AEh	RAM 431 AFh	RAM 432 B0h	RAM 433 B1h	RAM 434 B2h	RAM 435 B3h	RAM 436 B4h	RAM 437 B5h	RAM 438 B6h	RAM 439 B7h	RAM 440 B8h	RAM 441 B9h	RAM 442 BAh	RAM 443 B Bh	RAM 444 BCh	RAM 445 BDh	RAM 446 BEh	RAM 447 BFh	RAM 448 C0h	RAM 449 C1h	RAM 450 C2h	RAM 451 C3h	RAM 452 C4h	RAM 453 C5h	RAM 454 C6h	RAM 455 C7h	RAM 456 C8h	RAM 457 C9h	RAM 458 CAh	RAM 459 C Bh	RAM 460 CCh	RAM 461 CDh	RAM 462 CEh	RAM 463 CFh	RAM 464 D0h	RAM 465 D1h	RAM 466 D2h	RAM 467 D3h	RAM 468 D4h	RAM 469 D5h	RAM 470 D6h	RAM 471 D7h	RAM 472 D8h	RAM 473 D9h	RAM 474 DAh	RAM 475 DBh	RAM 476 DCh	RAM 477 DDh	RAM 478 DEh	RAM 479 DFh	RAM 480 E0h	RAM 481 E1h	RAM 482 E2h	RAM 483 E3h	RAM 484 E4h	RAM 485 E5h	RAM 486 E6h	RAM 487 E7h	RAM 488 E8h	RAM 489 E9h	RAM 490 EAh	RAM 491 EBh	RAM 492 ECh	RAM 493 EDh	RAM 494 EEh	RAM 495 EFh	RAM 496 F0h	RAM 497 F1h	RAM 498 F2h	RAM 499 F3h	RAM 500 F4h	RAM 501 F5h	RAM 502 F6h	RAM 503 F7h	RAM 504 F8h	RAM 505 F9h	RAM 506 FAh	RAM 507 FBh	RAM 508 FCh	RAM 509 FDh	RAM 510 FEh	RAM 511 FFh
6	RAM 500 F0h	RAM 501 F1h	RAM 502 F2h	RAM 503 F3h	RAM 504 F4h	RAM 505 F5h	RAM 506 F6h	RAM 507 F7h	RAM 508 F8h	RAM 509 F9h	RAM 510 FAh	RAM 511 FBh	RAM 512 FCh	RAM 513 FDh	RAM 514 FEh	RAM 515 FFh	RAM 516 00h	RAM 517 01h	RAM 518 02h	RAM 519 03h	RAM 520 04h	RAM 521 05h	RAM 522 06h	RAM 523 07h	RAM 524 08h	RAM 525 09h	RAM 526 0Ah	RAM 527 0Bh	RAM 528 0Ch	RAM 529 0Dh	RAM 530 0Eh	RAM 531 0Fh	RAM 532 10h	RAM 533 11h	RAM 534 12h	RAM 535 13h	RAM 536 14h	RAM 537 15h	RAM 538 16h	RAM 539 17h	RAM 540 18h	RAM 541 19h	RAM 542 1Ah	RAM 543 1Bh	RAM 544 1Ch	RAM 545 1Dh	RAM 546 1Eh	RAM 547 1Fh	RAM 548 20h	RAM 549 21h	RAM 550 22h	RAM 551 23h	RAM 552 24h	RAM 553 25h	RAM 554 26h	RAM 555 27h	RAM 556 28h	RAM 557 29h	RAM 558 2Ah	RAM 559 2Bh	RAM 560 2Ch	RAM 561 2Dh	RAM 562 2Eh	RAM 563 2Fh	RAM 564 30h	RAM 565 31h	RAM 566 32h	RAM 567 33h	RAM 568 34h	RAM 569 35h	RAM 570 36h	RAM 571 37h	RAM 572 38h	RAM 573 39h	RAM 574 3Ah	RAM 575 3Bh	RAM 576 3Ch	RAM 577 3Dh	RAM 578 3Eh	RAM 579 3Fh	RAM 580 40h	RAM 581 41h	RAM 582 42h	RAM 583 43h	RAM 584 44h	RAM 585 45h	RAM 586 46h	RAM 587 47h	RAM 588 48h	RAM 589 49h	RAM 590 4Ah	RAM 591 4Bh	RAM 592 4Ch	RAM 593 4Dh	RAM 594 4Eh	RAM 595 4Fh	RAM 596 50h	RAM 597 51h	RAM 598 52h	RAM 599 53h	RAM 600 54h	RAM 601 55h	RAM 602 56h	RAM 603 57h	RAM 604 58h	RAM 605 59h	RAM 606 5Ah	RAM 607 5Bh	RAM 608 5Ch	RAM 609 5Dh	RAM 610 5Eh	RAM 611 5Fh	RAM 612 60h	RAM 613 61h	RAM 614 62h	RAM 615 63h	RAM 616 64h	RAM 617 65h	RAM 618 66h	RAM 619 67h	RAM 620 68h	RAM 621 69h	RAM 622 6Ah	RAM 623 6Bh	RAM 624 6Ch	RAM 625 6Dh	RAM 626 6Eh	RAM 627 6Fh	RAM 628 70h	RAM 629 71h	RAM 630 72h	RAM 631 73h	RAM 632 74h	RAM 633 75h	RAM 634 76h	RAM 635 77h	RAM 636 78h	RAM 637 79h	RAM 638 7Ah	RAM 639 7Bh	RAM 640 7Ch	RAM 641 7Dh	RAM 642 7Eh	RAM 643 7Fh																																																																																																																																

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Composite Video Signal Output Level (internal generation)



Output level (IRE)	Output voltage (VDC)
100	3.200
85	2.986
46.1	2.430
20	2.057
5.8	1.854
0	1.771
-20	1.486
-40	1.200

$V_{DD}=5.000V_{DC}$