Ordering number: EN3258A

SANYO No. 3258A

CMOS LSI

LC7584N

LCD DRIVER with CHARACTER GENERATOR

Overview

The LC7584N is an LCD driver which has the serial interface with a microcomputer, and controls and drives a 1/2-duty LCD. It supports a segment display and level meter display.

The segment display enables up to 6 characters (that is, 6-digit display layout. 14 segments per digit) to be displayed at the same time.

The character generator (CG) generates the segment patterns to display sixty-four characters, symbols and the like on the LCD panel.

Any segment pattern can be generated not via the programmable logic array CG circuit.

The level meter display enables the data output from the on-chip 5- bit AD converter on the LCD panel.

Features

1. 1/2 duty-1/2 bias 96 segments (maximum. Note that the number of segments used for level meter display and direct display is not included here.)

2. Number of characters displayed at the same time = 6 digits (maximum). 14 segments per digit. Characters, symbols and so on to be displayed = 64 kinds

3. Characters and any segment pattern can be displayed on the LCD panel at the same time.

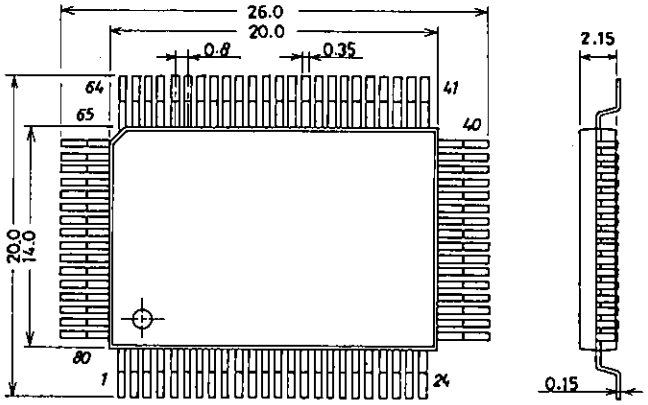
4. Display pin provided for direct display ($\overline{DSP1}$ and $\overline{DSP2}$ pins)

5. On-chip 5-bit AD converter. The following three level output modes are available.
   (1) 13-ladder x 2 channels --- Log scale (with peak hold function)
   (2) 13-ladder x 2 channels --- Linear scale (with peak hold function)
   (3) 26-ladder x 1 channel --- Linear scale

6. The reset time of the peak hold latch circuit for level output can be determined by an external CR time constant.

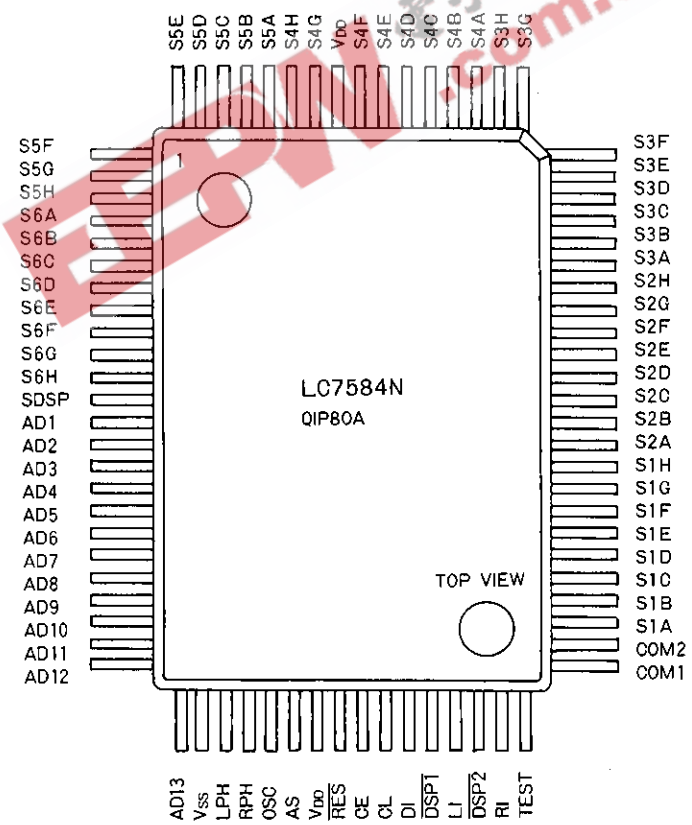
7. All of these LSI chip functions can be controlled by the seven commands from a microcomputer.

Package Dimensions 3044B
(unit: mm)



SANYO: QIP80A

Pin layout



Absolute maximum ratings at Ta=25℃,Vss=0V

				unit
Supply voltage	V_{DD}		-0.3 to +6.5	V
Input voltage	$V_{IN}(1)$	$\overline{RES}$,CE,CL,DI,$\overline{DSP1}$,$\overline{DSP2}$	-0.3 to +6.5	V
	$V_{IN}(2)$	LPH,RPH,LI,RI,OSC,AS	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	LPH,RPH,OSC, all output pins	-0.3 to V_{DD}+0.3	V
Maximum power dissipation	Pdmax	Ta≦85℃	200	mW
Operating ambient temperature	**Topr**		-40 to +85	℃
Storage ambient temperature	Tstg		-50 to +125	℃

Allowable operating conditions at Ta=-40 to 85℃, Vss=0V

			min	typ	max	unit
Supply voltage	$V_{DD}(1)$	AD converter used	4.0		5.5	V
	$V_{DD}(2)$	AD converter not used	3.0		5.5	V
H-level input voltage	$V_{IH}(1)$	$\overline{RES}$,CE,CL,DI	0.6V_{DD}		5.5	V
	$V_{IH}(2)$	$\overline{DSP1}$,$\overline{DSP2}$	0.7V_{DD}		5.5	V
	$V_{IH}(3)$	AS	0.7V_{DD}		V_{DD}	V
L-level input voltage	$V_{IL}(1)$	$\overline{RES}$,CE,CL,DI	0		0.2V_{DD}	V
	$V_{IL}(2)$	$\overline{DSP1}$,$\overline{DSP2}$	0		0.3V_{DD}	V
	$V_{IL}(3)$	AS	0		0.3V_{DD}	V
Input voltage	V_{IN}	LI,RI	0		V_{DD}	V
Oscillation frequency	fosc	OSC		160		kHz
Recommended external resistance	Rosc	OSC		36		kΩ
Recommended external capacitance	Cosc	OSC		220		pF
Recommended external resistance	R_{PH}	LPH,RPH			700	kΩ
Recommended external capacitance	C_{PH}	LPH,RPH			15	μF
Minimum operational pulse width	P_{RES}	$\overline{RES}$	1.0			μs

Electrical characteristics/Under the allowable operational conditions

			min	typ	max	unit
H-level input current	I_{IH}	$\overline{RES}$,CE,CL,DI,$\overline{DSP1}$,$\overline{DSP2}$ (V_I=5.5V)			5.0	μA
L-level input current	I_{IL}	$\overline{RES}$,CE,CL,DI,$\overline{DSP1}$,$\overline{DSP2}$ (V_I=Vss)			5.0	μA
Pull-down resistance	R_{PD}	TEST		50		kΩ
Hysteresis width	V_H	CE,CL,DI	0.03V_{DD}			V
L-level output voltage	$V_{OL}(1)$	OSC (Io=1mA)			2.0	V
	$V_{OL}(2)$	LPH,RPH (Io=1mA)			0.1	V
Oscillation frequency	fosc(1)	OSC(C=220pF R=36kΩ,V_{DD}(1))	130	160	200	kHz
	fosc(2)	OSC(C=220pF R=36kΩ,V_{DD}(2))	120	160	200	kHz

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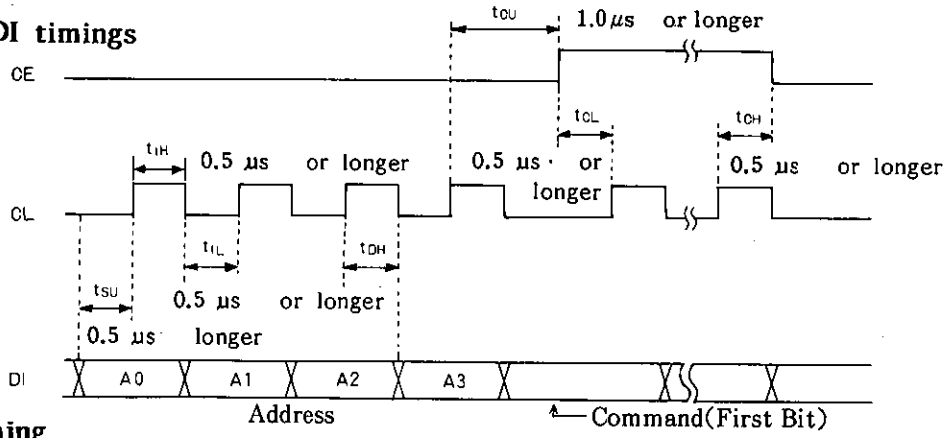
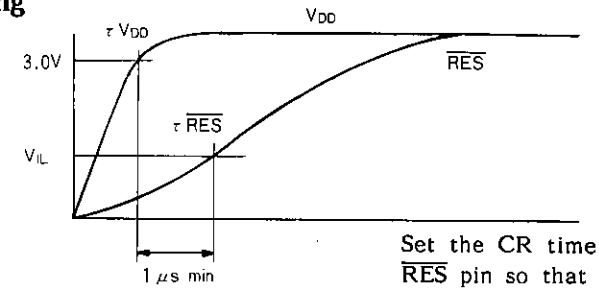
			min	typ	max	unit
H-level input threshold voltage	$V_{TH}(1)$	OSC	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
	$V_{TH}(2)$	LPH,RPH	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
AD conversion error	AD_{ERR}	LI,RI	-1/2		1/2	LSB
H-level output voltage	$V_{OH}(1)$	Smn,ADm,SDSP (Io=0.1mA,$V_{DD}(1)$)	V_{DD}-0.5			V
	$V_{OH}(2)$	(Io=0.1mA,$V_{DD}(2)$)	V_{DD}-0.7			V
L-level output voltage	$V_{OL}(3)$	Smn,ADm,SDSP (Io=0.1mA,$V_{DD}(1)$)			0.5	V
	$V_{OL}(4)$	(Io=0.1mA,$V_{DD}(2)$)			0.7	V
H-level output voltage	$V_{OH}(3)$	COM1,COM2 (Io=0.1mA) (C_M=0;2kΩ)	V_{DD}-0.3	V_{DD}-0.2	V_{DD}-0.1	V
L-level output voltage	$V_{OL}(5)$	COM1,COM2 (Io=0.1mA) (C_M=0;2kΩ)	0.1	0.2	0.3	V
H-level output voltage	$V_{OH}(4)$	COM1,COM2 (Io=0.01mA) (C_M=1;50kΩ)	V_{DD}-0.7	V_{DD}-0.5	V_{DD}-0.3	V
L-level output voltage	$V_{OL}(6)$	COM1,COM2 (Io=0.01mA) (C_M=1;50kΩ)	0.3	0.5	0.7	V
Intermediate level voltage	V_{MID}	COM1,COM2 (Pin='open') (C_M=0,1)	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
Supply current	$I_{DD}(1)$	ADC used (C_M=0;2kΩ) Note 1		2.5	4.0	mA
Supply current	$I_{DD}(2)$	ADC not used (C_M=0;2kΩ) Note 1		1.8	3.0	mA
Supply current	$I_{DD}(3)$	ADC used (C_M=1;50kΩ) Note 1		1.0	2.0	mA
Supply current	$I_{DD}(4)$	ADC not used (C_M=1;50kΩ) Note 1		0.5	1.0	mA
High-level clock pulse width	t_{wH}	CL	0.5			μs
Low-level clock pulse width	t_{wL}	CL	0.5			μs
Data set-up time	t_{SU}	CL,DI	0.5			μs
Data hold time	t_{DH}	CL,DI	0.5			μs
CE set-up time	t_{CU}	CL,CE	1.0			μs
CE clock time	t_{CL}	CL,CE	0.5			μs
CE hold time	t_{CH}	CL,CE	0.5			μs

Note 1: fosc = 160kHz and output pins = 'open'.

CE, CL and DI timings

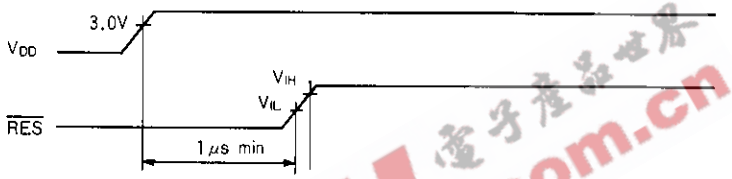


V_{DD}-$\overline{RES}$ timing

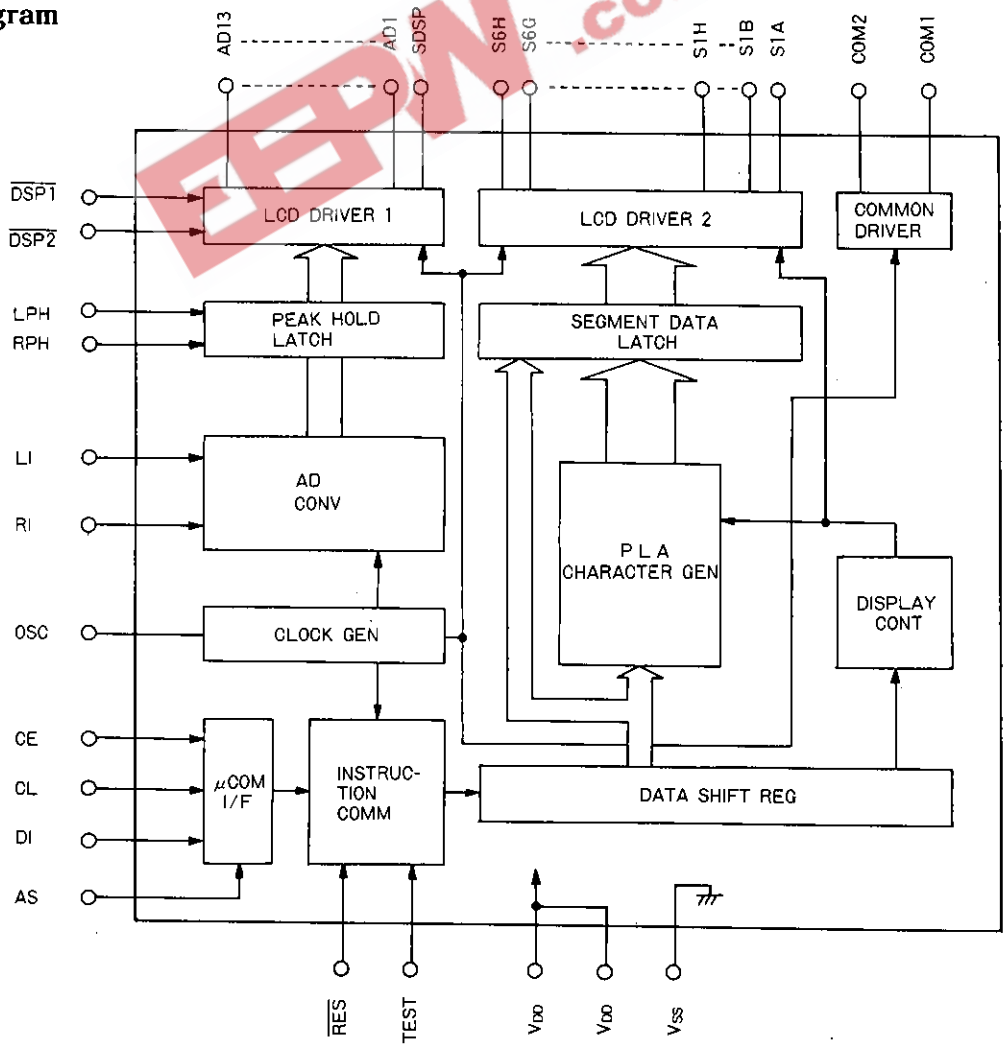


τVDD: Time constant of the power-on signal rise
τ$\overline{RES}$: Time constant of the $\overline{RES}$ pin signal rise

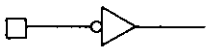
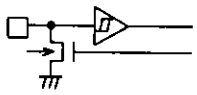
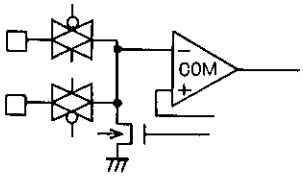
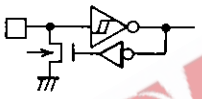
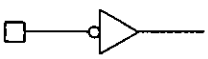
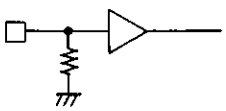
Set the CR time constant or input a signal to the $\overline{RES}$ pin so that the τVDD ≦ τ$\overline{RES}$ is satisfied.

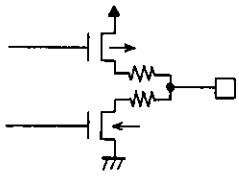
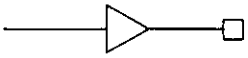
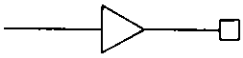
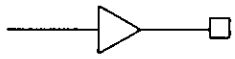
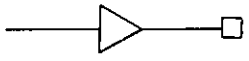


Block diagram



Pin description

Pin name	Pin No.	Pin design	Description
$\overline{DSP1}$ $\overline{DSP2}$	36 38		• Input pin used for direct (external input) display The segment drive signals are output from the SDSP pin. COM1 : $\overline{DSP1}$, COM2 : $\overline{DSP2}$
LPH RPH	27 28		• CR connection pins for determining the reset time of the peak hold circuit for level meter display.
LI RI	37 39		• Input pin for AD converter. Full scale: (31/48)V_{DD}
OSC	29		• CR connection pin for oscillation
CE CL DI	33 34 35		• Serial data input pin. CE: Chip enable. CL: Synchronous clock. DI: Input serial data
AS	30		• Address select input pin. The signal inputs to this pin are meaningful when the two LC7584N chips are used. AS pin: L / H Address A0: 0 / 1 Address A1: 0 / 0 Address A2: 1 / 1 Address A3: 0 / 0 HEX CODE: 4 / 5
$\overline{RES}$	32		• Reset signal input pin. If this pin becomes active, the LSI will be initialized and all the LCD segments are then forcibly turned off. To turn on the LCD segments, commands are transmitted to the LC7584N from a microcomputer.
TEST	40		• Left open or connected to the V_{SS} level.

Pin name	Pin No.	Pin design	Description
V_{DD}	31 73		• Voltage supply pin. Applies voltage in the range between 4.0V and 5.5V. If the on-chip AD converter is not used, it is possible to decrease down to 3.0V.
Vss	26		• Ground pin.
COM1 COM2	41 42		• LCD common driver pins. Frame frequency = fosc/1024 Hz.
S1A to S1H	43 to 50		• LCD segment driver pins: <for the first display digit>
S2A to S2H	51 to 58		• LCD segment driver pins: <for the second display digit>
S3A to S3H	59 to 66		• LCD segment driver pins: <for the third display digit>
S4A to S4H	67 to 75		• LCD segment driver pins: <for the fourth display digit>
S5A to S5E S5F to S5H	76 to 80 1 to 3		• LCD segment driver pins: <for the fifth display digit>
S6A to S6H	4 to 11		• LCD segment driver pins: <for the sixth display digit>
SDSP	12		• LCD segment driver pin: <direct ($\overline{DSP1}$ and $\overline{DSP2}$) display>
AD1 to AD13	13 to 25		• LCD segment drivers: <AD converter level display>. AD1: lowest level. AD13: highest level.

Control data (serial data command) format

Command list

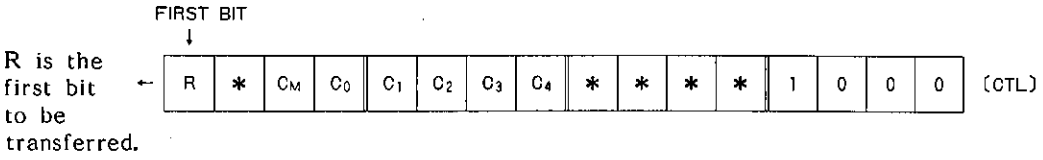
Command type	Function	Serial data				(HEX)
Control [CTL]	Initializes the LSI. This command is required each time the LSI is powered on.	1	0	0	0	1
Display 1 [DP1]	Turns off the drivers of a specified digit and the ADC drivers.	0	1	0	0	2
Display 2 [DP2]	Turns on the drivers of a specified digit and the ADC drivers.	1	1	0	0	3
Data 1 [DT1]	Updates the content of a specified digit: Via the PLA character generator.	0	0	1	0	4
Data 2 [DT2]	Updates the contents of all the digits: Via the PLA character generator.	1	0	1	0	5
Data 3 [DT3]	Updates the content of a specified digit: Any display data. Resets the data 2 inhibit flag.	0	1	1	0	6
Data 4 [DT4]	Updates the content of a specified digit: Any display data. Sets the data 2 inhibit flag.	1	1	1	0	7

Command processing time

Command	Processing time (CE : ↓ → Processing starts after this.)
Control [CTL]	$2 \times \frac{1}{fosc}$ s (12.5 µs : fosc = 160KHz)
Display 1 [DP1]	$10 \times \frac{1}{fosc}$ s (62.5 µs : ↑)
Display 2 [DP2]	$10 \times \frac{1}{fosc}$ s (62.5 µs : ↑)
Data 1 [DT1]	$10 \times \frac{1}{fosc}$ s (62.5 µs : ↑)
Data 2 [DT2]	$22 \times \frac{1}{fosc}$ s (137.5 µs : ↑)
Data 3 [DT3]	$10 \times \frac{1}{fosc}$ s (62.5 µs : ↑)
Data 4 [DT4]	$10 \times \frac{1}{fosc}$ s (62.5 µs : ↑)

* The next command should not be sent to the LSI from a microcomputer until the current command processing is complete. The transfer of the next command would cause an operational error in such a situation.

(1) Control --- <Initializes the LSI. This command is required each time the LSI is powered on.>



R : Resets the LSI. This serial data places the AD converter and the LCD drivers in halt mode operation.
0 → Reset; Release
1 → Reset; Initialization (ADC display, direct display and all display digits; OFF)

(The LSI can be also initialized by inputting an 'L' level signal to the $\overline{RES}$ pin (active low). However, the serial command data should be used to release the LSI from the initialization mode.)

C_M : Selects a 1/2 divider resistance value of the LCD common drivers (COM1, COM2) from the following two values.
0 → 2 kΩ
1 → 50 kΩ

Co : Controls the peak hold circuit used for ADC level meter display.
0 → Inactivates the peak hold circuit.
1 → Activates the peak hold circuit.

C_1 and C_2 : Selects an ADC display mode from the following four operation modes:
0 0 → Places the ADC in halt operation mode.
1 0 → Selects the 26-ladder x 1 channel linear scale display operation mode (with peak hold circuit disabled).
0 1 → Selects the 13-ladder x 2 channels log scale display operation mode.
1 1 → Selects the 13-ladder x 2 channels linear scale display operation mode.

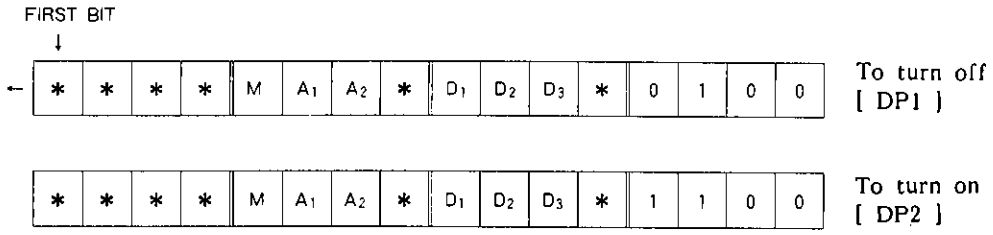
※ If the 1 channel operation mode is selected, the same signal should be input to both of the LI and RI pins.
If the 2 channel operation mode is selected, two independent signals should be input to the LI and RI pins separately.

C_3 and C_4 : Selects an ADC display update cycle from the following four values.
0 0 → 2^{10}/fosc s (6.7 ms ; fosc = 160kHz)
1 0 → 2^{13}/fosc s (50 ms ; fosc = 160kHz)
0 1 → 2^{14}/fosc s (100 ms ; fosc = 160kHz)
1 1 → 2^{15}/fosc s (200 ms ; fosc = 160kHz)

*: Indicates that these bits can be set to 'H' or 'L'.
※: AD converter halt : LI and RI pins are pulled down to the Vss level. AD1 to AD13 pins (segment pins) are also pulled down to the Vss level.

LCD driver halt : S1A to S6H, and SDSP (segment pins) pins ; Vss.
COM1 and COM2 ; Vss.

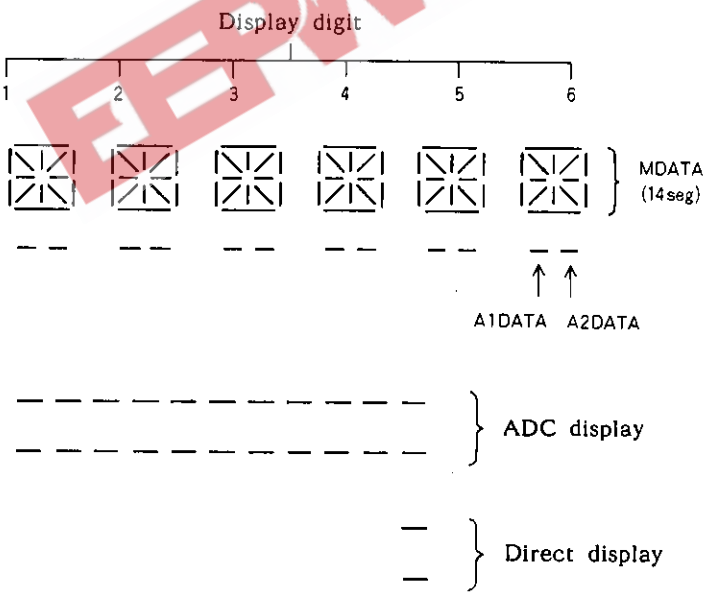
(2) Display --- <Turns ON/OFF the LCD drivers of a specified digit and the ADC display drivers>



M, A_1, A_2 : Specifies the type(s) of data (MDATA, ADATA).
- M → 1: MDATA
- A_1 → 1: A_1DATA
- A_2 → 1: A_2DATA

D_1, D_2, D_3 : Specifies a display digit to be turned ON/OFF.
- 0 0 0 → ADC display
- 1 0 0 → The first display digit
- 0 1 1 → The sixth display digit
- 1 1 1 → All the display digits (first to sixth digits)

*: indicates that these bits can be set to 'H' or 'L'.

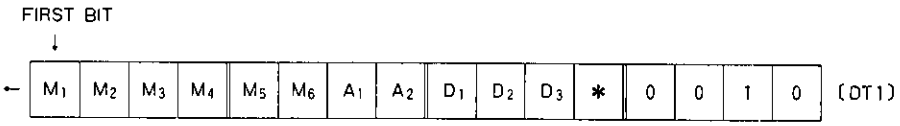


※ MDATA : Characters, symbols and so on displayed via the PLA character generator.

A_1, A_2 DATA : Any display data.

After reset : The [DP2] command should be executed in order that the LSI can be released from reset mode. This does not apply to the direct display mode.

(3) Data 1 --- <Updates the display data of a specified digit: Via the PLA character generator>



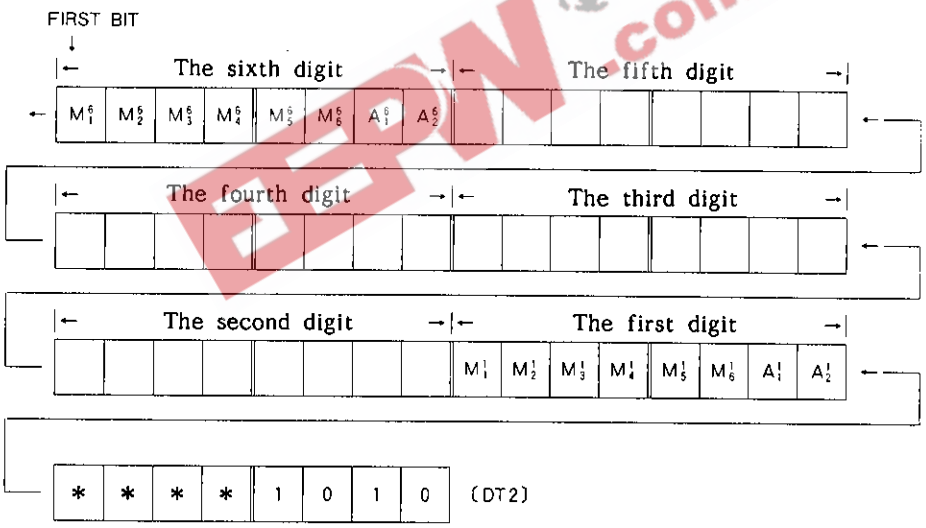
M_1 to M_6 : Input data (MDATA) to the PLA character generator. It enables the character generator to generate up to 64 kinds of characters, symbols and so on. Each display data requires 14 segments.

A_1 and A_2 : Additional data directly from a microcomputer (memory), not via the PLA character generator. That is, any segment data can be sent from the microcomputer as additional data when these bits are set. (A_1, A_2 DATA)

D_1 to D_3 : Specifies the digit of which data is updated.

0 0 0 → No update
1 0 0 → The first digit data
⋮ ⋮
0 1 1 → The sixth (last) digit data
1 1 1 → All of the digits will be updated.

(4) Data 2 ---<Updates the display data of all the digits: Via the PLA character generator>



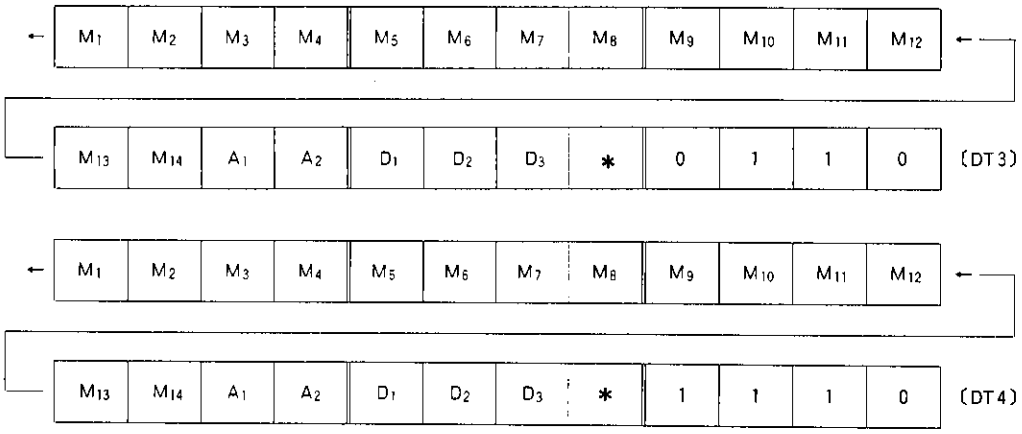
M_1^n to M_6^n : Input data (MDATA) to the PLA character generator. It enables the character generator to generate up to 64 kinds of characters, symbols and so on. Each display data requires 14 segments.

A_1^n and A_2^n : Additional data. These bits are used together with the preceding six bits (M1 to M6) to generate any segment pattern. Note that these two segment control bits are directly output from a microcomputer and then used to drive the A_1DATA and A_2DATA segment directly while the preceding six bits are input to the PLA character generator.

※ If a certain digit has been masked by the data 4 [DT4] command, the display data of the digit cannot be updated. Note that the DT4 command has the function to set the data 2 inhibit flag.

* : Indicates that these bits can be set to 'H' or 'L'.

(5) Data 3 and 4 commands ---<Updates the display data of a specified digit : any display data>



M_1 to M_{14} :Display data directly used to drive segments to generate any segment pattern. These bits are not input to the PLA character generator. (MDATA)

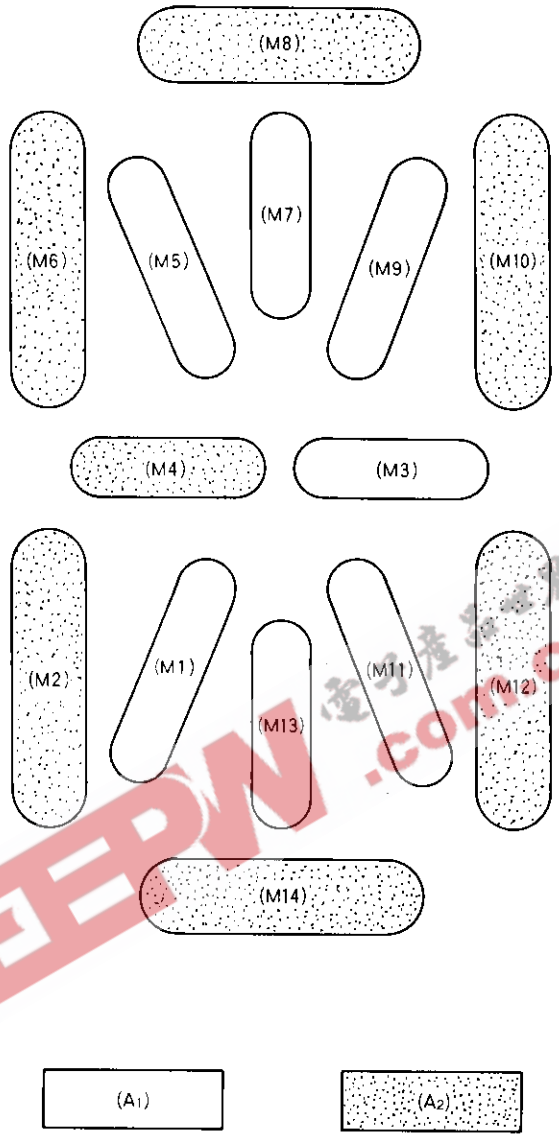
A_1 and A_2 : Additional data. These two bits are directly used to drive segments to generate any segment pattern together with bits M1 to M16. (A_1 and A_2 DATA)

D_1 to D_3 :Specifies the digit of which display data is updated.

0 0 0 → No update
1 0 0 → The first digit
⋮ ⋮
0 1 1 → The sixth digit
1 1 1 → All the digits

※ The [DT3] command has the function to reset the DATA 2 inhibit flag.
The [DT4] command has the function to set the DATA 2 inhibit flag.
The [DT3] and [DT4] commands are used to set or reset the inhibit flag which corresponds to the digit specified by D_1 to D_3.
If the flag controlling a certain digit has been set and the [DT2] command is executed, the display data of that digit is not updated.
In this case, the display data specified by the [DT3] or [DT4] command remains unchanged.
Note that the [DT1] command can be used to update the current display data of any digit, irrespectively of flags.
When the LSI is reset, the data 2 inhibit flag will be also reset.

LCD panel layout <fig 1>

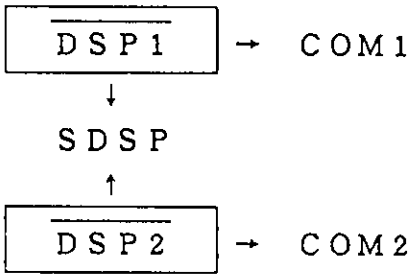


nth digit (n: 1 to 6)

Pin name	SnA	SnB	SnC	SnD	SnE	SnF	SnG	SnH
COM1	M2	M4	M6	M8	M10	M12	M14	A_2
COM2	M1	M3	M5	M7	M9	M11	M13	A_1

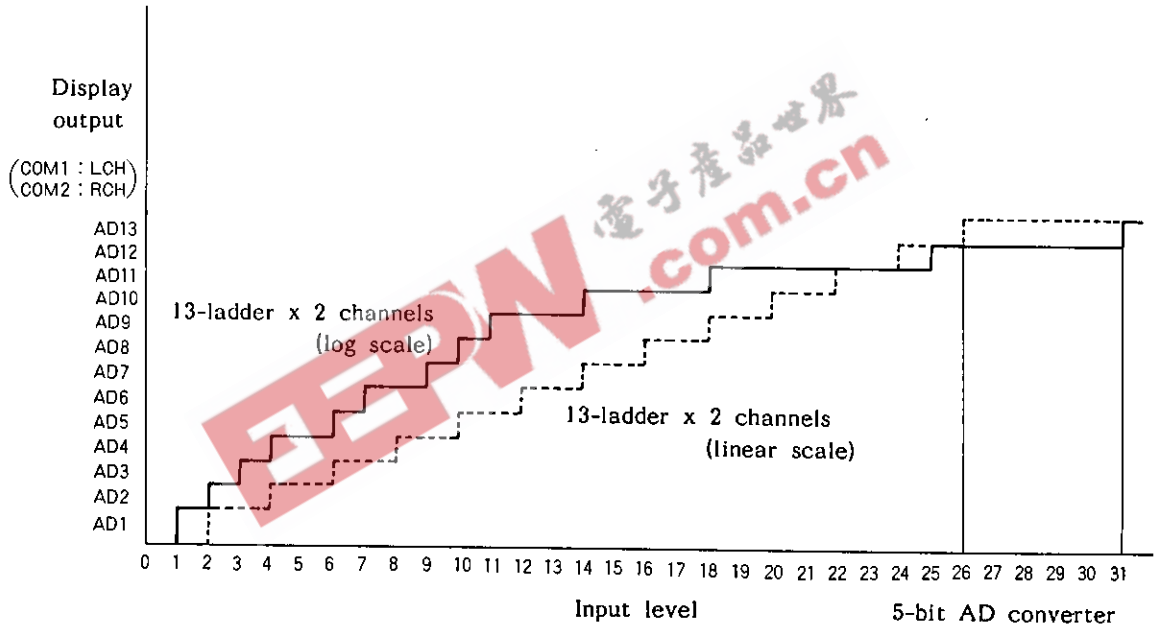
LCD common connection

(1) Direct display ($\overline{DSP1}$, $\overline{DSP2}$)

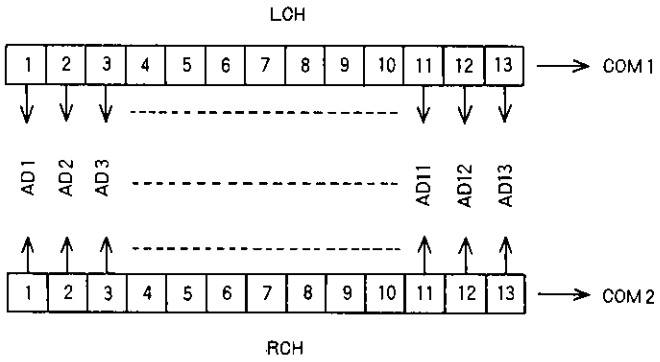


(2) ADC display mode

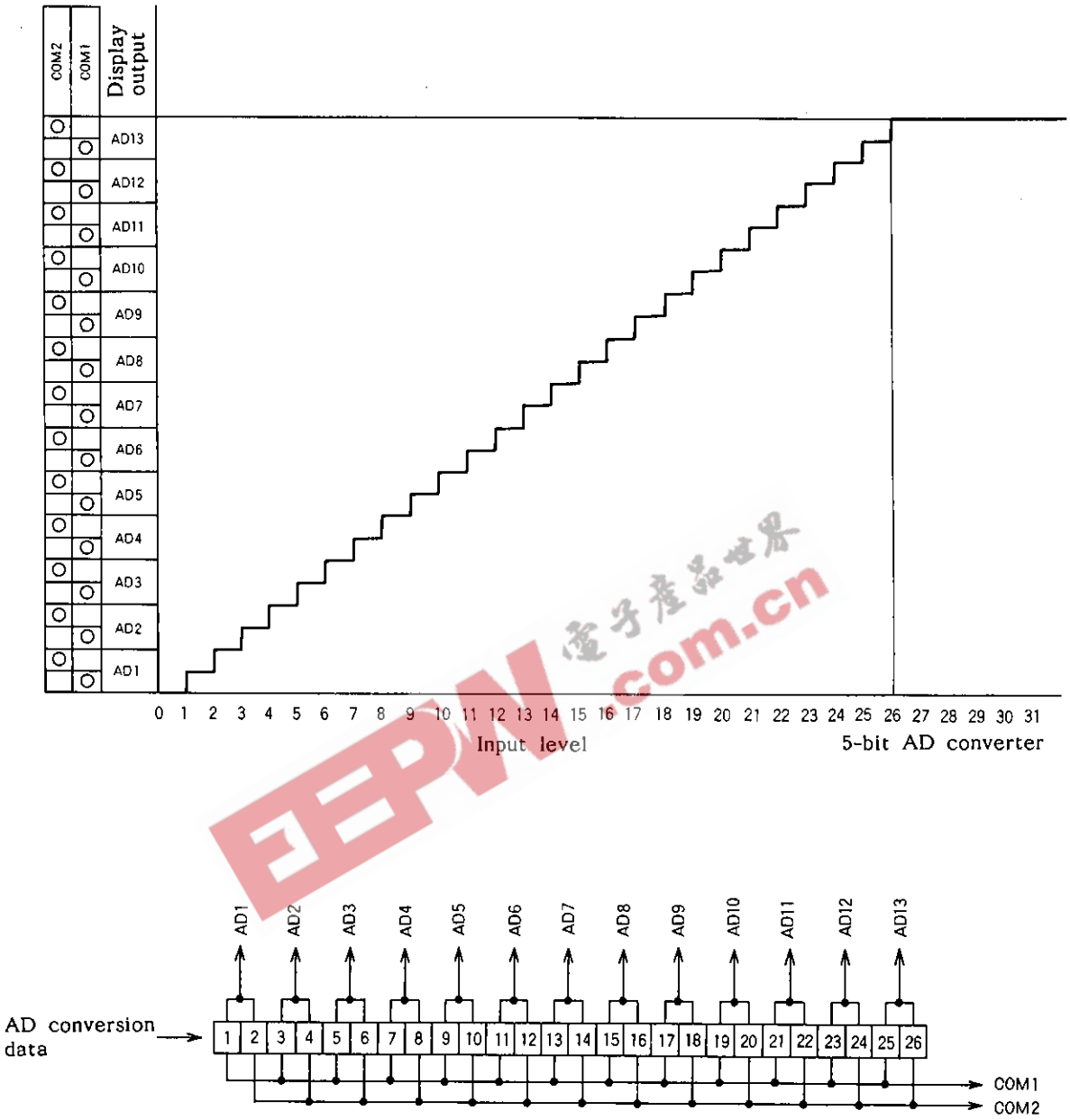
• 2-channel (stereo) display mode (Only the data from one of the two is displayed) <fig 2>



COMMON connection



• One-channel (monaural) display mode <fig 3>



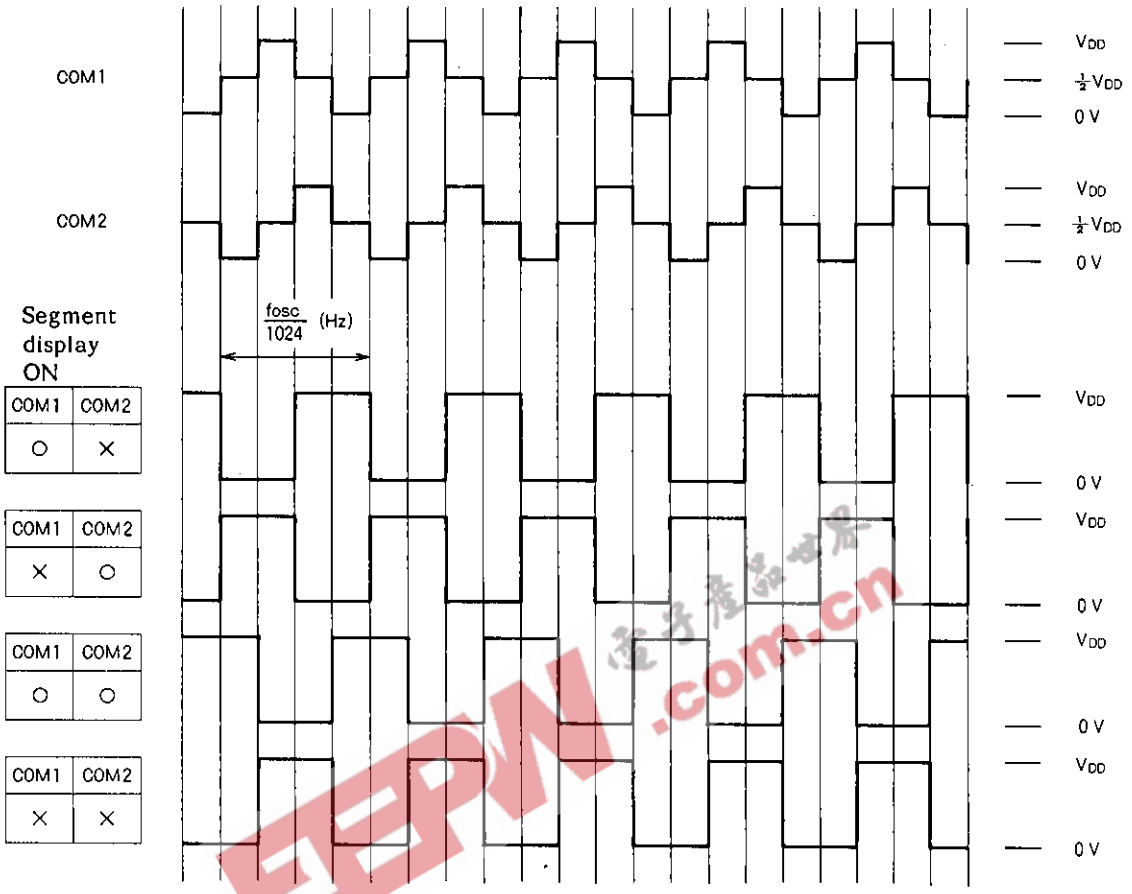
When the monaural display operation is employed, the RI and LI pins should be wired together.

※ AD converter reference voltage (laboratory value); Viref

$$Viref = \frac{1}{3} V_{DD} (D_4 + \frac{1}{2} D_3 + \frac{1}{4} D_2 + \frac{1}{8} D_1 + \frac{1}{16} D_0)$$

D_0 to D_4 : ADC 5 bits D_0 ; LSB

• LCD driver output signal waveforms <fig 4>



COM1	COM2
○	×

COM1	COM2
×	○

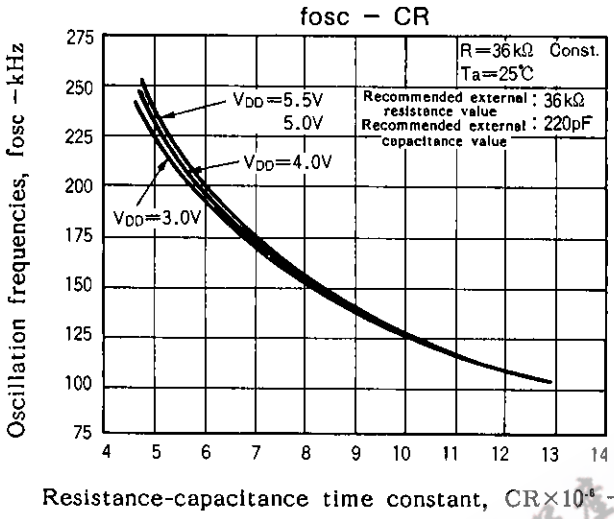
COM1	COM2
○	○

COM1	COM2
×	×

Oscillation frequency

The oscillation frequency can be determined based on the values in the figure below.

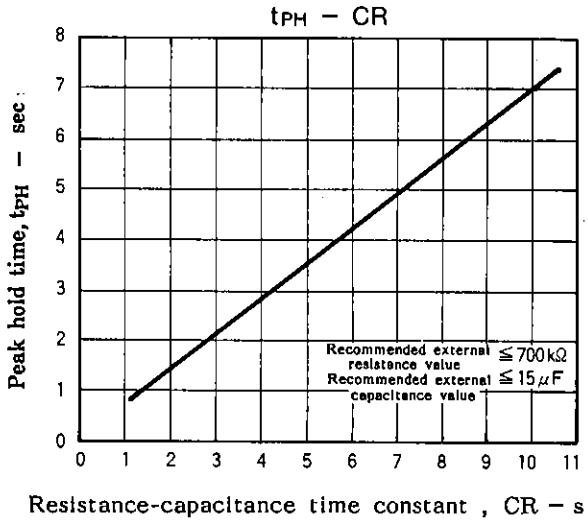
<fig 5> Oscillation frequencies of the OSC pin and CR time constants



Peak hold time (LPH/RPH)

The peak hold time can be determined based on the following values in the figure below.

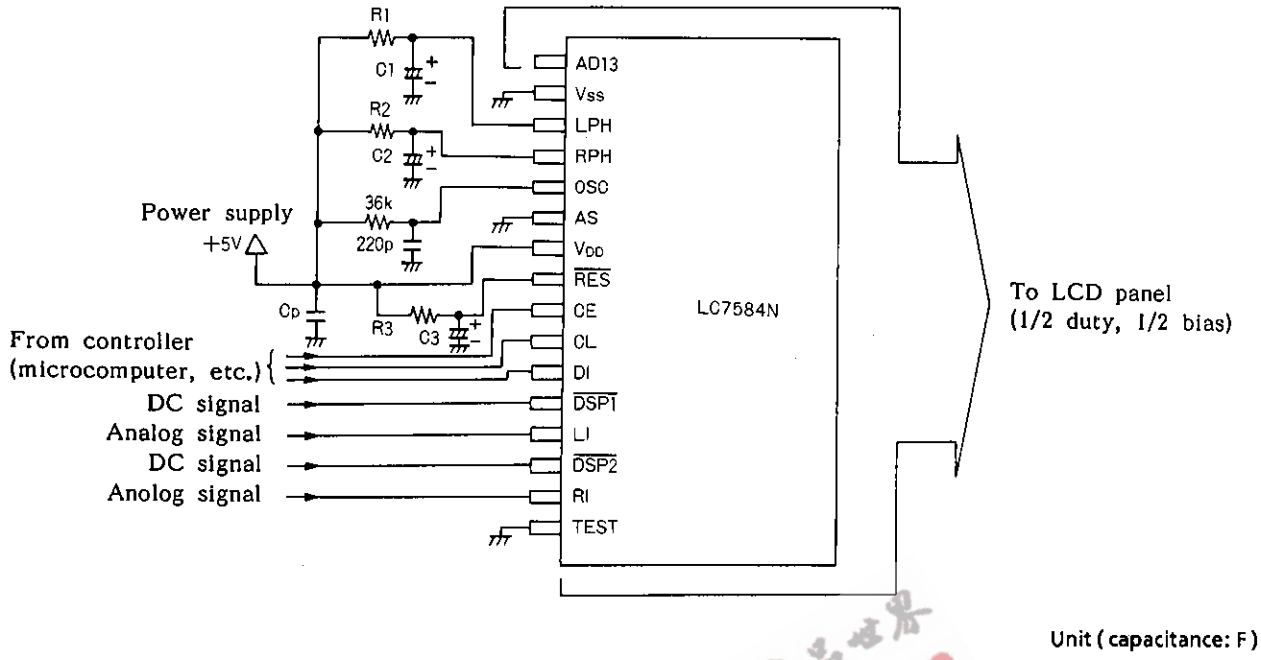
<fig 6> Peak hold times and CR time constants



* Peak hold time
tph (laboratory value)
$t_{PH} \simeq 0.69 \times CR$(s)

[Example]
If R=430 kΩ
and C=10 μF
are selected,
the peak hold
time will be
about 3 seconds.

Sample application circuit

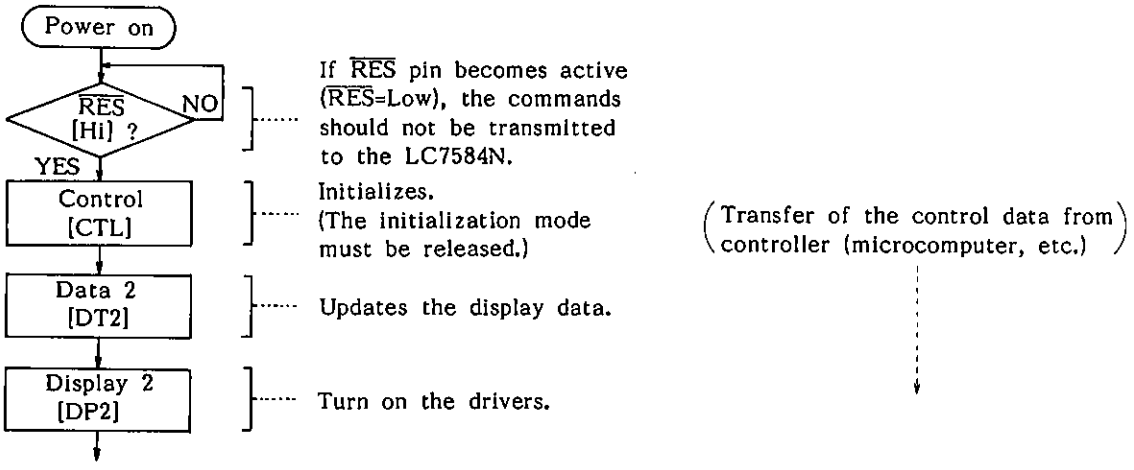


Unit (capacitance: F)

*1. If R1=R2=430kΩ and C1=C2=10μF are selected, the peak hold time will be about 3 seconds.
*2. R3 and C3 are time constant for reset. The time constant can be determined by the characteristic of power-on signal rise. (P_{RES}>1μS)
*3. Cp is a bypass capacitor.

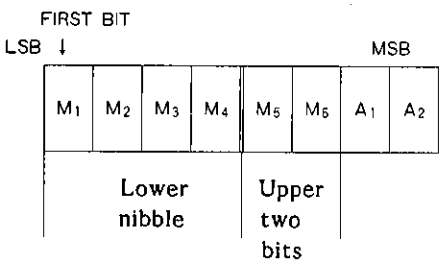
Example of using control data

From power-on to turning-on of the drivers.

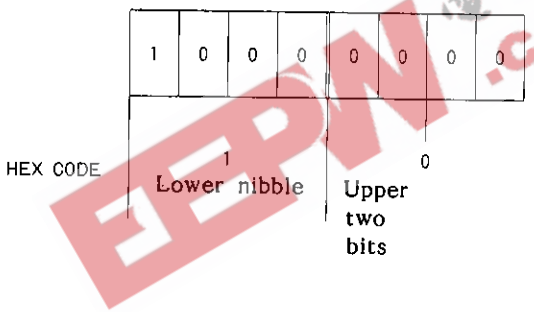


PLA (character generator) conversion code

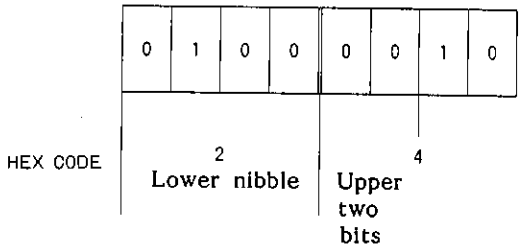
The serial command data [DT1] or [DT2] can be used to enable up to 64 kinds of characters, symbols and so on to be displayed on the LCD panel via the PLA character generator. (See the LCD panel layout shown in <fig 1>)



Example 1) Character 'A' is to be displayed.

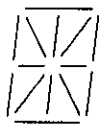


Example 2) Character 'B' is displayed and additional data A_1 is also lit up.



PLA (character generator) conversion code table

Characters (1)

No	Display character	Display segment pattern	HEX CODE Upper two bits	HEX CODE Lower nibble
0	Blank		0	0
1	A		0	1
2	B		0	2
3	C		0	3
4	D		0	4
5	E		0	5
6	F		0	6
7	G		0	7

No	Display character	Display segment pattern	HEX CODE
8	H		0 8
9	I		0 9
10	J		0 A
11	K		0 B
12	L		0 C
13	M		0 D
14	N		0 E
15	O		0 F

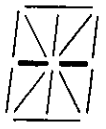
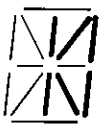
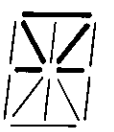
Characters (2) Numbers

No.	Display character	Display segment pattern	HEX CODE Upper two bits	HEX CODE Lower nibble
16	P		1	0
17	Q		1	1
18	R		1	2
19	S		1	3
20	T		1	4
21	U		1	5
22	V		1	6
23	W		1	7

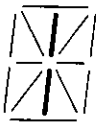
No.	Display character	Display segment pattern	HEX CODE
24	X		1 8
25	Y		1 9
26	Z		1 A
27	0		1 B
28	1		1 C
29	2		1 D
30	3		1 E
31	4		1 F

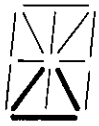
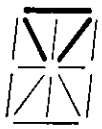
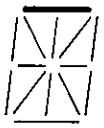
Numbers and Symbols (1)

No	Display character	Display segment pattern	HEX CODE Upper two bits	HEX CODE Lower nibble
32	5		2	0
33	6		2	1
34	7		2	2
35	8		2	3
36	9		2	4
37			2	5
38			2	6
39			2	7

No	Display character	Display segment pattern	HEX CODE
40			2 8
41			2 9
42			2 A
43			2 B
44			2 C
45			2 D
46			2 E
47			2 F

Symbols (2)

No.	Display character	Display segment pattern	HEX CODE
48			3 0
49			3 1
50			3 2
51			3 3
52			3 4
53	Lower-case character d		3 5
54	Lower-case character h		3 6
55	Lower-case character r		3 7

No.	Display character	Display segment pattern	HEX CODE
56			3 8
57			3 9
58			3 A
59			3 B
60			3 C
61			3 D
62			3 E
63			3 F