Ordering number : EN5330

CMOS LSI

LC75372E

Electronic Volume Control for Car Stereo Systems

Overview

The LC75372E is an electronic volume control that can implement volume, balance, fader, bass/treble, loudness, input switching, and input level control functions with a minimal number of external components.

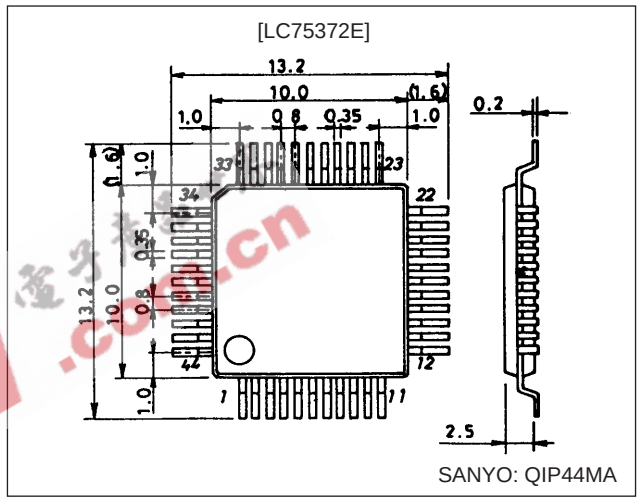
Features

- Volume: Provides 81 positions, from 0 dB to –79 dB (in 1-dB steps) and –∞. A balance function can be implemented by controlling the left and right channels independently.
- Fader: This function can attenuate either the rear or the front outputs over 16 positions. (From 0 to –20 dB in 2-dB steps, from –20 to –25 dB in one 5-dB step, from –25 to –45 dB in 10-dB steps, –60 dB, and –∞.)
- Bass/treble: Forms an NF-type tone control circuit (LUX type) with the addition of external capacitors. The base and treble controls each have 15 positions.
- Loudness: The volume resistor ladders are tapped starting at the –20-dB position. A loudness function can be implemented by adding external RC circuits at these taps.
- The signal can be selected from one of three inputs for each of the left and right channels. The input signals can be amplified from 0 to +18 dB in 6-dB steps.
- On-chip buffer amplifiers for a minimum of external components.
- Minimal switching noise due to fabrication in a silicon-gate CMOS process.
- Built-in reference voltage generation circuit
- Serial data input: Supports CCB format communication with the system controller.

Package Dimensions

unit: mm

3148-QFP44MA



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	260	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

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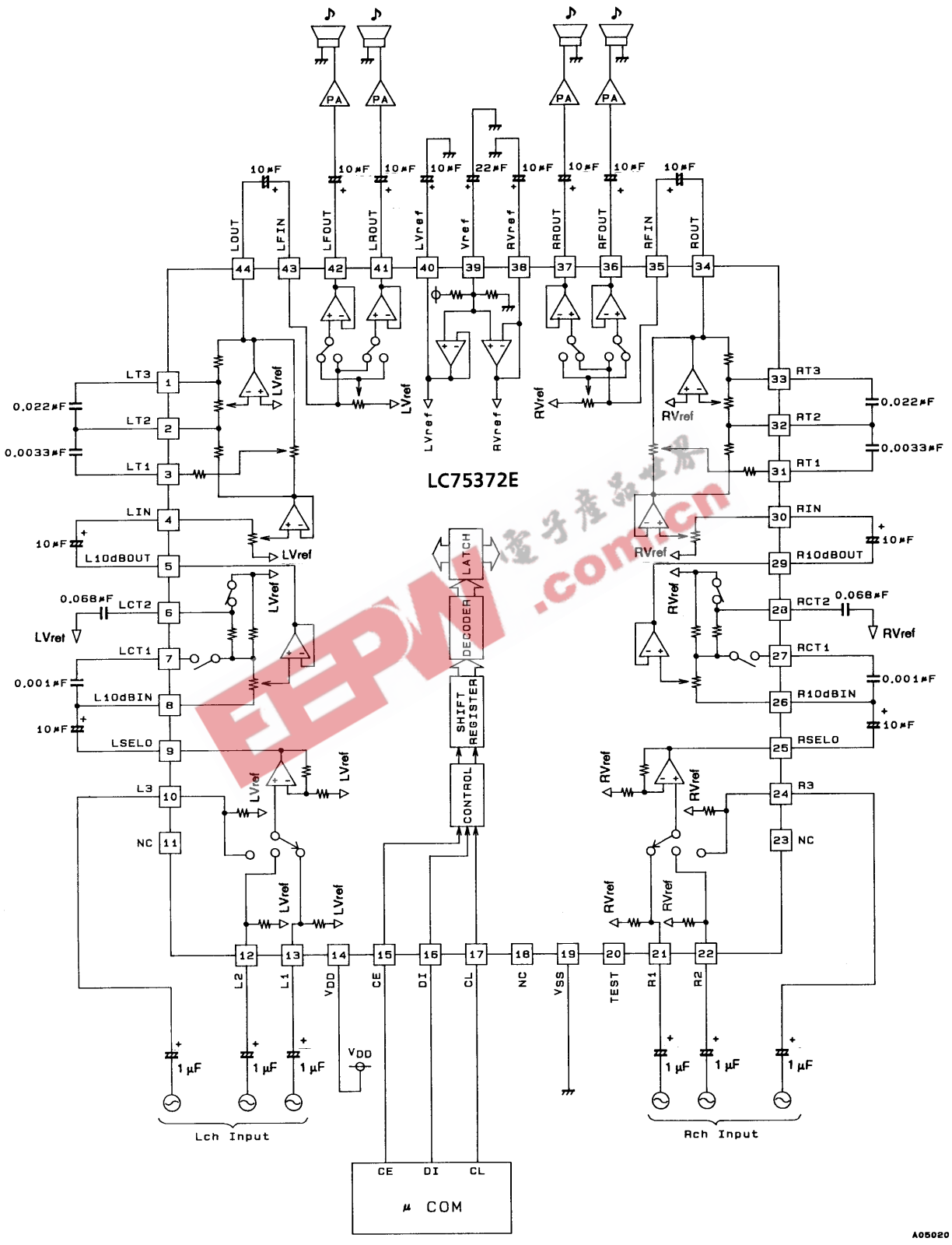
Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	6.0		10.0	V
Input high-level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low-level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LIN, RIN, LFIN, RFIN, L1 to L3, R1 to R3	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1			µs
Setup time	tsetup	CL, DI, CE	1			µs
Hold time	thold	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 9 V, V_{SS} = 0 V

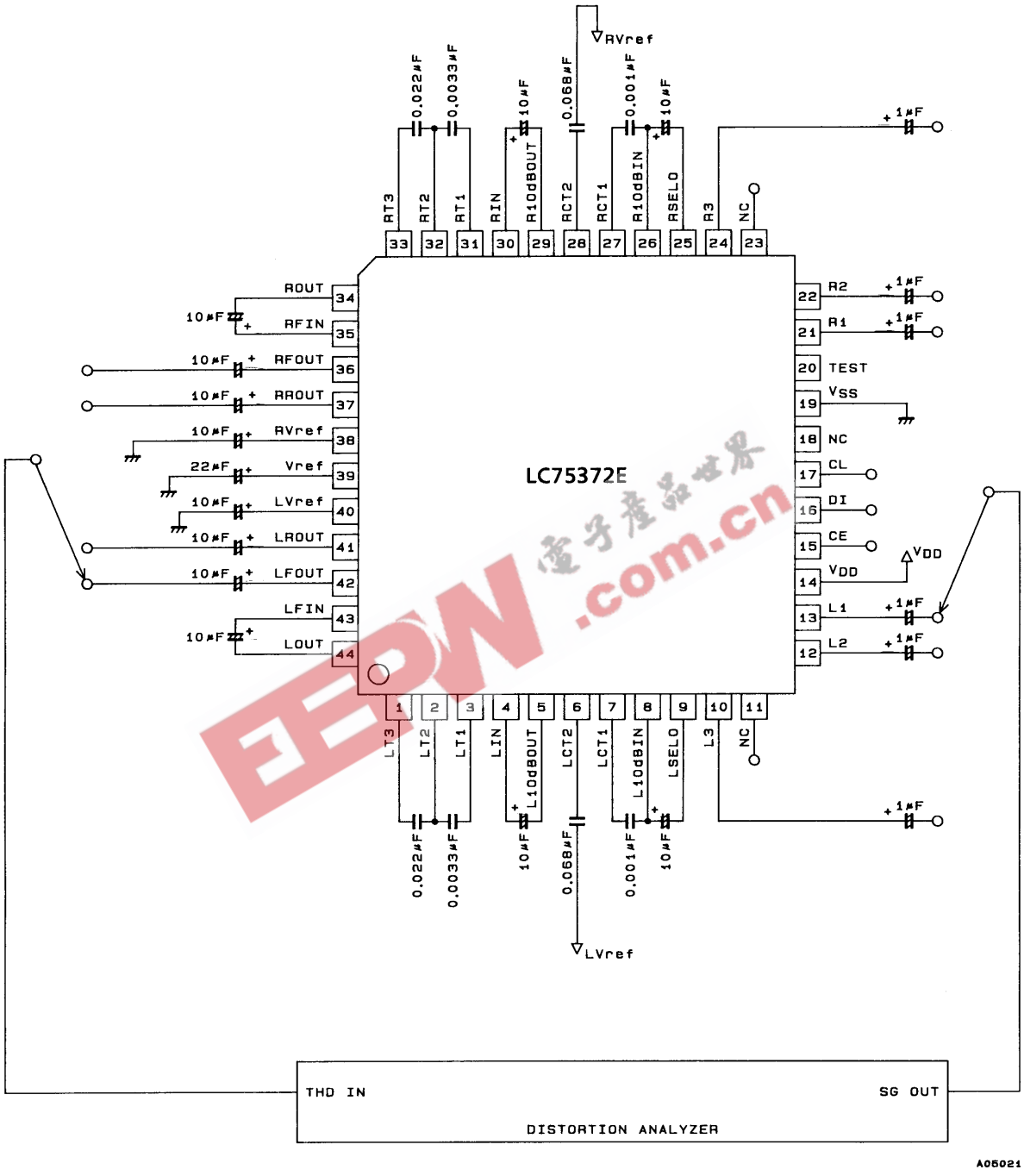
Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	Rin	L1 to L3, R1 to R3	30	50	70	kΩ
Minimum input gain	Gin min		–2	0	+2	dB
Maximum input gain	Gin max		+16.0	+18.0	+20.0	dB
Step resolution	Gstep			+6.0		dB
[Volume Control Block]						
Input resistance	Rv10	L10dBIN, R10dBIN: 10-dB steps, loudness off	30	50	70	kΩ
	Rv1	LIN, RIN: 1-dB steps	12	20	28	kΩ
Step resolution	ATstep			1		dB
Step error	ATerr	step = 0 to –20 dB	–1	0	+1	dB
		step = –20 to –50 dB	–3	0	+3	dB
[Fader Volume Block]						
Input resistance	Rfed	LFIN, RFIN	12	20	28	kΩ
Step resolution	ATstep	step = 0 to –20 dB		2		dB
		step = –20 to –25 dB		5		dB
		step = –25 to –45 dB		10		dB
Step error	ATerr	step = 0 to –45 dB	–2	0	+2	dB
		step = –45 to –60 dB	–3	0	+3	dB
Output load resistance	R_L	LFOUT, LROUT, RFOUT, RROUT	10			kΩ
[Bass/Treble Control Block]						
Bass control range	Gbass	Max. boost/cut	±9	±10.5	±12	dB
Treble control range	Gtre	Max. boost/cut	±8	±10.5	±13	dB
[Overall Characteristics]						
Total harmonic distortion	THD (1)	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall		0.045		%
	THD (2)	V_{IN} = 1 Vrms, f = 20 kHz, all settings flat overall		0.040		%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, all settings flat overall, Rg = 1 kΩ		80		dB
Output at maximum attenuation	V_O min	V_{IN} = 1 Vrms, f = 1 kHz, main volume at –∞		–78		dB
		V_{IN} = 1 Vrms, f = 1 kHz, main volume at –∞, INMUTE		–81		dB
Output noise voltage	V_N (1)	All settings flat overall (IHF-A), Rg = 1 kΩ		15	30	µV
	V_N (2)	All settings flat overall (DIN-AUDIO), Rg = 1 kΩ		20	40	µV
Current drain	I_{DD}	V_{DD} – V_{SS} = 10 V		25	30	mA
Input high-level current	I_{IH}	CL, DI, CE: V_{IN} = 9 V			10	µA
Input low-level current	I_{IL}	CL, DI, CE: V_{IN} = 0 V	–10			µA
Maximum input level	V_{CL}	All settings flat overall, measurement point; fader output THD = 1%, RL = 10 KΩ		2		Vrms

Equivalent Circuit Block Diagram and Sample Application Circuit

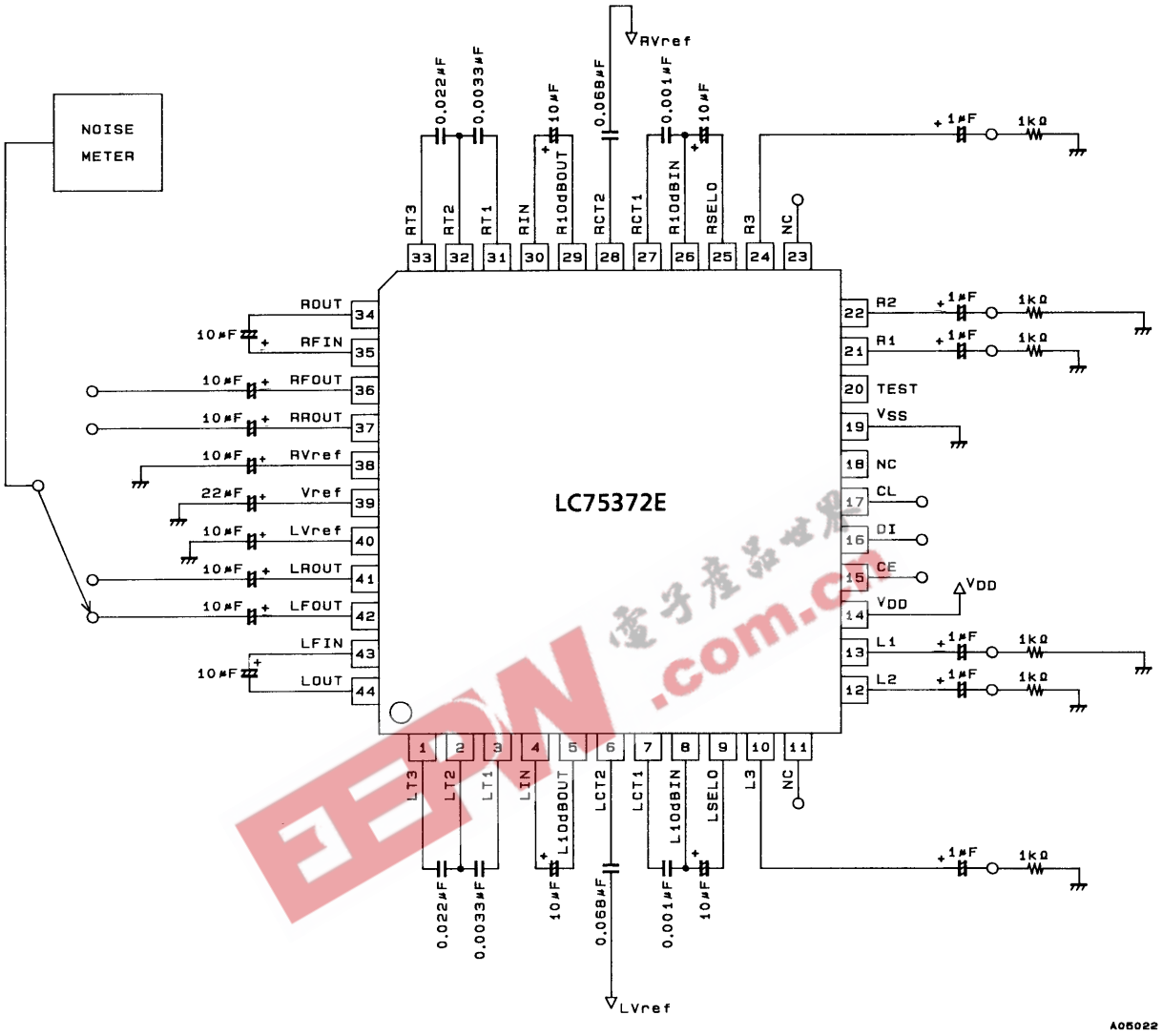


Electrical Characteristics Test Circuits

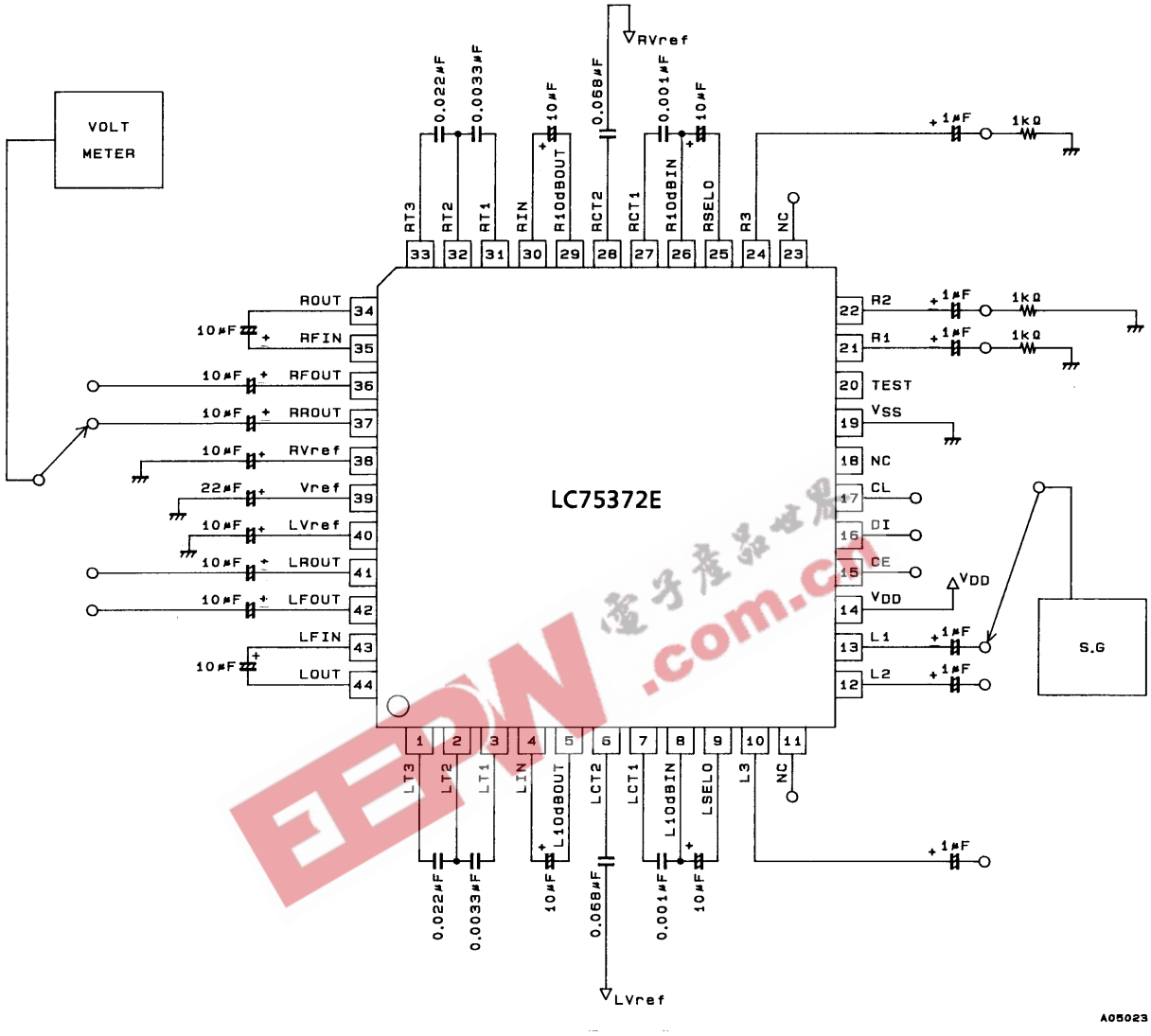
1. Total harmonic distortion



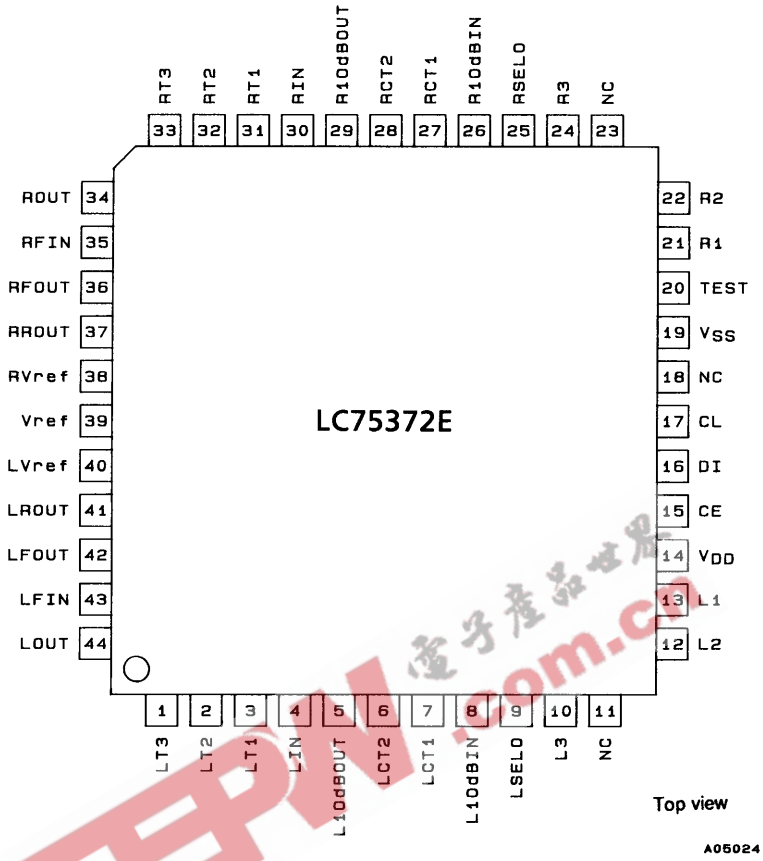
2. Output noise voltage



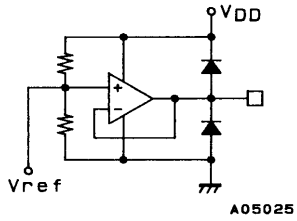
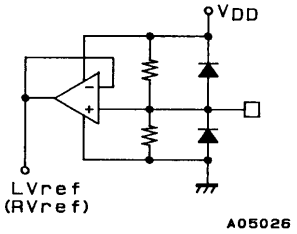
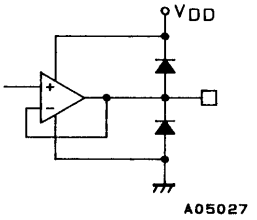
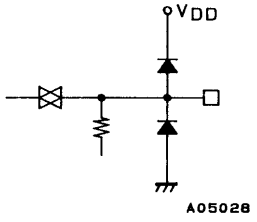
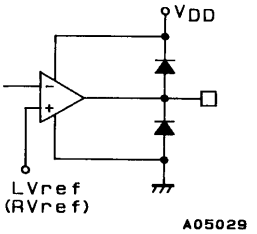
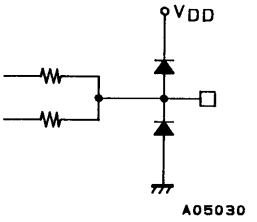
3. Crosstalk


VOLT METER
LC75372E
RVref
LVref
Vref
VDD
S.G
ROUT
RFIN
RFOUT
RROUT
LROUT
LFOUT
LFIN
LOUT
R2
R1
TEST
VSS
NC
CL
DI
CE
VDD
L1
L2
RT3
RT2
RT1
RIN
R10dBOUT
RCT2
RCT1
R10dBIN
RSELO
R3
NC
LT3
LT2
LT1
LIN
L10dBOUT
LCT2
LCT1
L10dBIN
LSELO
L3
NC
0.022μF
0.0033μF
10μF
0.068μF
0.001μF
1μF
1kΩ
22μF
A05023

Pin Assignment

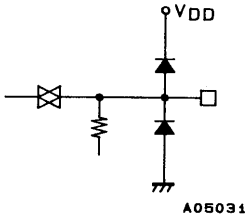
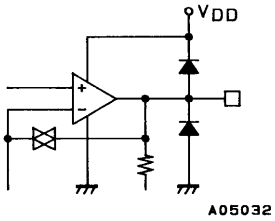
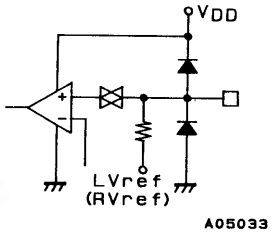
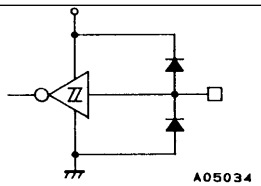


Pin Functions

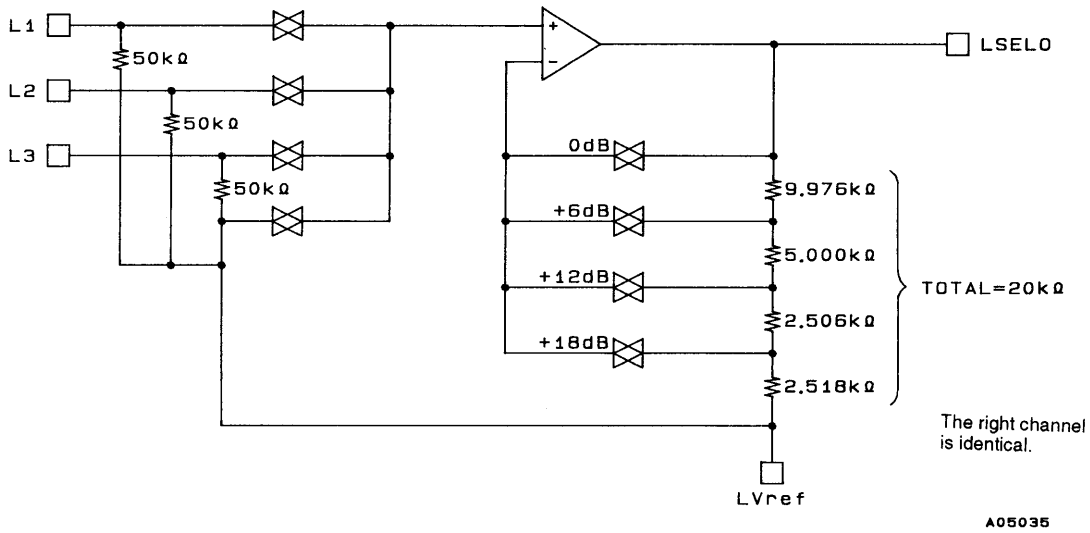
Pin No.	Symbol	Equivalent I/O circuit	Function
40 38	LVref RVref	• Common pins for the main volume block, fader volume block, tone block, gain control block, and input switching block. • Since the capacitors connected between LVref/RVref and V_{SS} become the residual resistance when the volume control is at maximum attenuation, the values of these capacitors must be chosen carefully. • The applied voltage must never exceed V_{DD}.	
39	Vref	0.488 V_{DD} voltage generation block. A capacitor must be connected between Vref and V_{SS} to suppress power supply ripple.	
41 42 37 36	LROUT LFOUT RROUT RFOUT	• Fader outputs. The front and rear systems can be attenuated independently. The amount of attenuation is the same in the left and right channels. • Low impedance operational amplifier outputs	
43 35	LFIN RFIN	• Fader inputs • Must be driven from low-impedance circuits.	
44 34	LOUT ROUT	Tone control outputs	
3 2 1 31 32 33	LT1 LT2 LT3 RT1 RT2 RT3	Connections for the bass and treble compensation capacitors for the tone control circuit Connect high-band compensation capacitors between T1 and T2. Connect low-band compensation capacitors between T2 and T3.	
7 6 27 28	LCT1 LCT2 RCT1 RCT2	Loudness pins. Connect high-band compensation capacitors between LCT1/RCT1 and L10dBIN/R10dBIN, and connect low-band compensation capacitors between LCT2/RCT2 and LVref/RVref.	

Continued on next page.

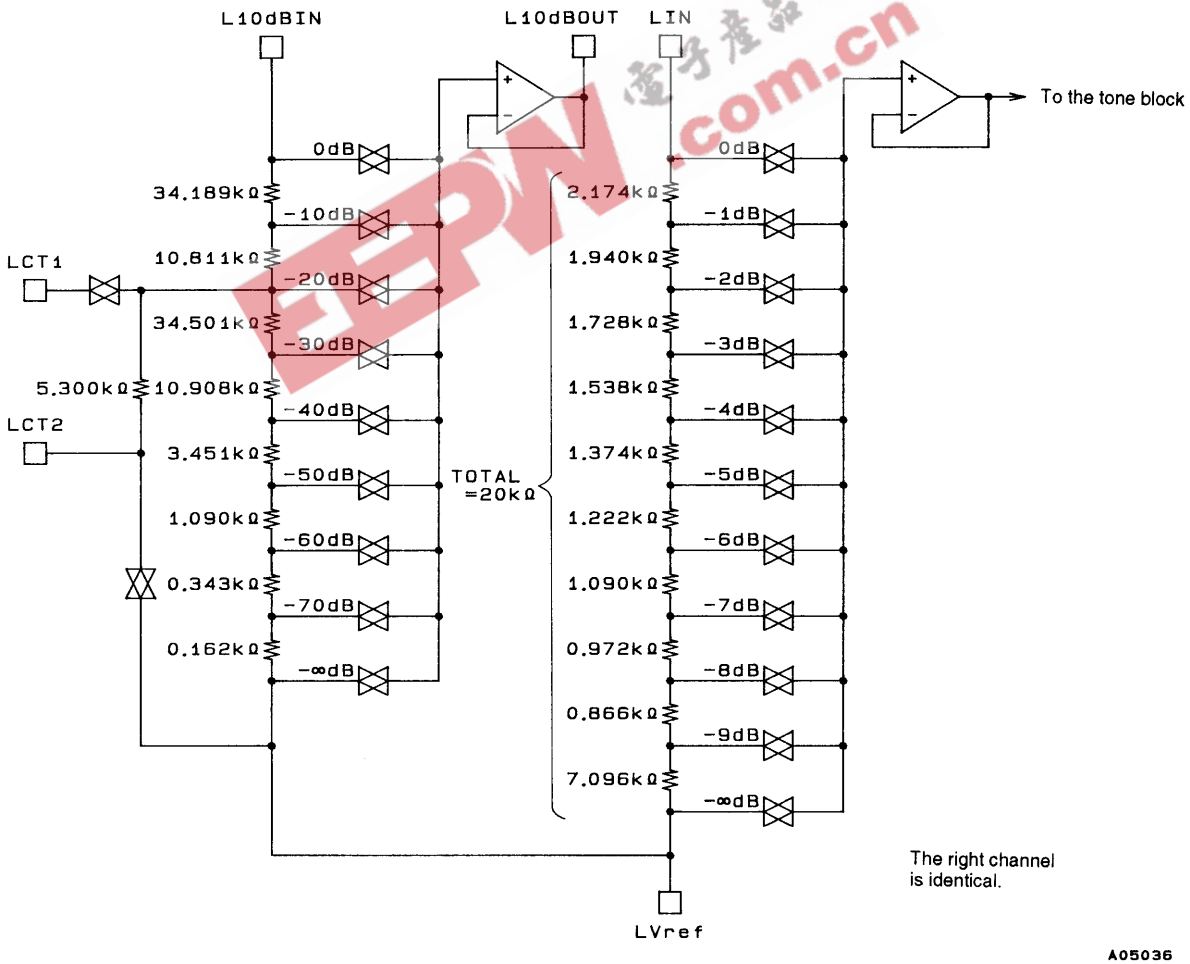
Continued from preceding page.

Pin No.	Symbol	Equivalent I/O circuit	Function
8 26	L10dBIN R10dBIN	• 10-dB volume control inputs • These inputs must be driven from low-impedance circuits.	
9 25	LSELO RSELO	Outputs from the input selector	
13 12 10 21 22 24	L1 L2 L3 R1 R2 R3	Signal inputs	
14	V_{DD}	Power supply connection	
19	V_{SS}	Ground	
15	CE	Chip enable. Data is latched internally at the point this pin goes from high to low. The analog switches operate at that point. Data transfer is enabled when this pin is high.	
16 17	DI CL	Inputs for the serial data and clock used for LSI control.	
20	TEST	Test input (Must be left open during normal operation.)	
5 29	L10dBOUT R10dBOUT	10-dB block outputs	
4 30	LIN RIN	• 1-dB block inputs • These inputs must be driven by low-impedance circuits.	
11 18 23	NC	No-connection pins.	

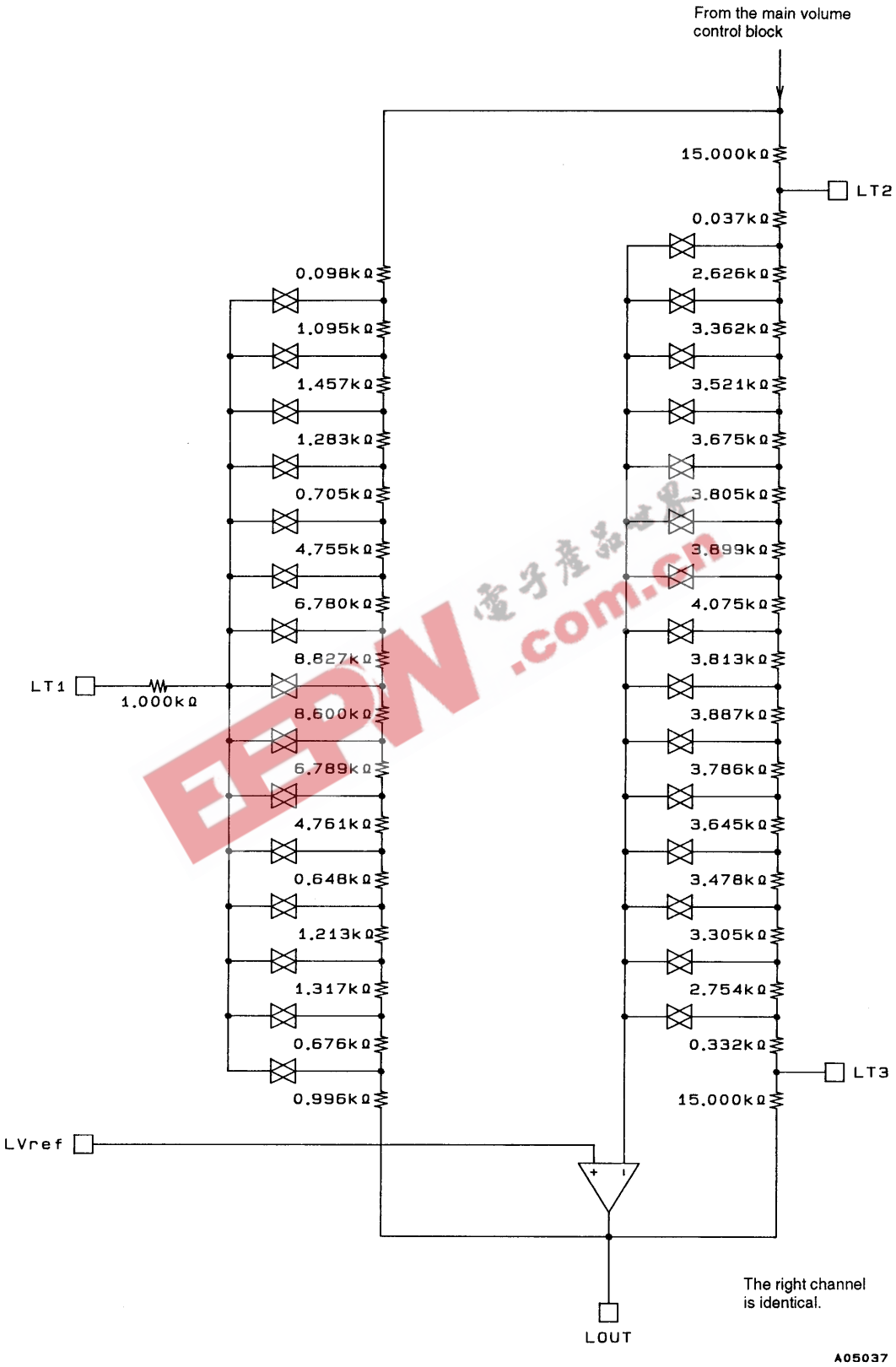
Input Block Equivalent Circuit



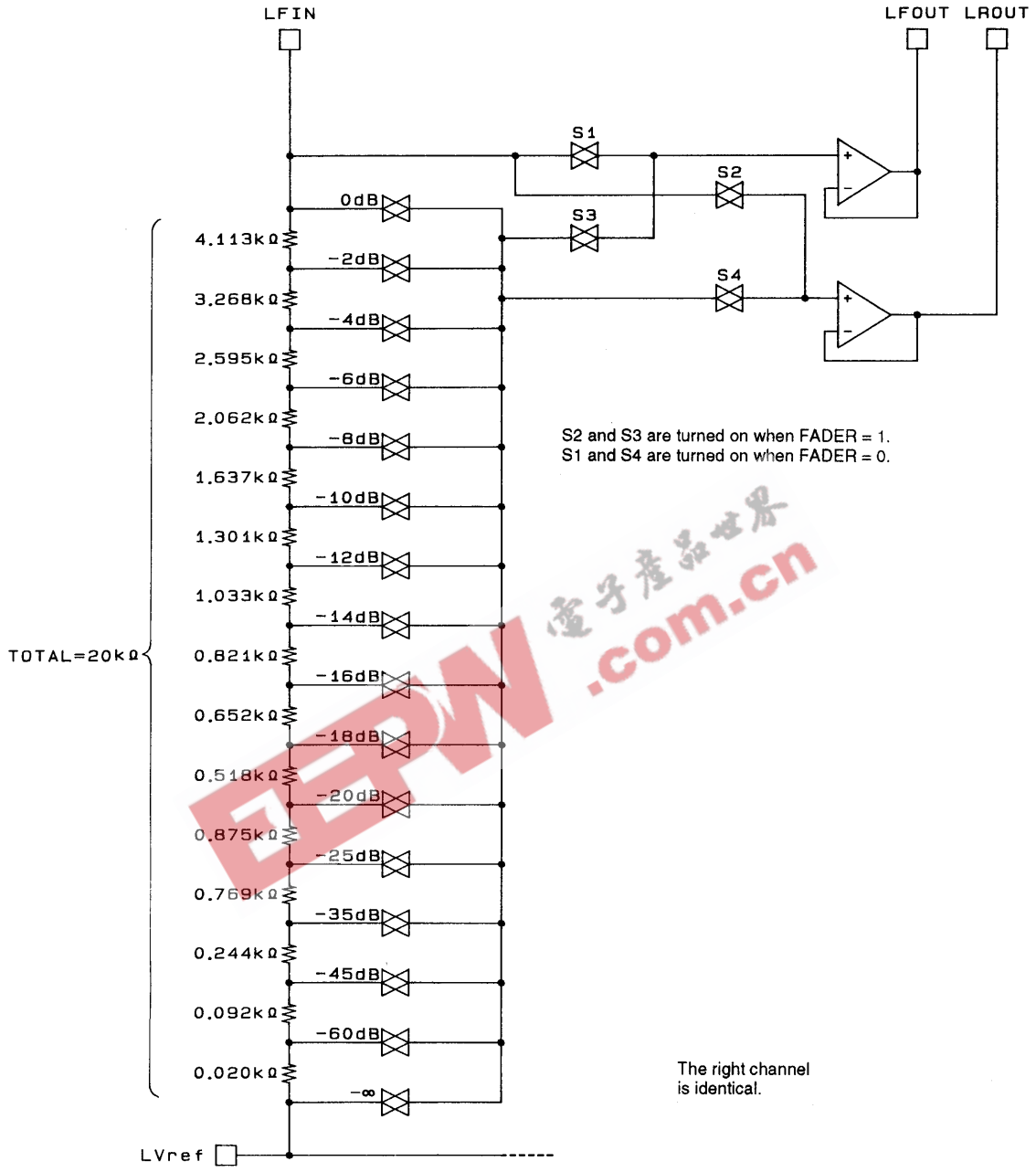
Main Volume Control Equivalent Circuit



Tone Control Block Equivalent Circuit



Fader Volume Control Block Equivalent Circuit



Sample Calculation of the Loudness Circuit External Constants

First, see the LC75372E 10-dB step internal equivalent circuit shown on page 10. Figure 1 shows a circuit to which the loudness circuit external components have been added, and which has been simplified for this calculation. The sample calculation below uses this circuit diagram to acquire a 5-dB boost at f = 100 Hz.

(f = 100 Hz, 5-dB boost)

Assuming that the resistors and capacitors in Figure 1 have the following values:

R1 = R2 = 50 kΩ

R3 = 5 kΩ

And C1 = Z1 and C2 = Z2.

Then:

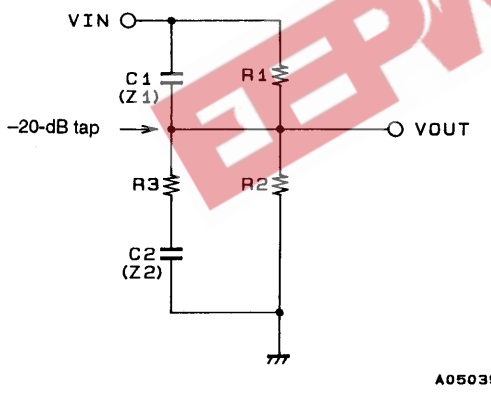
$$V_{OUT} \text{ (at = 1 kHz)} = \frac{\frac{R2\,(R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2\,(R3 + Z2)}{R2 + R3 + Z2}} = -20 \text{ dB}$$

$$V_{OUT} \text{ (at = 100 Hz)} = \frac{\frac{R2\,(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2\,(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15 \text{ dB}$$

From the above equations we find:

$Z1 \neq 891.5\ k\Omega$ and $Z2 = 880\ \Omega$.

Therefore, the specifications will be met if capacitors that have these impedances at f = 1 kHz are connected externally. The result is that C1 = 178.5 pF and C2 = 0.18 μF.

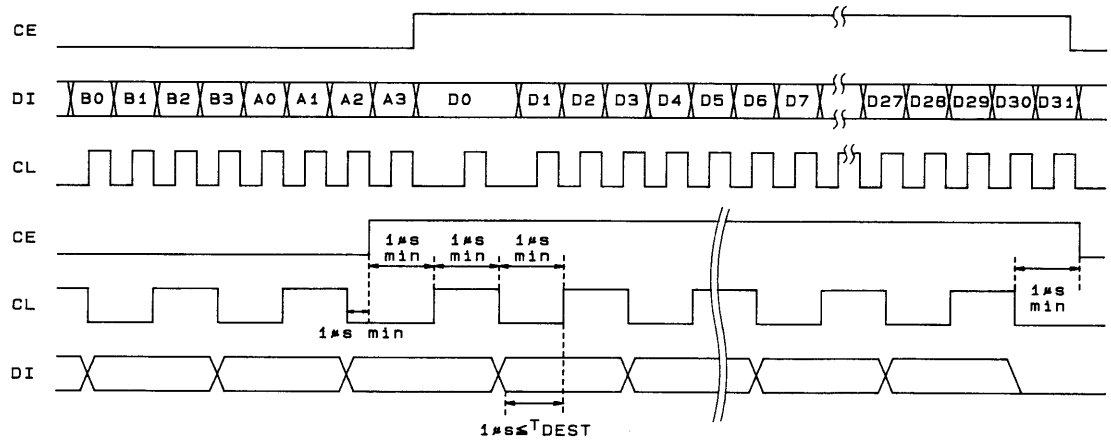


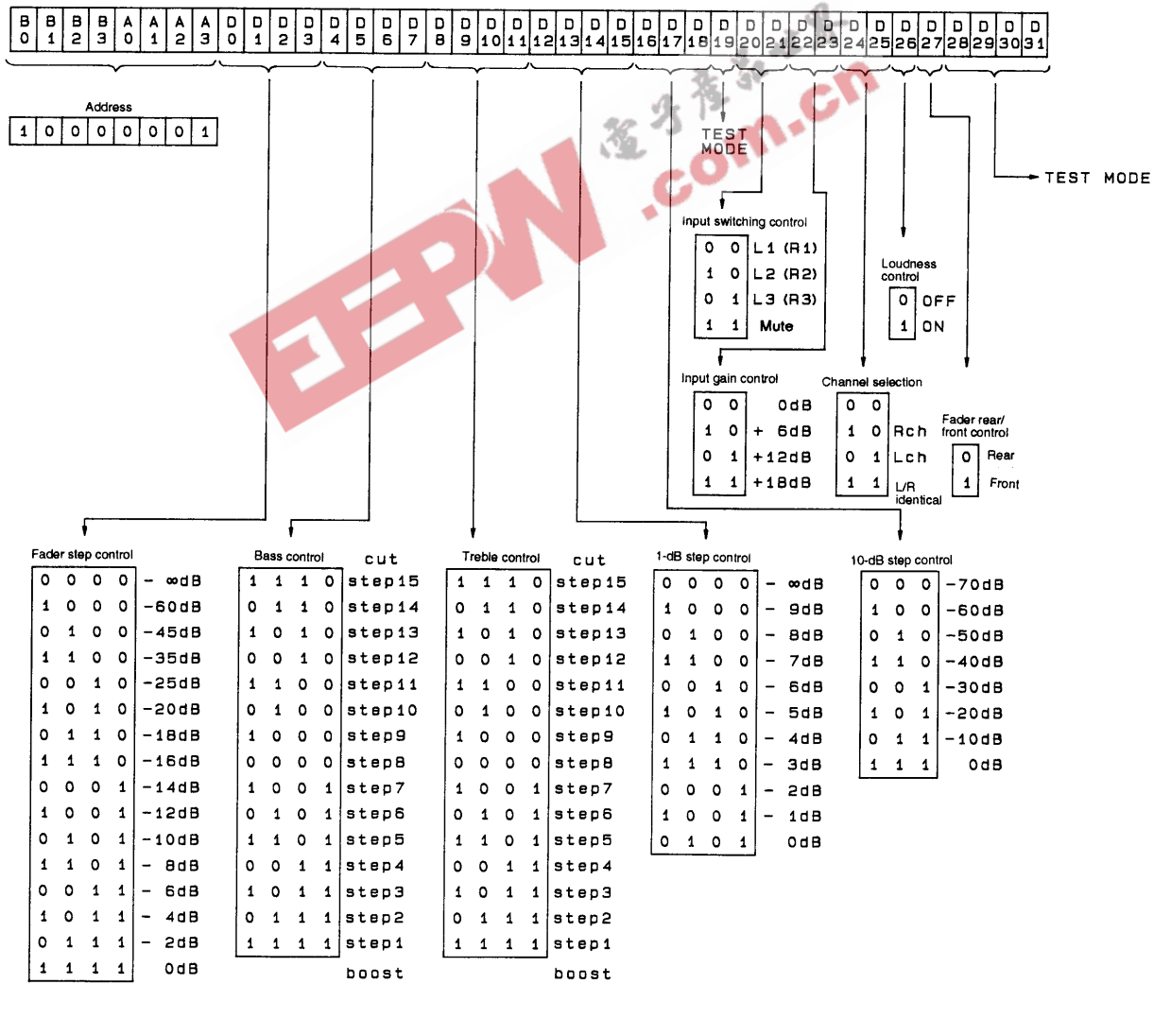
R1, R2, R3: LC75372E internal resistances
C1: External high-band compensation capacitor
C2: External low-band compensation capacitor

Figure 1

Control System Timing and Data Format

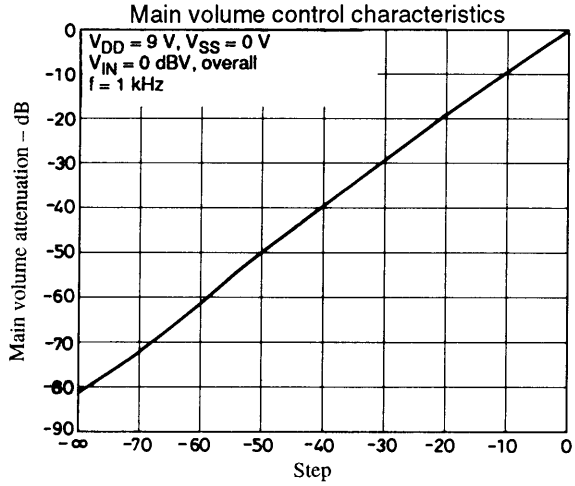
The LC75372E is controlled by applying data in the stipulated format to the CE, CL, and DI pins. The data consists of 40 bits, of which 8 bits are the chip address and 32 bits are the data.



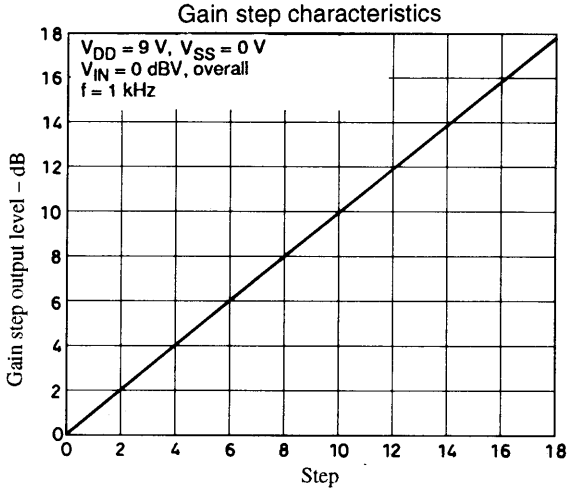


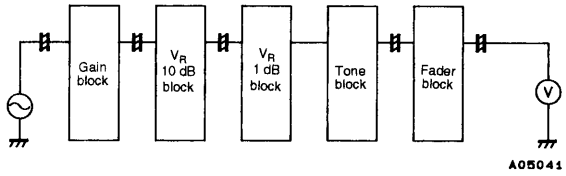
Note: The bits D19 and D28 to D31 are LSI test bits, and must be set to 0.

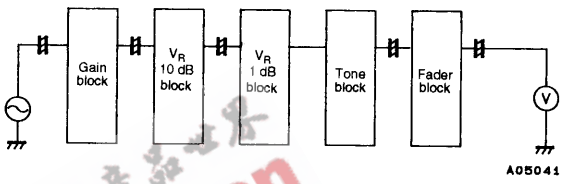
Main volume control characteristics



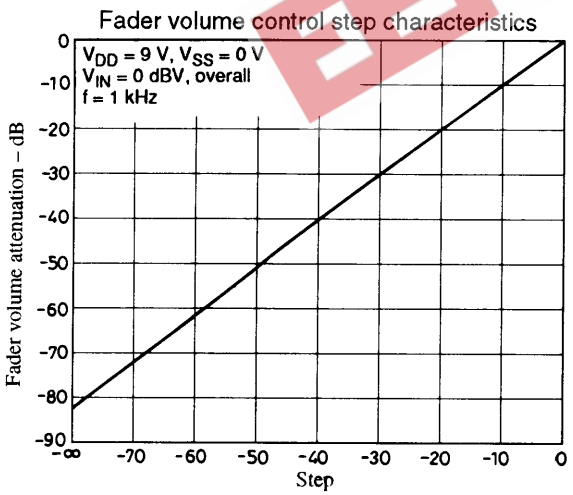
Gain step characteristics



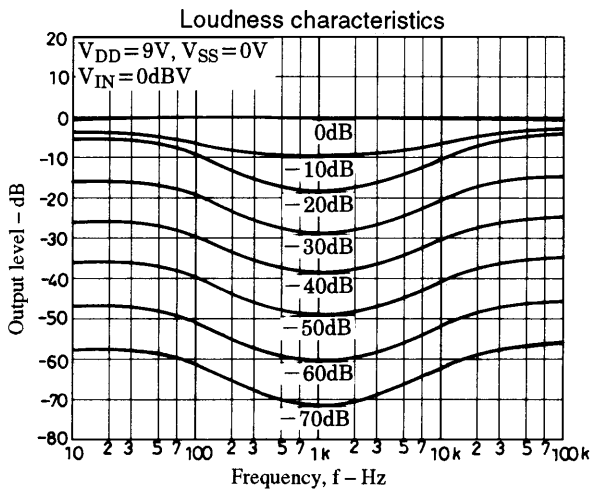


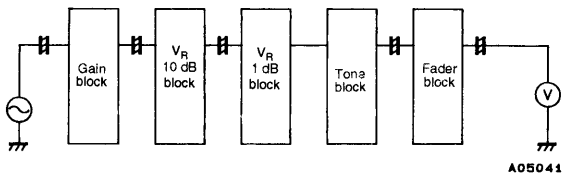


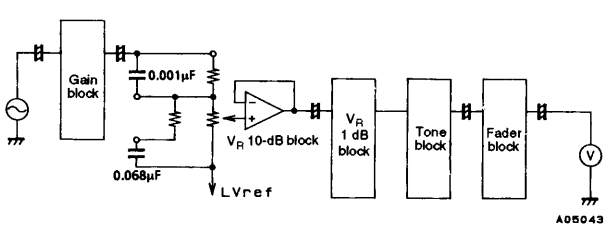
Fader volume control step characteristics



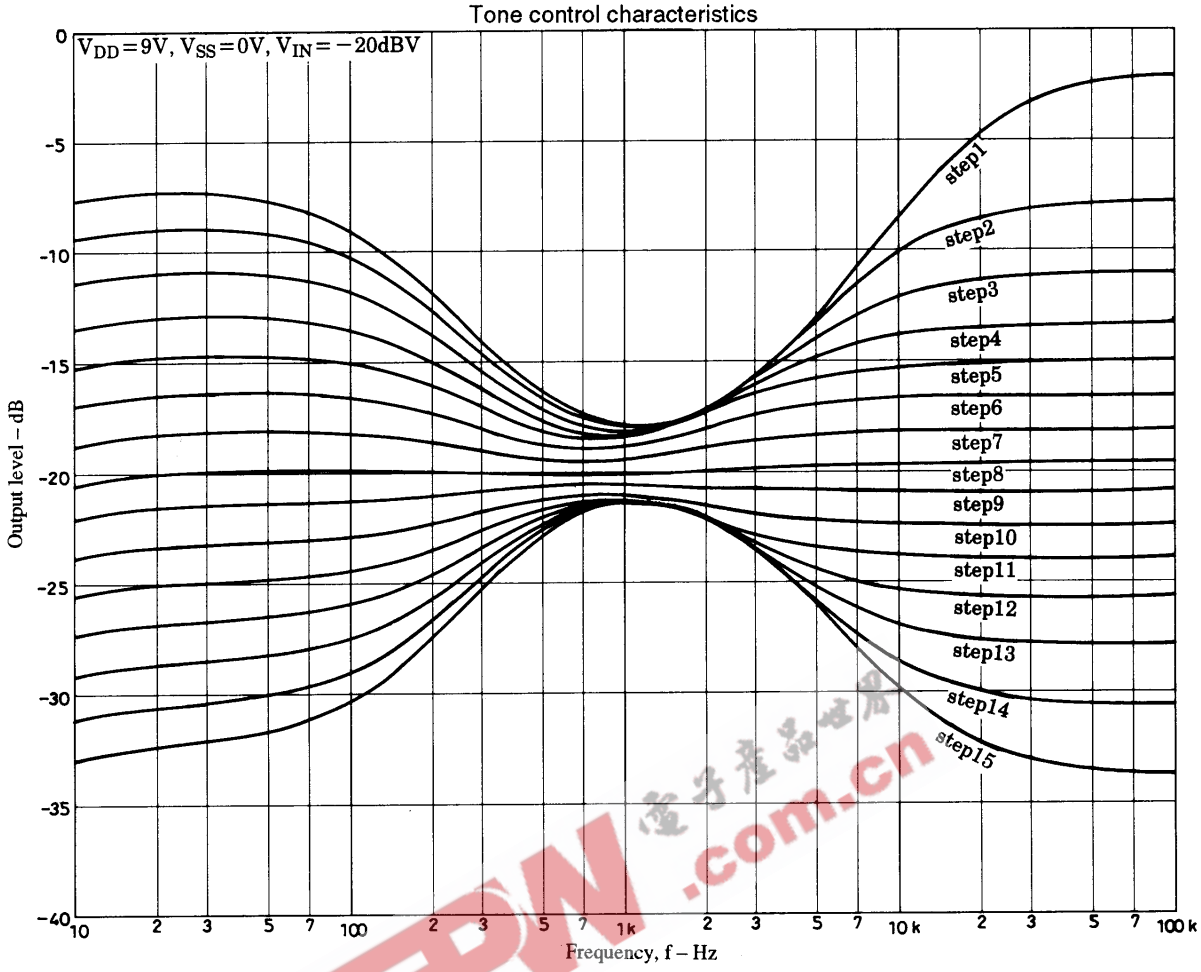
Loudness characteristics

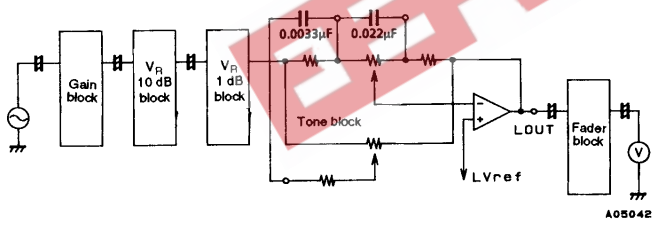




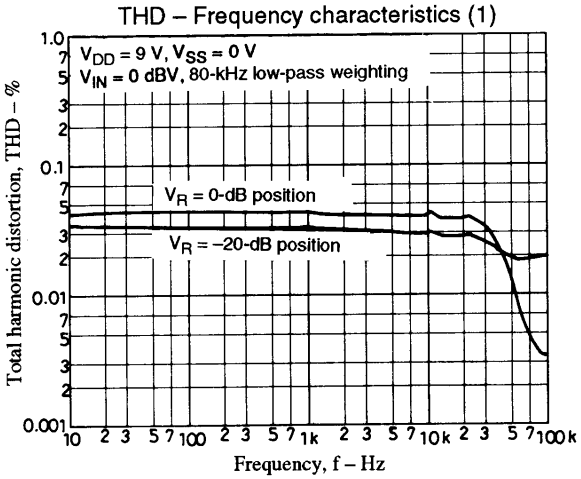


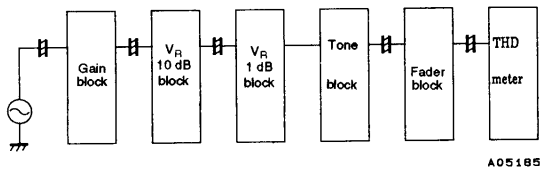
Tone control characteristics



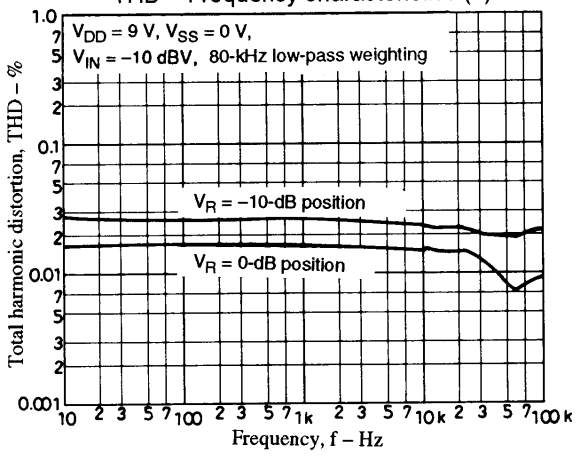


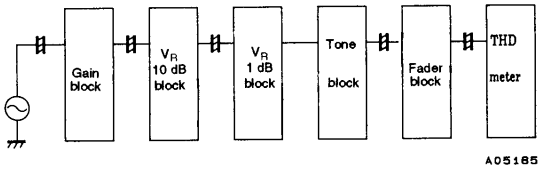
THD – Frequency characteristics (1)



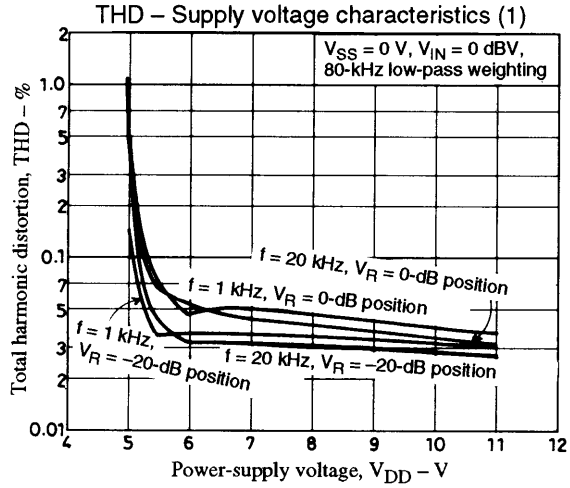


THD – Frequency characteristics (2)

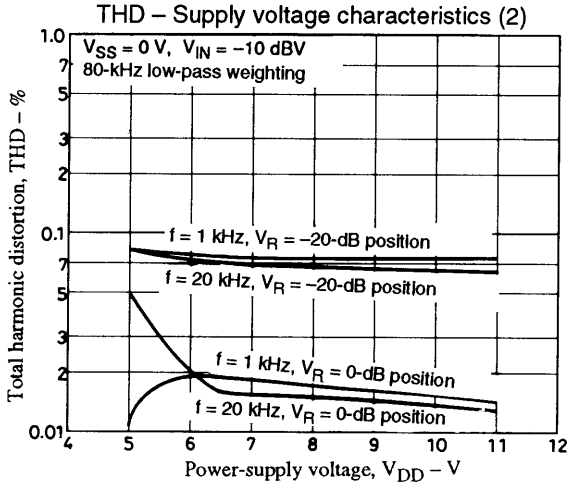


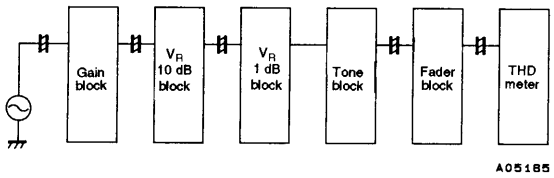


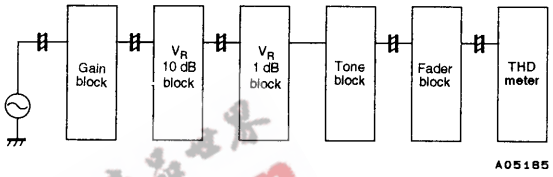
THD – Supply voltage characteristics (1)



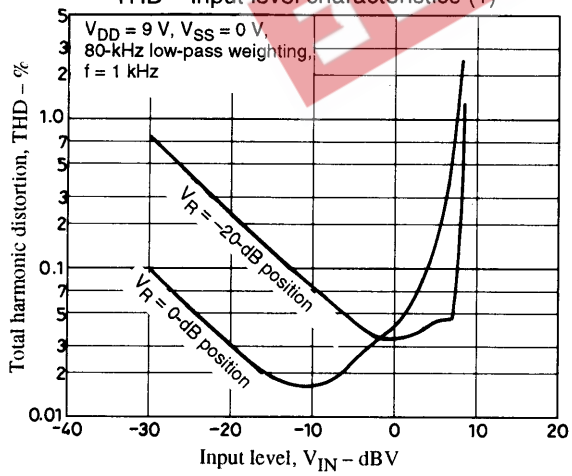
THD – Supply voltage characteristics (2)



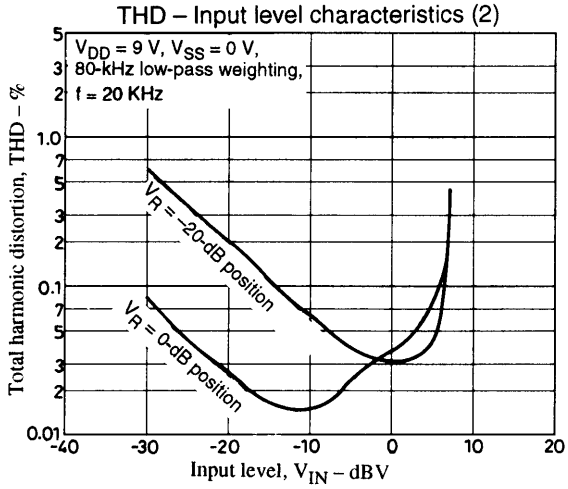


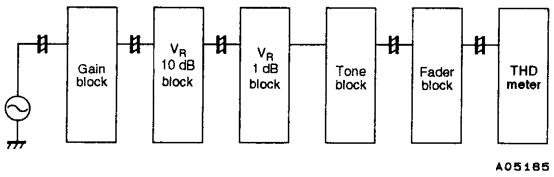


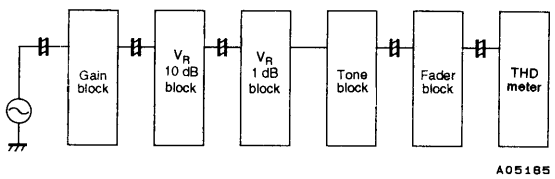
THD – Input level characteristics (1)

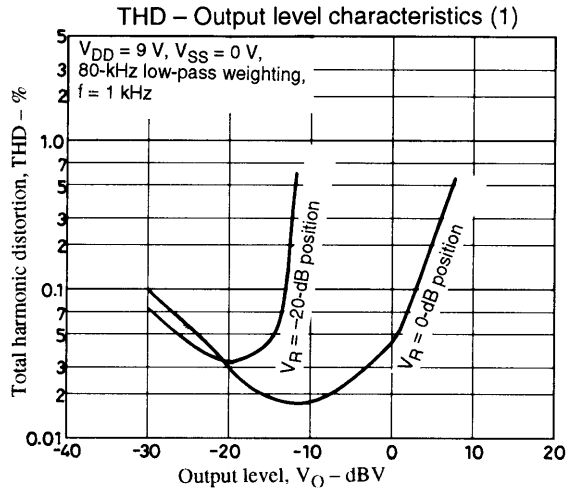


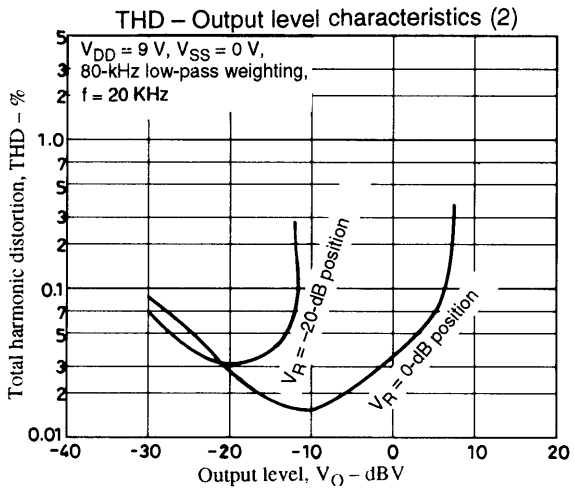
THD – Input level characteristics (2)

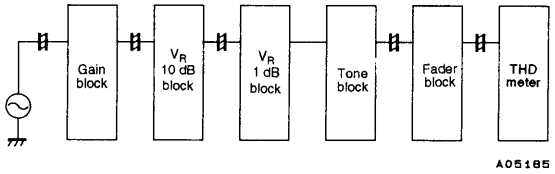


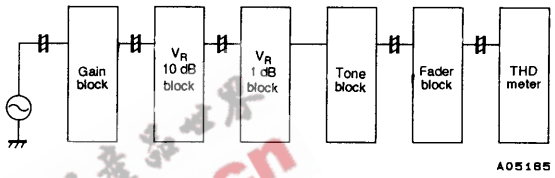












Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Use an external muting circuit or other technique to mute the outputs until correct control data has been set up in the LC75372E.
2. Either cover the lines connected to the CL, DI, and CE pins with the ground pattern or use shielded cable for those lines to prevent the high-frequency digital signals on those lines from entering the analog system.
3. Muting by input switching must be used in conjunction with the volume control setting when the maximum volume control attenuation (the VOL = –∞ position) is used.