Ordering number: EN 6157

LC7940Y

Dot-matrix LC

Overview

The LC7940YC and LC7941YC are segment driver ICs for driving large, dot-matrix LCD displays. They read 4-bit parallel or serial input, display data from a controller into an 80-bit latch, and then generate LCD drive signals corresponding to that data.

The LC7940YC and LC7941YC feature mirror-image pin assignments, allowing them to be used together to increase component density. They are designed to be used with the LC7942YC common driver to drive large LCD panels.

Features

- 80 built-in LCD display drive circuits
- 1/8 to l/128 display duty cycle
- Serial or 4-bit parallel data input
- Chip disable for low power dissipation for large-sized panels
- Bias supply voltags can be supplied externally
- Operating supply voltage and ambient temperature
  - 2.7 to 5.5 V logic supply (V_{DD}) at Ta = -20 to +85°C
  - 8 to 20V LCD supply (V_{DD} - V_{EE}) at Ta = -20 to +85 °C
- CMOS process

Specifications

The following electrical characteristics apply when sealed in a Sanyo standard QIC-100 package.

Absolute Maximum Ratings at Ta = 25 ± 2°C, V_{SS} = 0 V

Parameter	Symbol	Ratings
Logic supply voltge	V_{DD} max	–0.3 to +7.0
LCD supply voltage, See Note below.	V_{DD} – V_{EE} max	0 to 22
Input voltage	V_I max	–0.3 to V_{DD} + 03

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Parameter	Symbol	Ratings
Operating temperature range	T_{opr}	–20 to +85
Storage temperature range	T_{stg}	–40 to +125

Note

$V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$

Recommended Operating Condltions at Ta = –20 to + 85°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings		
			min	typ	max
Logic supply voltage	V_{DD}		2.7	–	
LCD supply voltage	$V_{DD} - V_{EE}$	See Notes 1 and 2.	8	–	
HIGH–level input voltage	V_{IH}	CP, CDI, DI1 to DI3, M, SDI, P/S, $\overline{DISPOFF}$ and LOAD	$0.8V_{DD}$	–	
LOW–level inpvt voltage	V_{IL}	CP, CDI, DI1 to DI3, M, SDI, P/S,$\overline{DISPOFF}$ and LOAD	–	–	0.2
CP shift clock frequency	f_{CP}			–	
CP pulsewidth	t_{WC}		100	–	
LOAD pulsewidth	t_{WL}		100	–	
DIn and SDI to CP setup time	t_{SETUP}		80	–	
DIn and SDI to CP hold time	t_{HOLD}		80	–	
CP to LOAD time	t_{CL1}		0	–	
	t_{CL2}		100	–	
LOAD to CP time	t_{LC}		100	–	
CP rise time	t_R		–	–	
CP fall time	t_F		–	–	
LOAD rise time	t_{RL}		–	–	
LOAD fall time	t_{FL}		–	–	

Notes

1. $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$
2. At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF should be cut after or simultaneously with the LCD supply.

Electrlcai Characterfstlcs at Ta = 25 ± 2°C,V_{SS} = 0V, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Conditions	Ratings		
			min	typ	max
HIGH–level input current	I_{IH}	$V_{IN} = V_{DD}$; LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and $\overline{DISPOFF}$	–	–	
LOW–level input current	I_{IL}	VIN = VSS; LOAD, CP, CDI, P/S, DI1 to DI3, SDI, M, and $\overline{DISPOFF}$	–	–	
CDO HIGH–level output voltage	V_{OH}	I_{OH} = –400 µA	V_{DD} – 0.4	–	
CDO LOW–levef output voltage	V_{OL}	I_{OL} = 400 µA	–	–	
O1 to O80 driver ON resistance	R_{ON}	$V_{DD} - V_{EE}$ = 18 V, $\lvert V_{DE} - V_{O}\rvert$ = 0.25 V. See note	–	2	

Parameter	Symbol	Conditions	Ratings		
			min	typ	max
V_{DD} to V_{SS} standby supply current	I_{ST}	CDI = V_{DD}, $V_{DD} - V_{EE}$ = 18 V, f_{CP} = 3.3 MHz, no output load ; V_{SS}	–	–	
V_{DD} to V_{ss} operating supply current	I_{SS}	$V_{DD} - V_{EE}$ = 18 V, f_{CP} = 3.3 MHz, I_{LOAD}= 5.156 kHz, f_M = 52 Hz ;VSS	–	–	
V_{DD} to V_{EE} operating supply current	I_{EE}	$V_{DD} - V_{EE}$ = 18V, f_{CP} = 3.3 MHz, f_{LOAD} = 5,156 kHz, f_M = 52 Hz ; V_{EE}	–	–	
CP input capacitance	C_I	f_{CP} = 3.3 MHz ; CP	–	5	

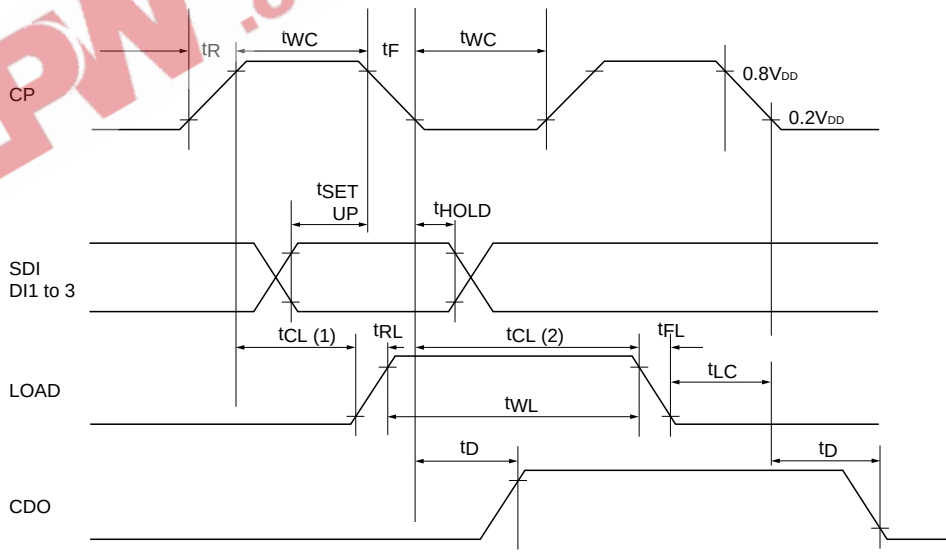
Note

$V_{DE} = V_1$ or V_3, or V_4 or V_{EE}, $V_1 = V_{DD}$, $V_3 = 9/11 \times (V_{DD} - V_{EE})$, $V_4 = 2/11 \times (V_{DD} - V_{EE})$

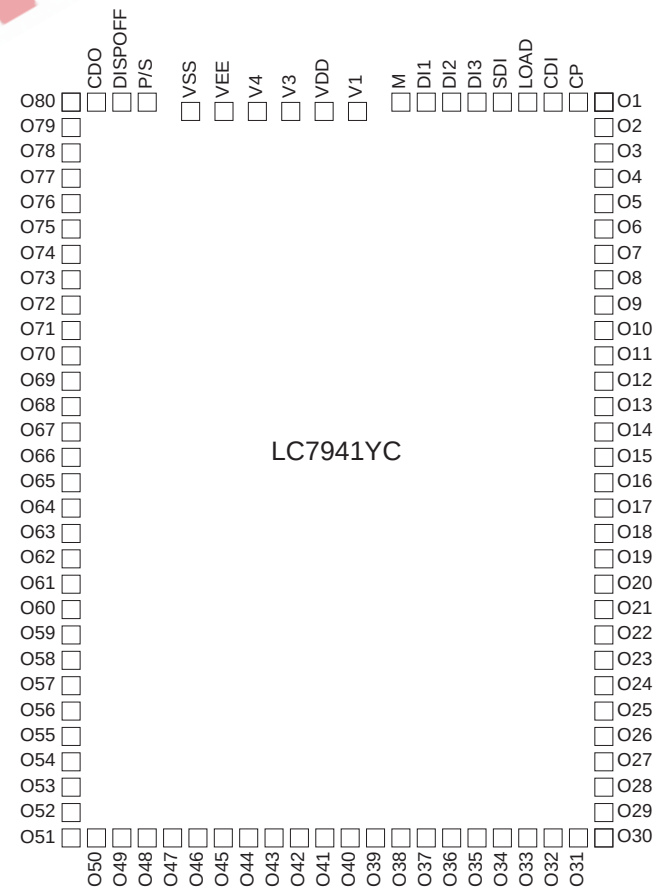
Switching Characteristics at Ta = 25 ± 2°C, V_{SS} = 0V, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Conditions	Ratings		
			min	typ	max
CDO output delay time	t_D	C_L = 30 pF	–	–	

Switching Characteristics Waveform



Pad Layout (Top view)



LC7940YC Pad Location

chip size : 4.830 mm x 3.550 mm

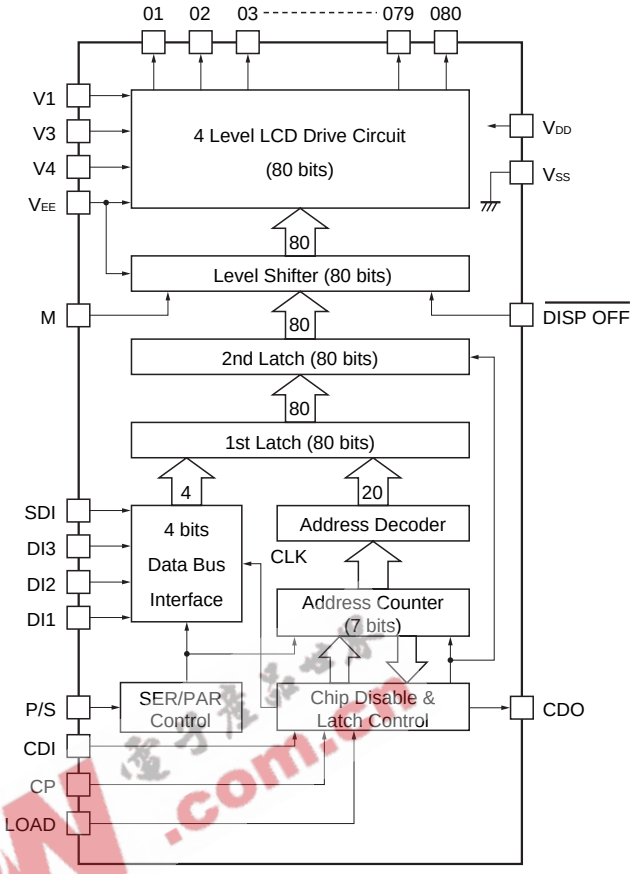
Pin_No.	Name	X	Y	Pin_No.	Name	X
1	O1	-1600	2240	51	O51	1600
2	O2	-1600	2072	52	O52	1600
3	O3	-1600	1906	53	O53	1600
4	O4	-1600	1742	54	O54	1600
5	O5	-1600	1580	55	O55	1600
6	O6	-1600	1420	56	O56	1600
7	O7	-1600	1262	57	O57	1600
8	O8	-1600	1106	58	O58	1600
9	O9	-1600	952	59	O59	1600
10	O10	-1600	800	60	O60	1600
11	O11	-1600	650	61	O61	1600
12	O12	-1600	502	62	O62	1600
13	O13	-1600	356	63	O63	1600
14	O14	-1600	212	64	O64	1600
15	O15	-1600	70	65	O65	1600
16	O16	-1600	-70	66	O66	1600
17	O17	-1600	-212	67	O67	1600
18	O18	-1600	-356	68	O68	1600
19	O19	-1600	-502	69	O69	1600
20	O20	-1600	-650	70	O70	1600
21	O21	-1600	-800	71	071	1600
22	O22	-1600	-952	72	O72	1600
23	O23	-1600	-1106	73	O73	1600
24	O24	-1600	-1262	74	O74	1600
25	O25	-1600	-1420	75	O75	1600
26	O26	-1600	-1580	76	O76	1600
27	O27	-1600	-1742	77	O77	1600
28	O28	-1600	-1906	78	O78	1600
29	O29	-1600	-2072	79	O79	1600
30	O30	-1600	-2240	80	O80	1600
31	O31	-1420	-2240	81	---	---
32	O32	-1262	-2240	82	CDO	1415
33	O33	-1106	-2240	83	---	---
34	O34	-952	-2240	84	$\overline{\text{DISPOFF}}$	1252
35	O35	-800	-2240	85	P/S	1091
36	O36	-650	-2240	86	V_{SS}	825
37	O37	-502	-2240	87	V_{EE}	629
38	O38	-356	-2240	88	V_4	464
39	O39	-212	-2240	89	V_3	299
40	O40	-70	-2240	90	---	---
41	O41	70	-2240	91	V_{DD}	123
42	O42	212	-2240	92	V_1	-42
43	O43	356	-2240	93	M	-316
44	O44	502	-2240	94	DI1	-467
45	O45	650	-2240	95	DI2	-620
46	O46	800	-2240	96	DI3	-775
47	O47	952	-2240	97	SDI	-932
48	O48	1106	-2240	98	LOAD	-1091
49	O49	1262	-2240	99	CDI	-1252
50	O50	1420	-2240	100	CP	-1415

LC7941C Pad Location

chip size : 4.830 mm x 3.550 mm

Pin No.	Name	X	Y	Pin No.	Name	X
1	O80	-1600	2240	51	O30	1600
2	O79	-1600	2072	52	O29	1600
3	O78	-1600	1906	53	O28	1600
4	O77	-1600	1742	54	O27	1600
5	O76	-1600	1580	55	O26	1600
6	O75	-1600	1420	56	O25	1600
7	O74	-1600	1262	57	O24	1600
8	O73	-1600	1106	58	O23	1600
9	O72	-1600	952	59	O22	1600
10	O71	-1600	800	60	O21	1600
11	O70	-1600	650	61	O20	1600
12	O69	-1600	502	62	O19	1600
13	O68	-1600	356	63	O18	1600
14	O67	-1600	212	64	O17	1600
15	O66	-1600	70	65	O16	1600
16	O65	-1600	-70	66	O15	1600
17	O64	-1600	-212	67	O14	1600
18	O63	-1600	-356	68	O13	1600
19	O62	-1600	-502	69	O12	1600
20	O61	-1600	-650	70	O11	1600
21	O60	-1600	-800	71	O10	1600
22	O59	-1600	-952	72	O9	1600
23	O58	-1600	-1106	73	O8	1600
24	O57	-1600	-1262	74	O7	1600
25	O56	-1600	-1420	75	O6	1600
26	O55	-1600	-1580	76	O5	1600
27	O54	-1600	-1742	77	O4	1600
28	O53	-1600	-1906	78	O3	1600
29	O52	-1600	-2072	79	O2	1600
30	O51	-1600	-2240	80	O1	1600
31	O50	-1420	-2240	81	CP	1415
32	O49	-1262	-2240	82	CDI	1252
33	O48	-1106	-2240	83	LOAD	1091
34	O47	-952	-2240	84	SDI	932
35	O46	-800	-2240	85	DI3	775
36	O45	-650	-2240	86	DI2	620
37	O44	-502	-2240	87	DI1	467
38	O43	-356	-2240	88	M	316
39	O42	-212	-2240	89	V_1	42
40	O41	-70	-2240	90	V_{DD}	-123
41	O40	70	-2240	91	---	---
42	O39	212	-2240	92	V_3	-299
43	O38	356	-2240	93	V_4	-464
44	O37	502	-2240	94	V_{EE}	-629
45	O36	650	-2240	95	V_{SS}	-825
46	O35	800	-2240	96	P/S	-1091
47	O34	952	-2240	97	$\overline{\text{DISPOFF}}$	-1252
48	O33	1106	-2240	98	---	---
49	O32	1262	-2240	99	CDO	-1415
50	O31	1420	-2240	100	---	---

Block Diagram



Pin Functions

Pin No.		Symbol	I/O	Function
LC7940YC	LC7941YC			
91	90	V_{DD}	Supply	$V_{DD} - V_{SS}$ is the logic supply. $V_{DD} - V_{EE}$ is the LCD supply.
86	95	V_{SS}		
87	94	V_{EE}		
92	89	V_1	Supply	LCD panel drive voltage supplies V_1 and V_{EE} are selected levels. V_3 and V_4 are not–selected levels.
89	92	V_3		
88	93	V_4		
l00	81	CP	I	Display data Input clock (falling–edge trigger).
99	82	CDI	I	Chip disable. Data is read in when LOW, and not road in when HIGH.
98	83	LOAD	I	Display data latch clock (falling–edge trigger). On the falling edge, the LCD drive signals set by the display dat
97	84	SDI	I	Serial data input.
96	85	DI3	I	4–bit parallel data input pins.
95	86	DI2		
94	87	D11		

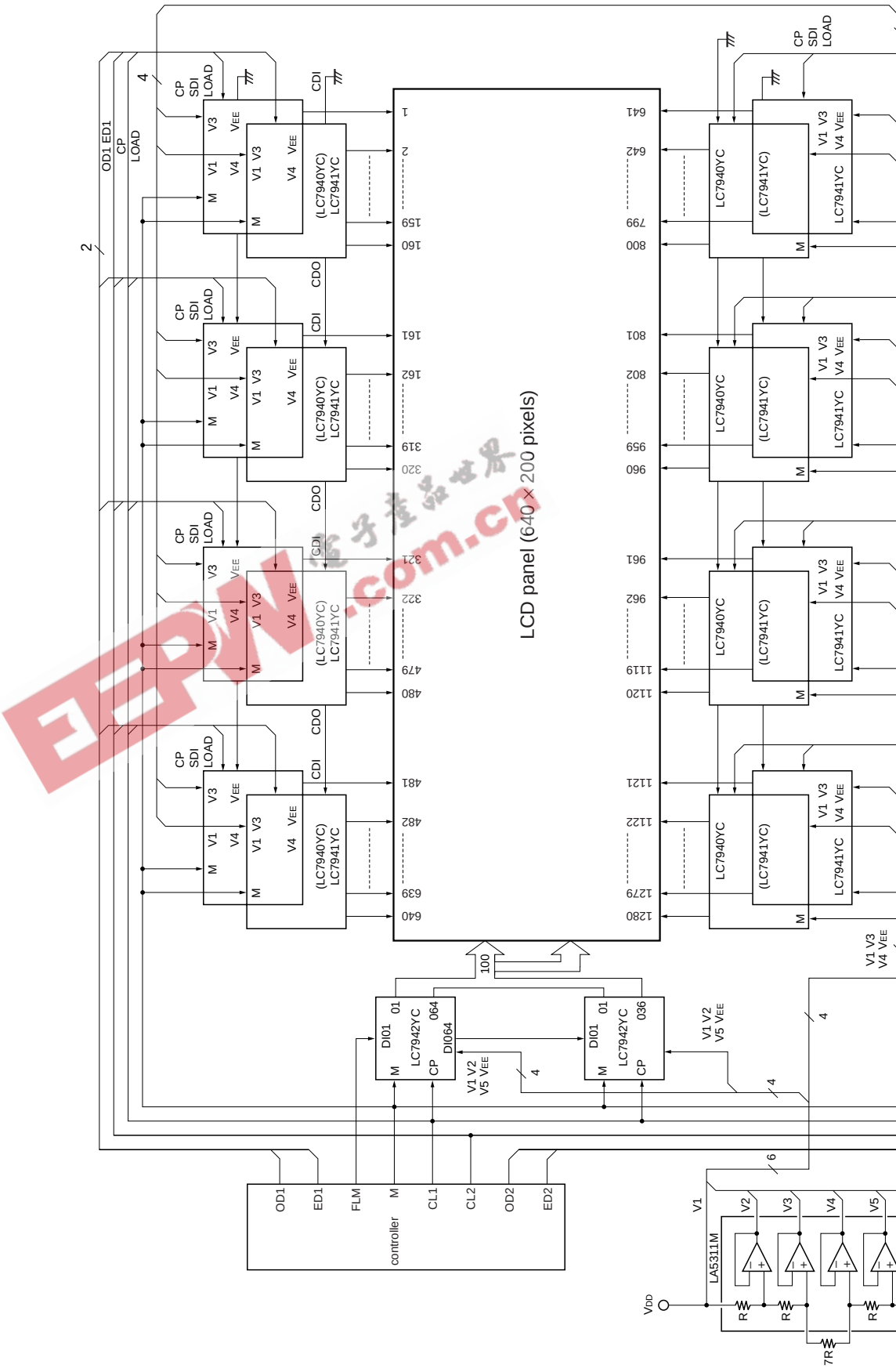
Data input	LCD driver outp	
SDI	O4	O8
DI3	O3	O7
DI2	O2	O6
DI1	O1	O5

In serial data input mode, DI1 to DI3 should all be tied HIGH or

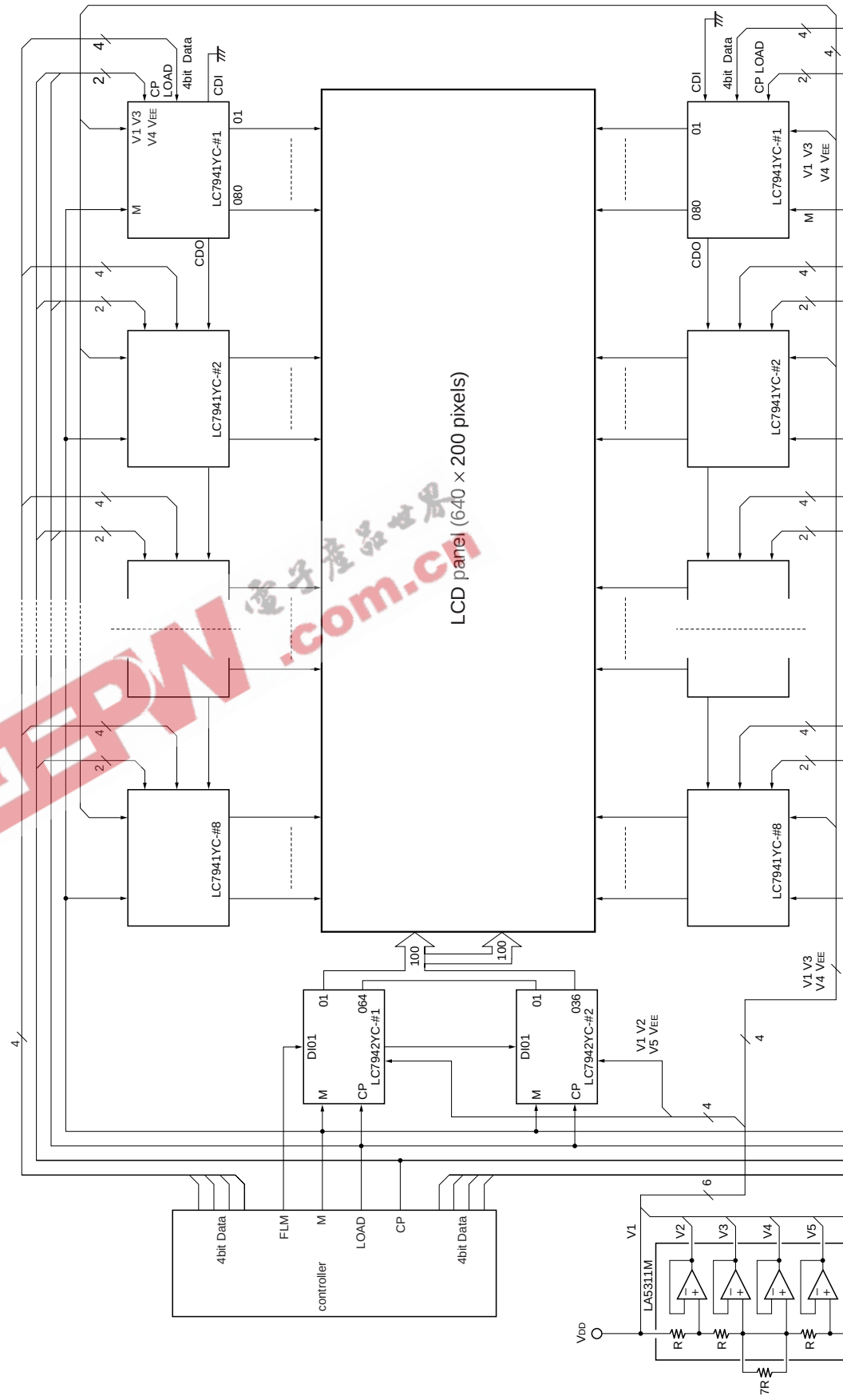
<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Symbol</th><th rowspan="2">I/O</th><th rowspan="2">Function</th></tr>
<tr><th>LC7940YC</th><th>LC7941YC</th></tr>
<tr><td>93</td><td>88</td><td>M</td><td>I</td><td>LCD panel drive voltage output alternation control signal.</td></tr>
<tr><td>85</td><td>96</td><td>P/S</td><td>I</td><td>Data input mode select. 4–bit parallel input when HIGH, and ser</td></tr>
<tr><td>82</td><td>99</td><td>CDO</td><td>O</td><td>Cascade connection pin for extension segment drivers. Data is
Goes LOW after data is read out. Connected to the CDI input of</td></tr>
<tr><td>1 to 80</td><td>80 to 1</td><td>Ol to O80</td><td>O</td><td>LCD drive outputs.
The output drive level is determined by the display data, M signa
input as shown below.
<table>
<tr><th>M</th><th>Q</th><th>$\overline{\text{DISP OFF}}$</th></tr>
<tr><td>LOW</td><td>LOW</td><td>HIGH</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>HIGH</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td></tr>
<tr><td>×</td><td>×</td><td>LOW</td></tr>
</table>
Note
x = don't care (tied HIGH or LOW)</td></tr>
<tr><td>84</td><td>97</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>O1 to O80 output control input pin.
When LOW, V1 is output on the O1 to 080 outputs, See the truth</td></tr>
<tr><td>81</td><td>91</td><td>NC</td><td rowspan="3">–</td><td rowspan="3">No connection.</td></tr>
<tr><td>83</td><td>98</td><td>NC</td></tr>
<tr><td>90</td><td>100</td><td>NC</td></tr>
</table>

Application Notes

LCD Panel 1



LCD Panel 2

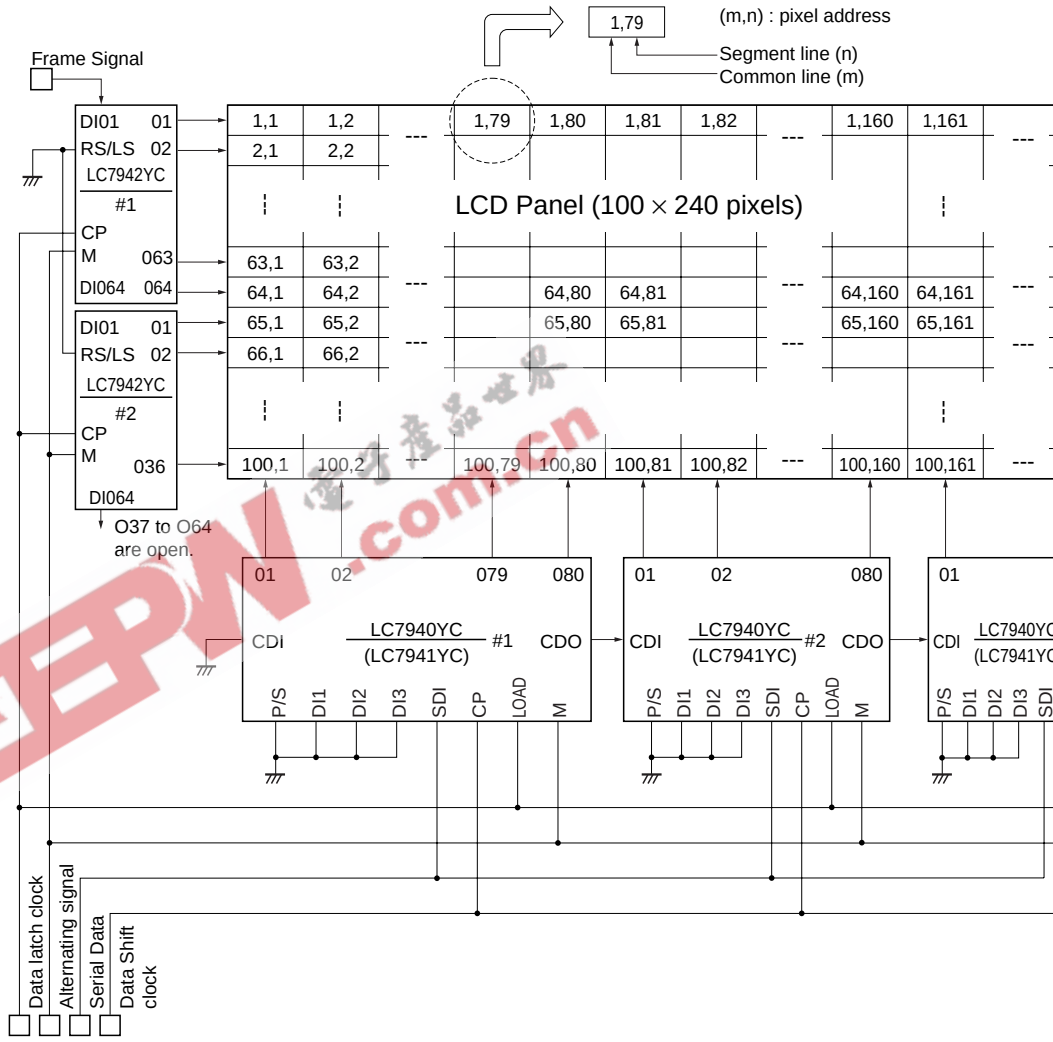

LCD panel (640 × 200 pixels)
LC7941YC-#1
LC7941YC-#2
LC7941YC-#8
LC7942YC-#1
LC7942YC-#2
4bit Data
CP LOAD
CDI
CDO
V1 V3
V4 VEE
V1 V2
V5 VEE
DI01
FLM
LOAD
CP
controller
LA5311M
VDD
R
7R

100 x 240-pixel LCD Panel Application

A 100 × 240–pixel LCD panel requires the following drivers.

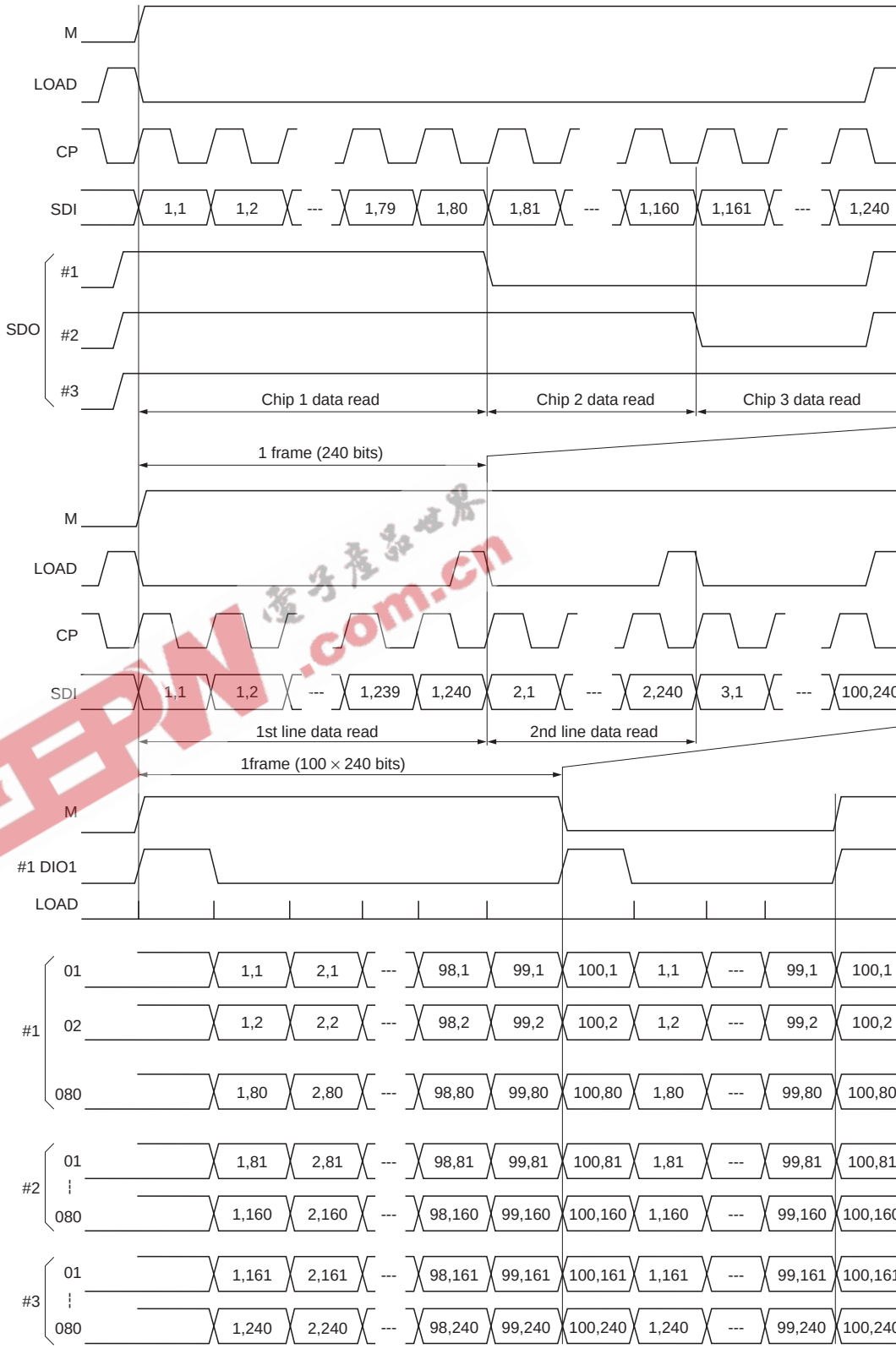
- 3 x LC7940YC (or LC7941YC) drivers
- 2 x LC7942YC drivers

An example using l/l00 duty cycle is shown below.



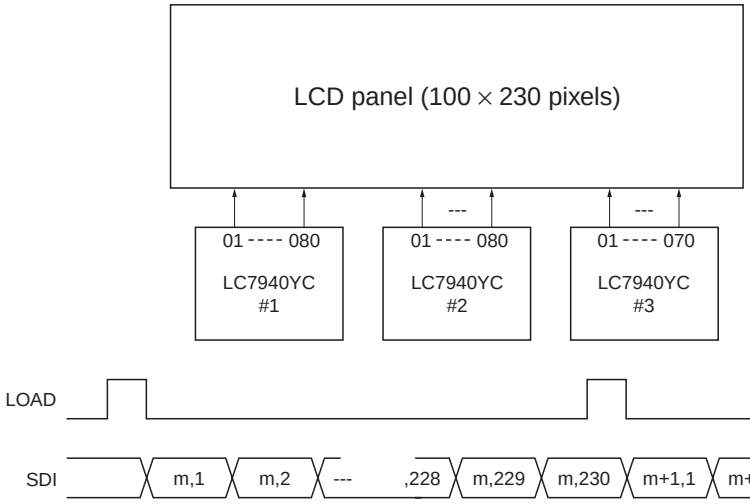
1. The LC7942YC chips are cascaded by connecting DIO64 on chip I to DIO1 on chip 2. For a 100–bit shift register, O37 to O64 on chip 2 are left open.
2. The LC7940YC (or LC7941YC) chips are cascaded by connecting CDO on chip I to CDI on chip 2, and CDO on chip 2 to CDI on chip 3. CDI on chip I is tied to GND, and CDO on chip 3 is not used. This configuration allows the input of 240–bit serial data.

100 x 240-pixel LCD Panel Timing Diagram

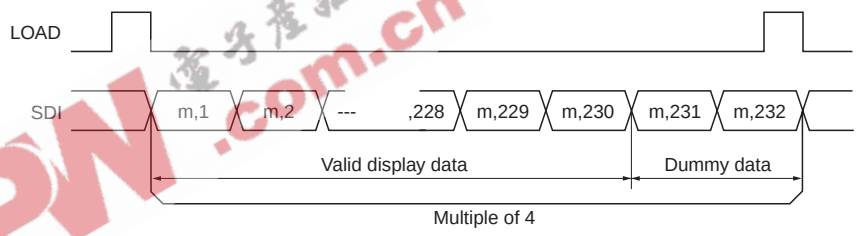


Segment Data Not Multiples of 4

Example.



If this timing data is sent, data elements (m, 229), (m, 230), (m+1, 229), (m+1. 230)... will not appear in the output (O69 and O70 on chip 3). This is because the LC7940YC (or LC7941YC) converts serial/parallel data in 4–bit units, which also decreases power data that is not a multiple of 4, like 23 scheme is used.



In this case, (m, 231) is output on O71 on chip 3, and (m, 232) on O72 on chip 3. However, these outputs are not connected to the panel and are, therefore, invalid.