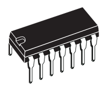
LM124-LM224-LM324

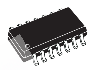
Low power quad operational amplifiers

Features

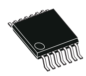
- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current per amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset voltage: 5 mV max. (For more accurate applications, use the equivalent parts LM124A-LM224A-LM324A which feature 3 mV max.)
- Low input offset current: 2 nA
- Wide power supply range:
  – Single supply: +3 V to +30 V
  – Dual supplies: ±1.5 V to ±15 V



N
DIP14
(Plastic package)



D
SO-14
(Plastic micropackage)



P
TSSOP-14
(Thin shrink small outline package)

Description

These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Order codes

Part number	Temperature range	Package	Packing
LM124N	-55°C, +125°C	DIP	Tube
LM124D/DT		SO	Tube or tape & reel
LM224N	-40°C, +105°C	DIP	Tube
LM224D/DT		SO	Tube or tape & reel
LM224PT		TSSOP (Thin shrink outline package)	Tape & reel
LM324N	0°C, +70°C	DIP	Tube
LM324D/DT		SO	Tube or tape & reel
LM324PT		TSSOP (Thin shrink outline package)	Tape & reel

Contents

1 Pin & schematic diagram

Figure 1. Pin connections (top view)

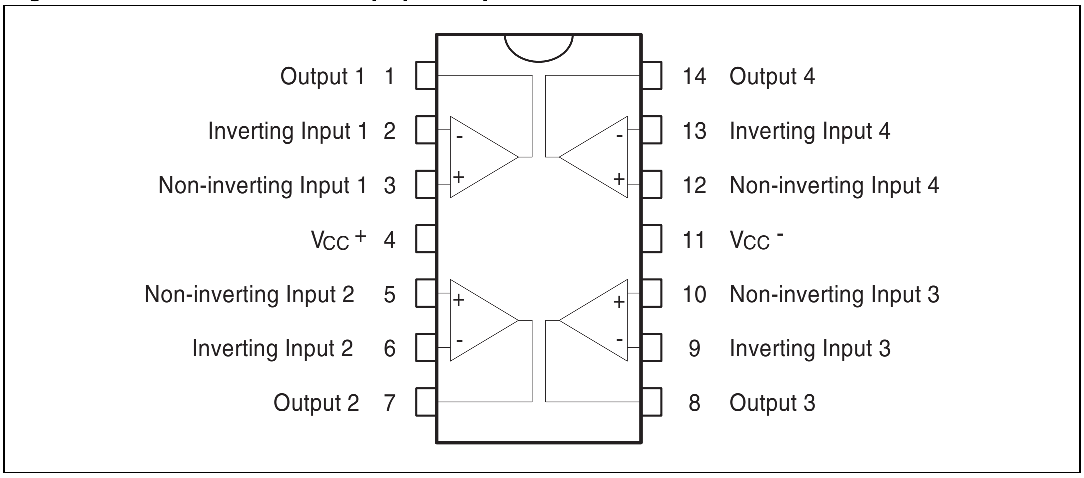
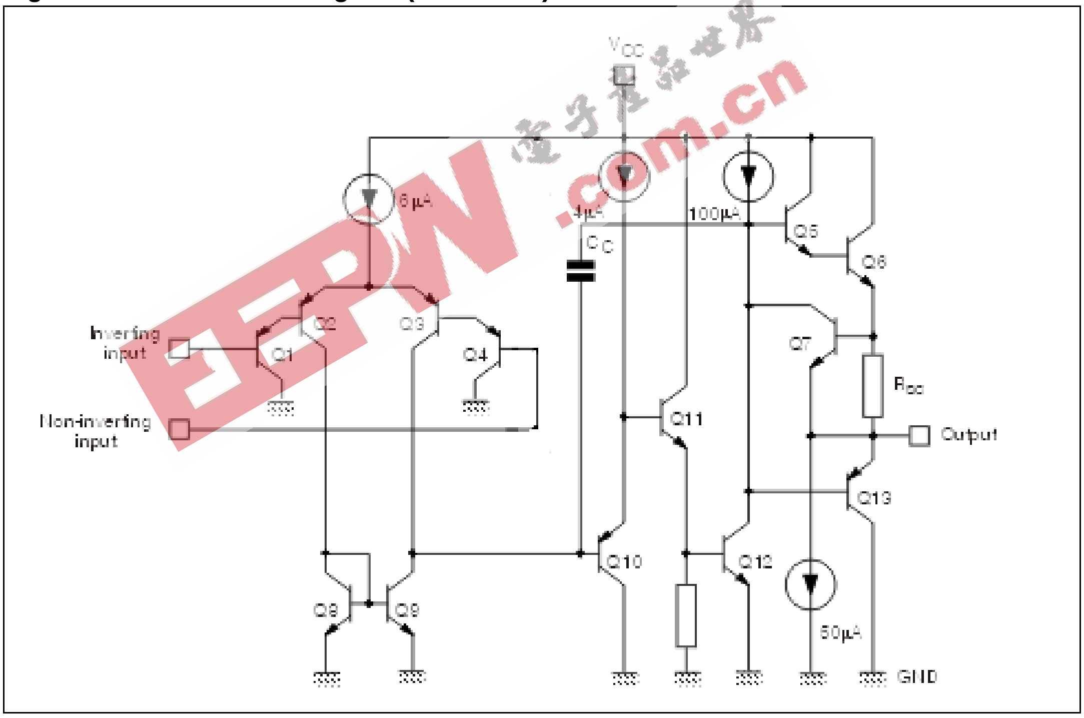


Figure 2. Schematic diagram (1/4 LM124)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	LM124	LM224	LM324	Unit
V_{CC}	Supply voltage	±16 or 32			V
V_i	Input voltage	32			V
V_{id}	Differential input voltage (1)	32			V
P_{tot}	Power dissipation N suffix D suffix	500	500 400	500 400	mW
	Output short-circuit duration (2)	Infinite			
I_{in}	Input current (3)	50	50	50	mA
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150			°C
T_j	Maximum junction temperature	150			°C
R_{thja}	Thermal resistance junction to ambient(4) SO14 TSSOP14 DIP14	 103 100 83			°C/W
R_{thjc}	Thermal resistance junction to case SO14 TSSOP14 DIP14	 31 32 33			°C/W
ESD	HBM: human body model(5)	250			V
	MM: machine model(6)	150			
	CDM: charged device model	1500			

1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
This is not destructive and normal output is restored for input voltages above -0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP, a two-layer board).
5. Human body model, 100 pF discharged through a 1.5 kΩ resistor into pin of device.
6. Machine model ESD, a 200 pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin-to-pin of device.

3 Electrical characteristics

Table 2. V_{CC}^+ = +5 V, V_{CC}^-= Ground, V_o = 1.4 V, T_{amb} = +25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = +25° C LM124-LM224 LM324		2	5 7	mV
	$T_{min} \le T_{amb} \le T_{max}$ LM124-LM224 LM324			7 9	
I_{io}	Input offset current T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		2	30 100	nA
I_{ib}	Input bias current (2) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		20	150 300	nA
A_{vd}	Large signal voltage gain V_{CC}^+ = +15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \le 10$ kΩ) V_{CC}^+ = 5 V to 30 V T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	65 65	110		dB
I_{CC}	Supply current, all Amp, no load T_{amb} = +25° C V_{CC} = +5 V V_{CC} = +30 V		0.7 1.5	1.2 3	mA
	$T_{min} \le T_{amb} \le T_{max}$ V_{CC} = +5 V V_{CC} = +30 V		0.8 1.5	1.2 3	
V_{icm}	Input common mode voltage range V_{CC} = +30 V (3) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common mode rejection ratio ($R_s \le 10$ kΩ) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	70 60	80		dB
I_{source}	Output current source (V_{id} = +1 V) V_{CC} = +15 V, V_o = +2 V	20	40	70	mA

Table 2. V_{CC}^{+} = +5 V, V_{CC}^{-}= Ground, V_o = 1.4 V, T_{amb} = +25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{sink}	Output sink current (V_{id} = -1 V) V_{CC} = +15 V, V_o = +2 V V_{CC} = +15 V, V_o = +0.2 V	 10 12	 20 50		 mA µA
V_{OH}	High level output voltage V_{CC} = +30 V T_{amb} = +25° C, R_L = 2 kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25° C, R_L = 10 kΩ $T_{min} \le T_{amb} \le T_{max}$	 26 26 27 27	 27 28 		V
	V_{CC} = +5 V, R_L = 2 kΩ T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	 3.5 3			
V_{OL}	Low level output voltage (R_L = 10 kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	 20 20	mV
SR	Slew rate V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.4		V/µs
GBP	Gain bandwidth product V_{CC} = 30 V, f = 100 kHz,V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF		1.3		MHz
THD	Total harmonic distortion f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC} = 30 V		0.015		%
e_n	Equivalent input noise voltage f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel separation (4) 1 kHz ≤ f ≤ 20 kHZ		120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^{+} < 30 V, 0 < V_{ic} < V_{CC}^{+} - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0. V. The upper end of the common-mode voltage range is V_{CC}^{+} - 1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 3. Input bias current vs. ambient temperature

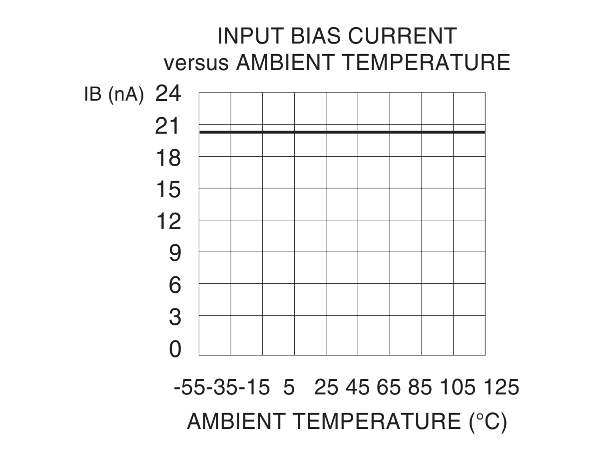


Figure 4. Current limiting

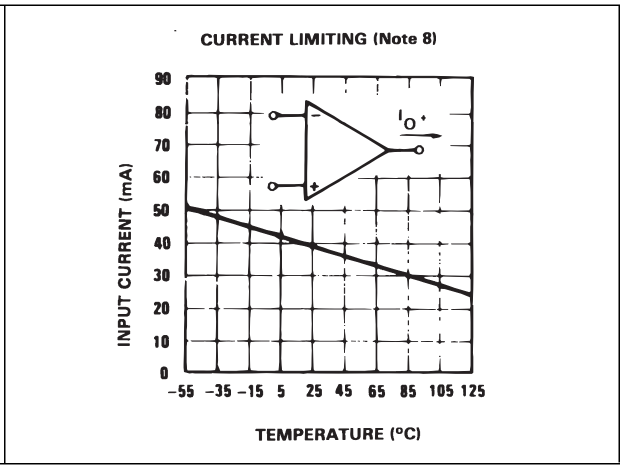


Figure 5. Input voltage range

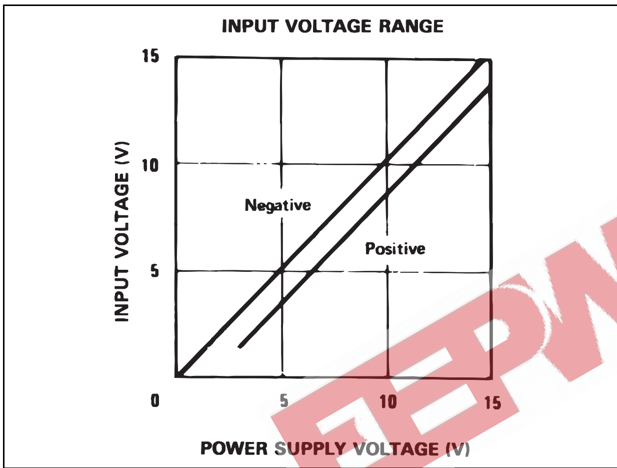


Figure 6. Supply current

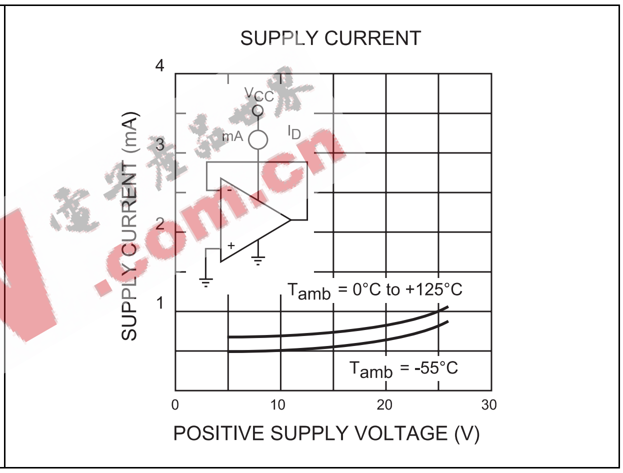


Figure 7. Gain bandwidth product

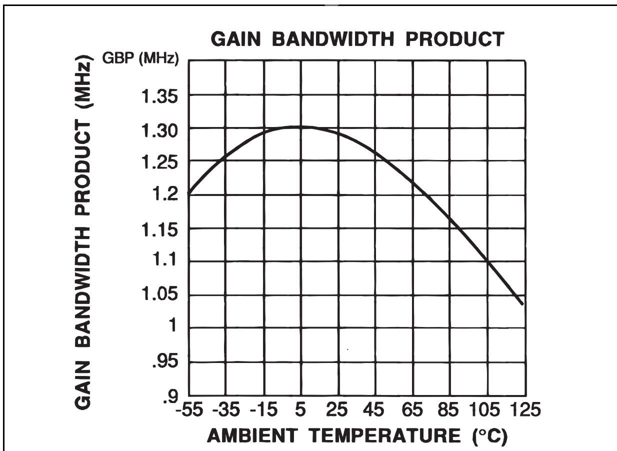
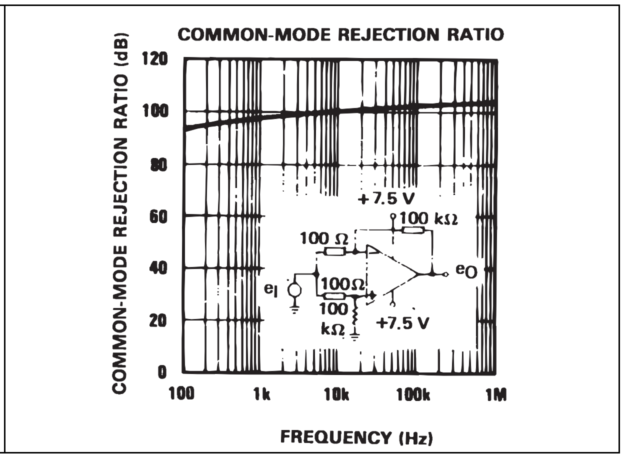
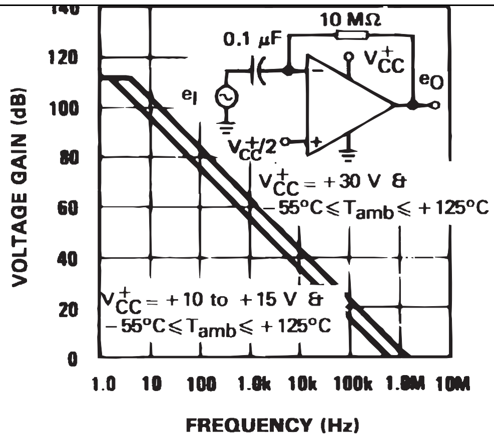
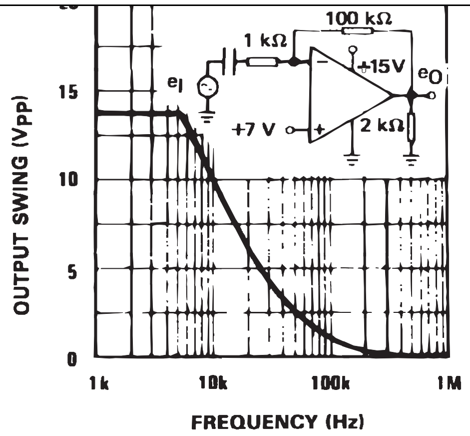


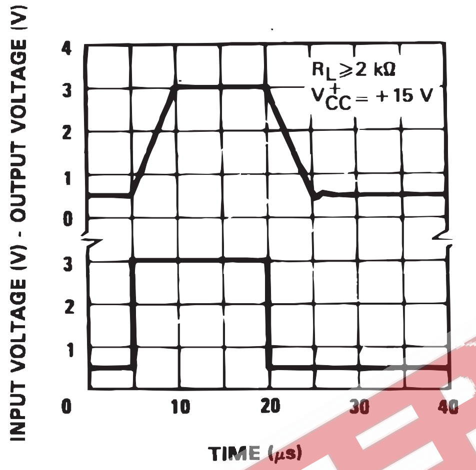
Figure 8. Common mode rejection ratio



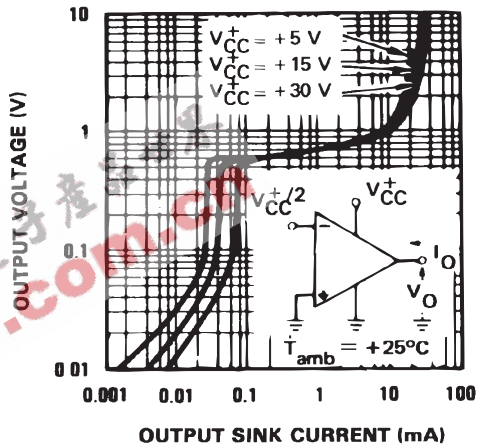




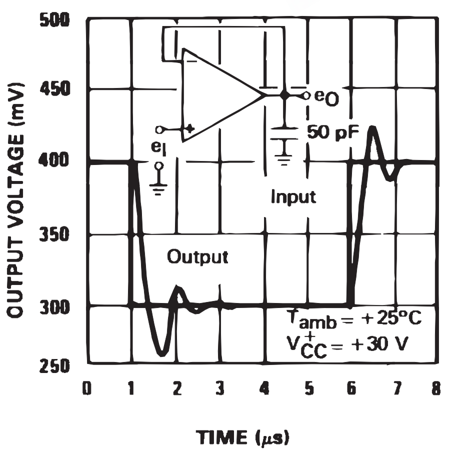
VOLTAGE FOLLOWER PULSE RESPONSE



OUTPUT CHARACTERISTICS (CURRENT SINKING)



VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



OUTPUT CHARACTERISTICS (CURRENT SOURCING)

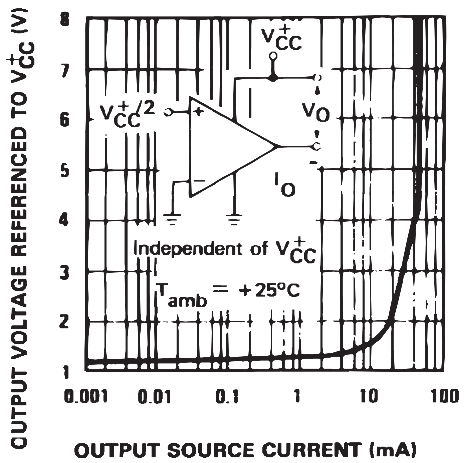


Figure 9. Input current

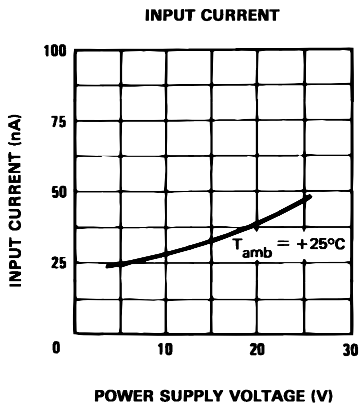


Figure 10. Large signal voltage gain

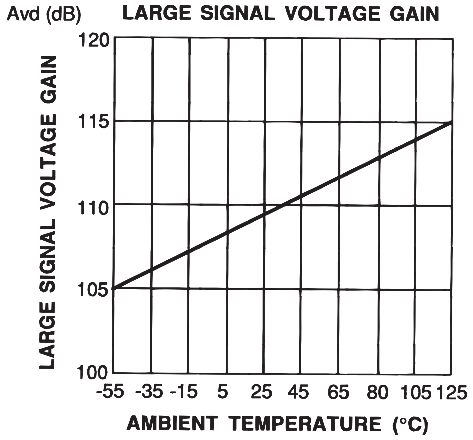


Figure 11. Power supply & common mode rejection ratio

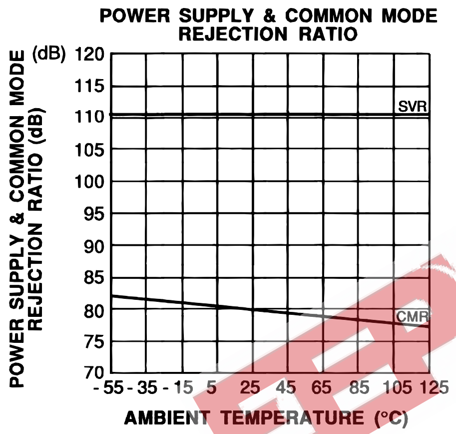
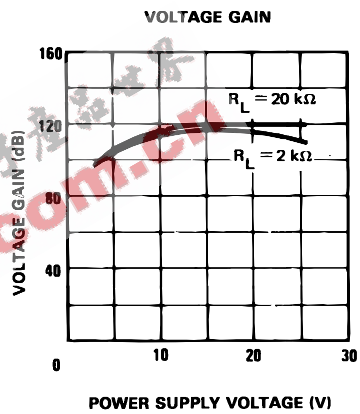


Figure 12. Voltage gain



4 Typical single-supply applications

Figure 13. AC coupled inverting amplifier

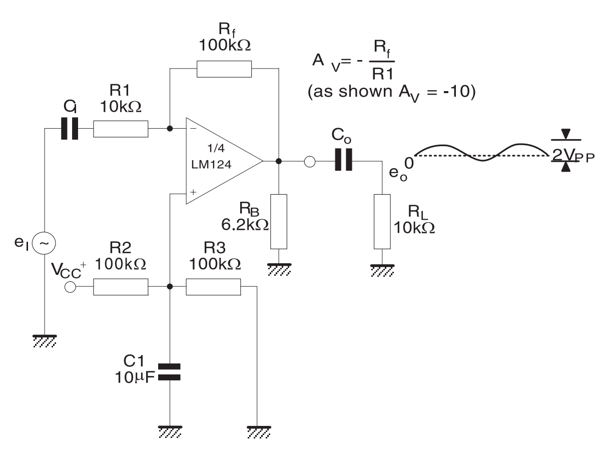


Figure 14. High input Z adjustable gain DC instrumentation amplifier

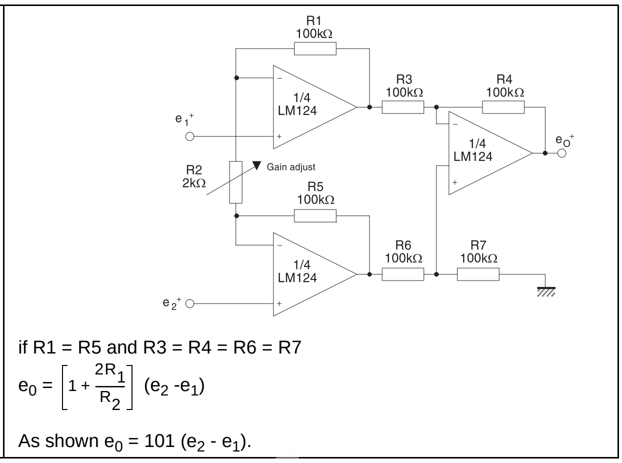


Figure 15. AC coupled non inverting amplifier

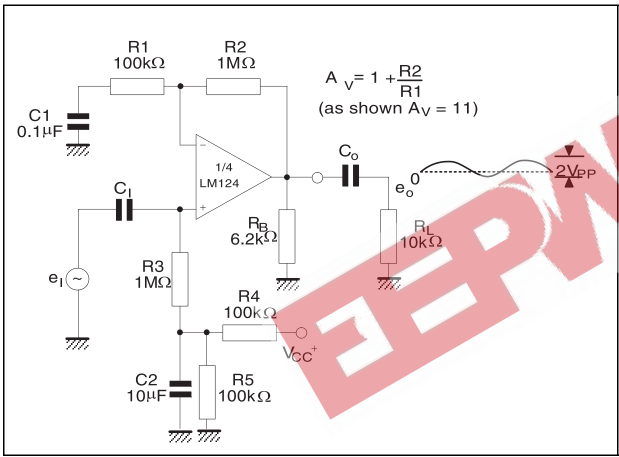


Figure 16. DC summing amplifier

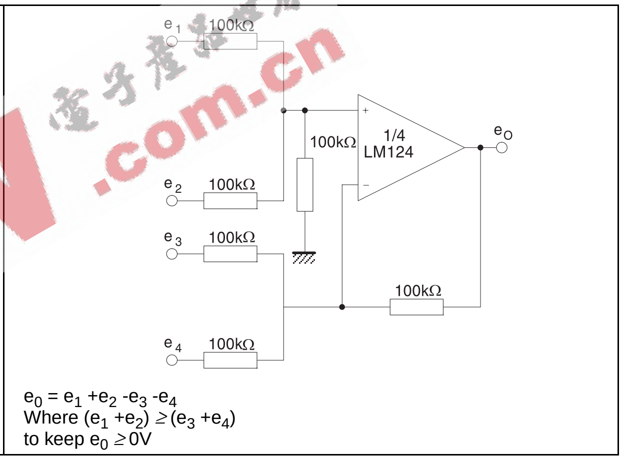


Figure 17. Non-inverting DC gain

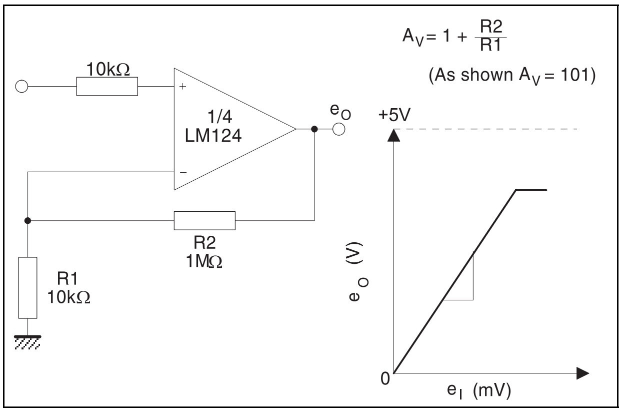


Figure 18. Low drift peak detector

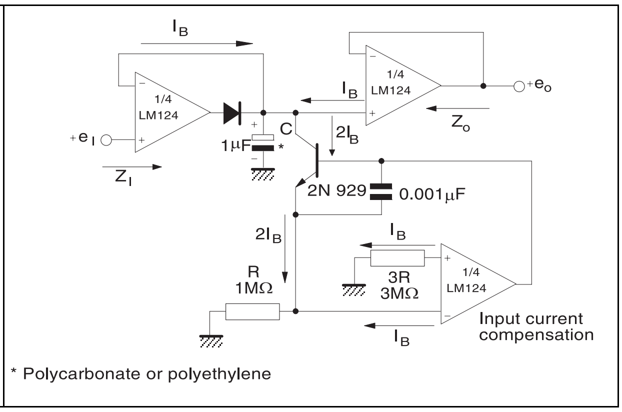


Figure 19. Active bandpass filter

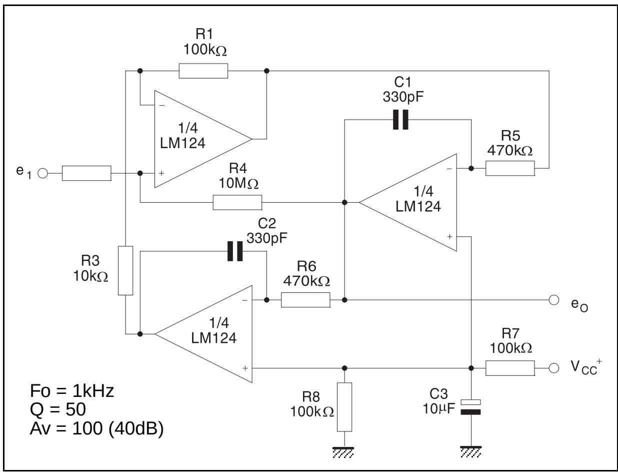


Figure 20. High input Z, DC differential amplifier

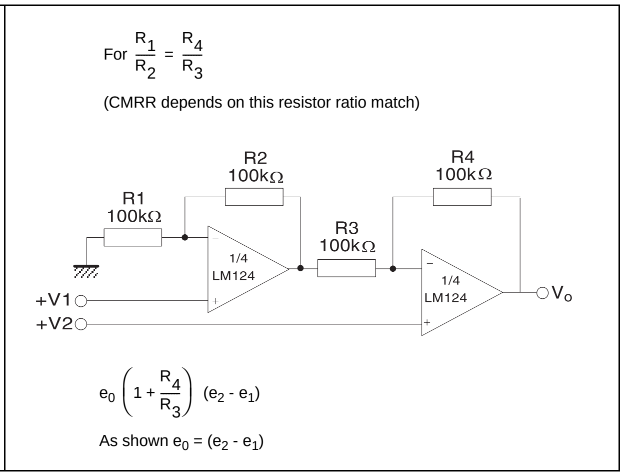
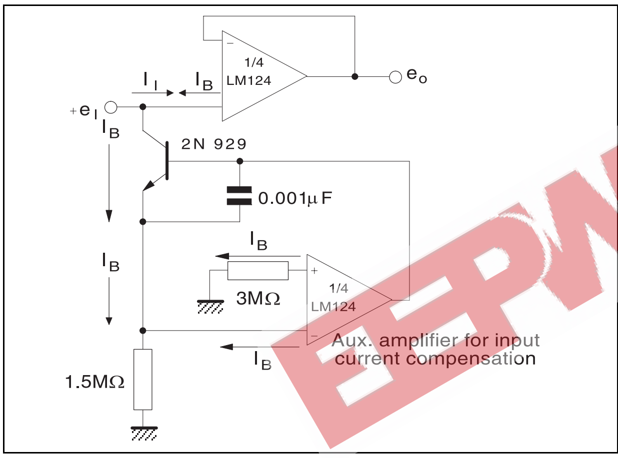


Figure 21. Using symmetrical amplifiers to reduce input current (general concept)



5 Macromodels

Note: Please consider the following before using this macromodel:

All models are a trade-off between accuracy and complexity (i.e. simulation time).

Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.

*A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.*

Data derived from macromodels that is used outside of the specified conditions (V_{cc}, temperature, etc.) or even worse, outside of the device operating conditions (V_{cc}, V_{icm}, etc.) is not reliable in any way.

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT LM124 1 3 2 4 5
********************************************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
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RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

The values provided in *Table 3* are derived from this macromodel.

Table 3. V_{cc}^{+} = +15V, V_{cc}^{-} = 0V, T_{amb} = 25°C (unless otherwise specified)

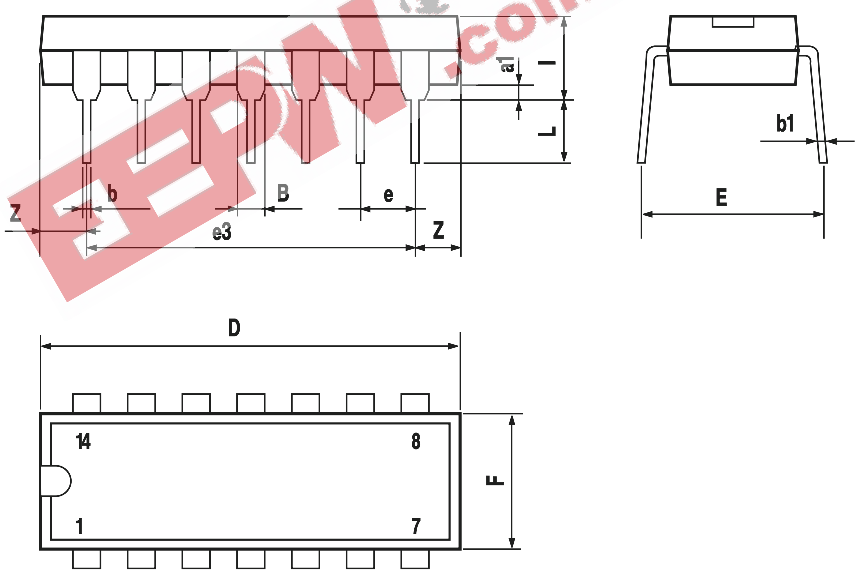
Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 2 kΩ	100	V/mV
I_{cc}	No load, per amplifier	350	µA
V_{icm}		-15 to +13.5	V
V_{OH}	R_L = 2 kΩ (V_{CC}^{+}=15V)	+13.5	V
V_{OL}	R_L = 10 kΩ	5	mV
I_{os}	V_o = +2 V, V_{CC} = +15 V	+40	mA
GBP	R_L = 2 kΩ, C_L = 100 pF	1.3	MHz
SR	R_L = 2 kΩ, C_L = 100 pF	0.4	V/µs

6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

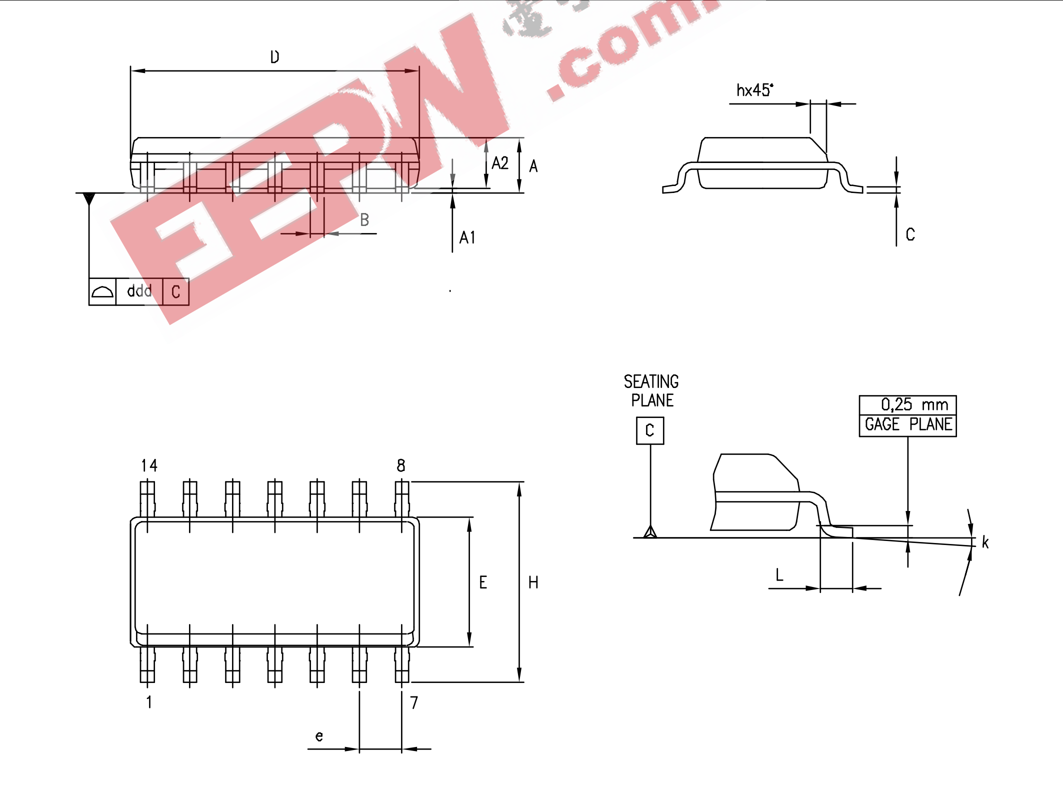
6.1 DIP14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



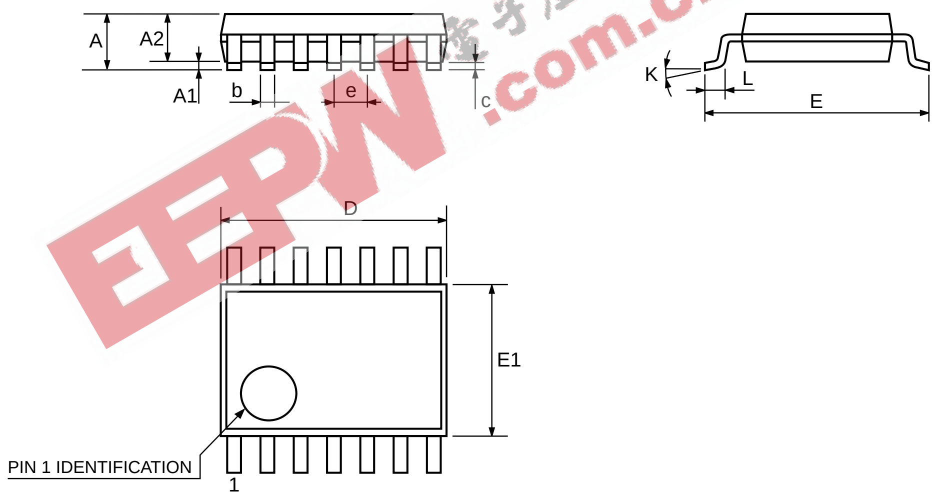
6.2 SO-14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
A1	0.1		0.2	0.003		0.007
A2			1.65			0.064
B	0.35		0.46	0.013		0.018
c	0.19		0.25	0.007		0.010
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
H	5.8		6.2	0.228		0.244
e		1.27			0.050	
E	3.8		4.0	0.149		0.157
L	0.5		0.127	0.019		0.050
k	8° (max.)					



6.3 TSSOP14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05	0.010	0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030



7 Revision history

Date	Revision	Changes
1-Oct.-2003	1	First release.
2-Jan-2005	2	Modifications on AMR *Table 1 on page 4* (explanation of V_{id} and V_i limits).
1-Jun-2005	3	ESD protection inserted in *Table 1 on page 4*.
2-Jan-2006	4	T_j and R_{thjc} parameters added in *Table 1. on page 4*.
4-Oct-2006	5	Editorial update. *Table 3* moved to *Section 5: Macromodels on page 12*.