LSI/CSI

LS7538-LS7539

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TOUCH CONTROL STEP DIMMER LIGHT SWITCH WITH AUTOMATIC GAIN CONTROL (AGC)

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FEATURES:

- Touch Sensitivity guaranteed to 600pF Touch Plate Capacitance.
- Touch Operation independent of line plug polarity.
- Pin selection of three available Brightness Step Sequences.
- Minimal external components.
- AGC Loop stabilizes immediately after Power-Up.
- Brightness state is Off after AC power applied.
- Brightness state is unchanged if AC power interrupted for < 0.5 sec.
- Advanced CMOS design for reliable operating characteristics and low power.
- 50/60 Hz Line Frequency.
- +6V to +9.5V Operation (V_{DD}-V_{SS}).
- LS7538, LS7539 (DIP); LS7538-S, LS7539-S (SOIC) - See Figure 1

APPLICATIONS:

- Screw-in and built-in adapter modules for converting table and floor lamps to touch control for step dimming.
- On-Off touch control of under-cabinet fluorescent lamps (LS7539 only).

PIN ASSIGNMENT
TOP VIEW

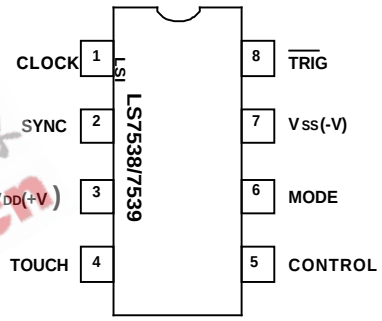


FIGURE 1

DESCRIPTION:

The LS7538 and LS7539 are CMOS integrated circuits which provide trigger pulses for triac phase control of incandescent lamps. The circuits are designed to operate with a wide variety of lamp sizes ranging from small table lamps to large floor lamps. The AGC Loop automatically adjusts Touch Sensitivity to be independent of lamp size.

There are 3 different Brightness Step Sequences for each version of the IC which can be selected by the Three-State MODE pin as shown in Table 1.

TABLE 1. BRIGHTNESS STEP MODES

MODE PIN	BRIGHTNESS STEP SEQUENCE
FLOAT	OFF-NIGHT LIGHT-MEDIUM-MAXIMUM-OFF
V_{DD}	OFF-NIGHT LIGHT- LOW MEDIUM-HIGH MEDIUM-MAXIMUM-OFF
Vss (LS7538)	OFF-MAXIMUM-MEDIUM-NIGHT LIGHT-OFF
(LS7539)	OFF-MAXIMUM-OFF

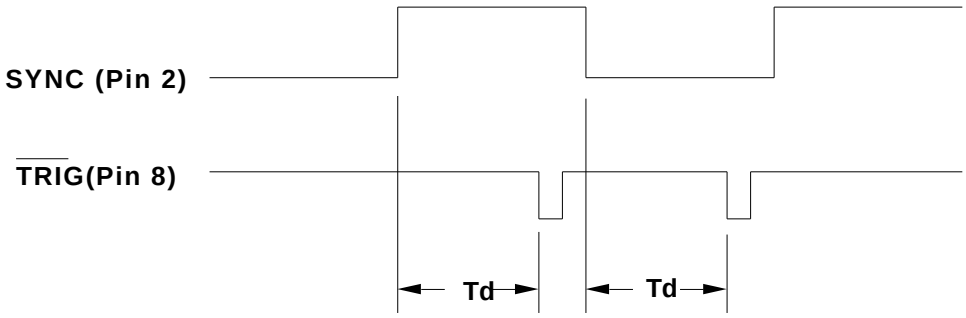
The lamp brightness is made to vary by changing the delay of the $\overline{TRIG}$ pulse to the triac from the zero-crossing of the SYNC input. The delays are shown in Table 2 for 50Hz and 60Hz operation along with Delivered Power as a percentage of Full Power. Figure 2 illustrates the delay.

TABLE 2. BRIGHTNESS POWER LEVELS

Brightness	**60Hz Delay** (1)	**50Hz Delay** (2)	**% PWR** (3)
Night Light	6.0 ms	7.2 ms	12
Low Medium	4.8 ms	5.7 ms	35
Medium	4.0 ms	4.8 ms	53
High Medium	3.2 ms	3.8 ms	72
Maximum	0.85 ms	1.0 ms	99

(1) With 300kΩ connected between Pin 1 and V_{DD}. **(2)** With 360kΩ connected between Pin 1 and V_{DD}.
(3) Percentage of Full Power delivered to a resistive load by the Triac Switch.

FIGURE 2. OUTPUT DELAY (Td)



INPUT/OUTPUT DESCRIPTION:

CLOCK Input (Pin 1)
An external resistor connected between this input and VDD, along with an internal capacitor and oscillator stage, generates a clock which is used for all timing functions. The recommended value of this resistor for 50Hz and 60Hz operation is specified in the ELECTRICAL CHARACTERISTICS. The resistor value determines the Brightness Levels produced. (See Table 2)

SYNC Input (Pin 2)
50 or 60Hz AC input for zero crossing detection.

VDD (Pin 3**)**
Supply voltage positive terminal.

TOUCH Input (Pin 4)
Input for sensing that a touch has been made on a lamp surface or other touch plate.

CONTROL I/O (Pin 5)
An external R-C network connected between this pin and VDD establishes the controlling feedback for the AGC Loop.

MODE Input (Pin 6)
A three-state input used to select the desired Brightness Step Sequence (See Table 1). The MODE Input may be changed during operation.

Vss (Pin 7**)**
Supply voltage negative terminal.

$\overline{\text{TRIG}}$ (Pin 8)
The $\overline{\text{TRIG}}$ output produces a negative going pulse every half-cycle of the SYNC input to trigger the triac. The delay, Td, of the pulse with respect to the SYNC signal determines the Brightness Level produced.
(See Table 2 & Figure 2)

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
DC supply voltage	VDD - VSS	+11	V
Any input voltage	VIN	VSS - 0.5 to VDD + 0.5	V
Operating temperature	TA	-20 to +85	°C
Storage temperature	TSTG	-65 to +150	°C

ELECTRICAL CHARACTERISTICS:
(All voltages referenced to Vss. T_A = +25°C unless otherwise specified.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	V_{DD}	+6	-	+9.5	V	-
Supply Current	I_{DD}	-	-	1.5	mA	Output off, V_{DD} = +8.0V
$\overline{\text{TRIG}}$ Sink Current Vo = V_{DD} - V	I_O	-50	-	-	mA	V_{DD} = +8.0V
$\overline{\text{TRIG}}$ Source Current Vo = V_{DD} - 0.2V	I_O	+0.1	-	-	mA	V_{DD} = +8.0V
$\overline{\text{TRIG}}$ Pulse Width	T_W	-	90	-	µs	R_C = 300kΩ, 60Hz
	-	-	110	-	µs	R_C = 360kΩ, 50Hz
$\overline{\text{TRIG}}$ Pulse Delay	Td	-	4.0	-	ms	Rc = 300kΩ, 60Hz
(Medium Brightness)		-	4.8	-	ms	Rc = 360kΩ, 50Hz
CLOCK Resistor	R_C	-	300	-	kΩ	60Hz
	-	-	360	-	kΩ	50Hz
CONTROL Resistor	-	-	10	-	MΩ	-
Capacitor	-	-	1	-	µF	-
Touch Plate Capacitance	C_L	-	-	600	pF	-

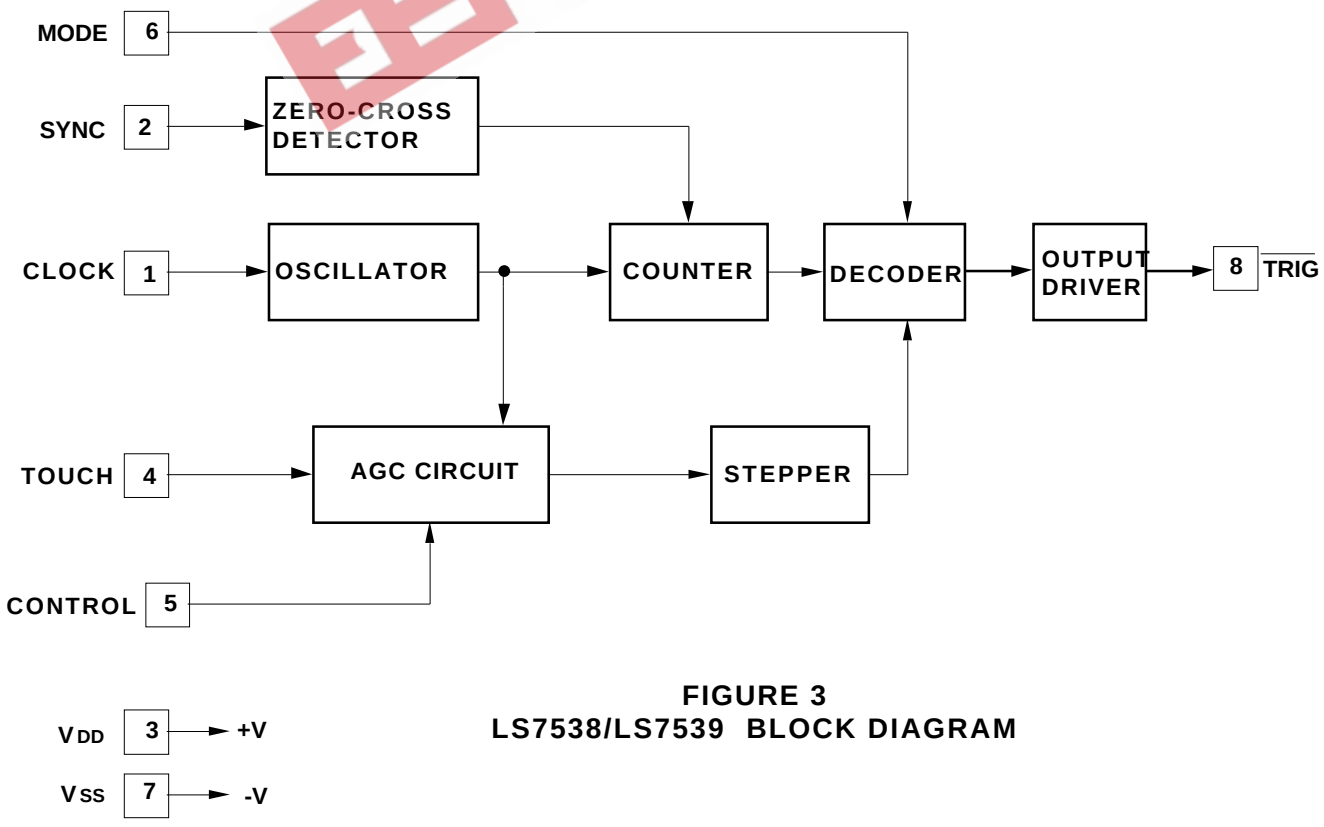
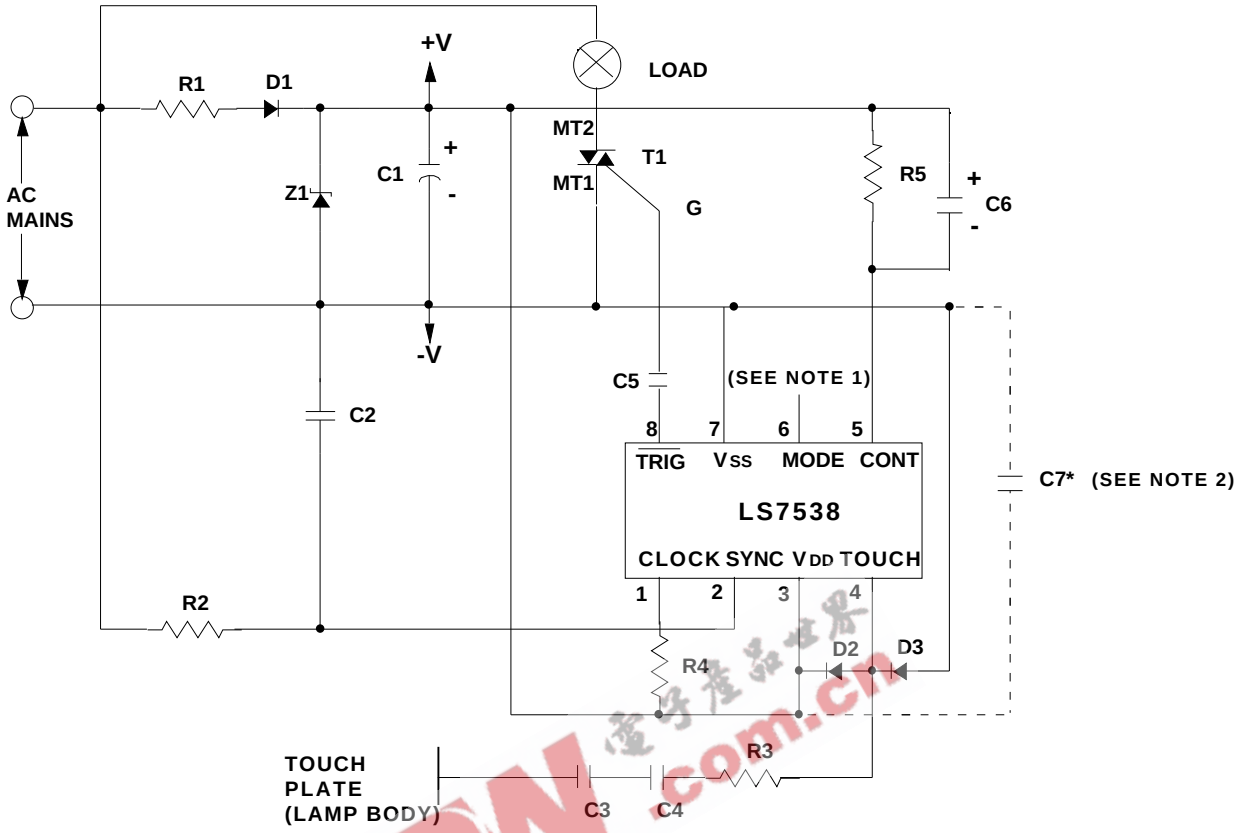


FIGURE 3
LS7538/LS7539 BLOCK DIAGRAM

FIGURE 4. TOUCH LAMP APPLICATION SCHEMATIC



115VAC APPLICATION

	R1	=	20kΩ, 1W	C4	=	1000pF, 1kV
	R2	=	470kΩ, 1/4W	C5	=	.03µF, 16V
	R3	=	1kΩ, 1/4W	C6	=	1µF, 16V
(1)	R4	=	300kΩ, 1/4W, 1%	Z1	=	8.2V, 1/4W Zener
	R5	=	10MΩ, 1/4W	D1	=	1N4004
	C1	=	47µF, 16V	D2	=	1N4148
	C2	=	1000pF, 16V	D3	=	1N4148
	C3	=	1000pF, 1kV	T1	=	Q2004L4 (Typical Triac)
					or	Q2004F41 (Typical Triac)

220VAC APPLICATION

	R1	=	39kΩ, 2W
	R2	=	910kΩ, 1/4W
(1)	R4	=	360kΩ, 1/4W, 1%
	D1	=	1N4005
	T1	=	Q4004L4 (Typical Triac)
		or	Q4004F41 (Typical Triac)

All other values remain the same.

(1) Resistor should be placed adjacent to Pin 1.

NOTE 1: Connect MODE (Pin 6) for desired Brightness Step Sequence (See Table 1).

NOTE 2: A good PCB layout using through-hole components will provide protection for ESD introduced at the Touch Plate in the range of 25kV. Using surface mount components and/or a poor PCB layout can reduce the ESD protection. The OEM can increase the ESD protection provided by the product with any combination of the following steps:

Step 1: The most effective and least costly way to increase ESD protection is to create a spark gap around the Touch Plate input on the PCB. This will increase ESD protection on a good PCB layout to abut 35kV. The gap should be made with a split metal ring with each side of the metal ring connected back to opposite sides of the AC line. This ensures that a path for the spark back to house ground through AC Neutral exists independent of line plug polarity. The split ring and the center conduction plate should be constructed so that the spacing between them conforms to UL requirements. The spark gap will absorb most of the ESD leaving a remnant of about 10kV for the rest of the circuit to absorb.

Step 2: Increase R3 from 1kΩ to 5.1kΩ and add C7, a 0.1µF capacitor, between V_{DD} and Vss. (A minimal loss in touch sensitivity may be experienced.)

Step 3: Replace diodes D2 and D3 (1N4148) with Schottky diodes (1N5819 or similar)