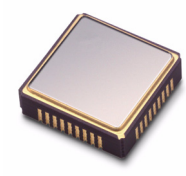
M2020/21

VCSO Based Clock PLL

General Description



The M2020/21 is a VCSO (Voltage Controlled SAW Oscillator) based clock jitter attenuator PLL designed for clock jitter attenuation and frequency translation. The device is ideal for generating the transmit reference clock for optical network systems supporting 2.5-10 GB data rates. It can serve to jitter attenuate a stratum reference clock or a recovered clock in loop timing mode. The M2020/21 module includes a proprietary SAW (surface acoustic wave) delay line as part of the VCSO. This results in a high frequency, high-Q, low phase noise oscillator that assures low intrinsic output jitter.

Features

- **Integrated SAW (surface acoustic wave) delay line; low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**
- **Output frequencies of 15 to 700 MHz ***
- **LVPECL clock output (CML and LVDS options available)**
- **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**
- **Loss of Lock (LOL) output pin**
- **Narrow Bandwidth control input (NBW pin)**
- **Hitless Switching (HS) options with or without Phase Build-out (PBO) available for SONET (GR-253) / SDH (G.813) MTIE and TDEV compliance during reference clock reselection**
- **Industrial temperature grade available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

Pin Assignment (9 x 9 mm SMT)

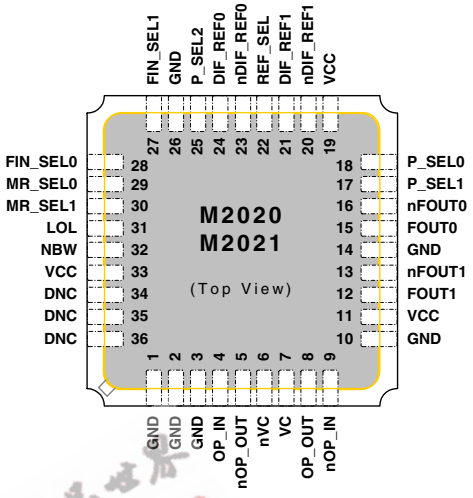


Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M2020-11-622.0800 or M2021-11-622.0800

Input Reference Clock (MHz)	PLL Ratio (Pin Selectable)	Output Clock (MHz)
(M2020) (M2021)	(M2020) (M2021)	
19.44 or 38.88	32 or 16	622.08
77.76	8	
155.52	4	
622.08	1	

Table 1: Example I/O Clock Frequency Combinations

* Specify VCSO center frequency at time of order.

Simplified Block Diagram

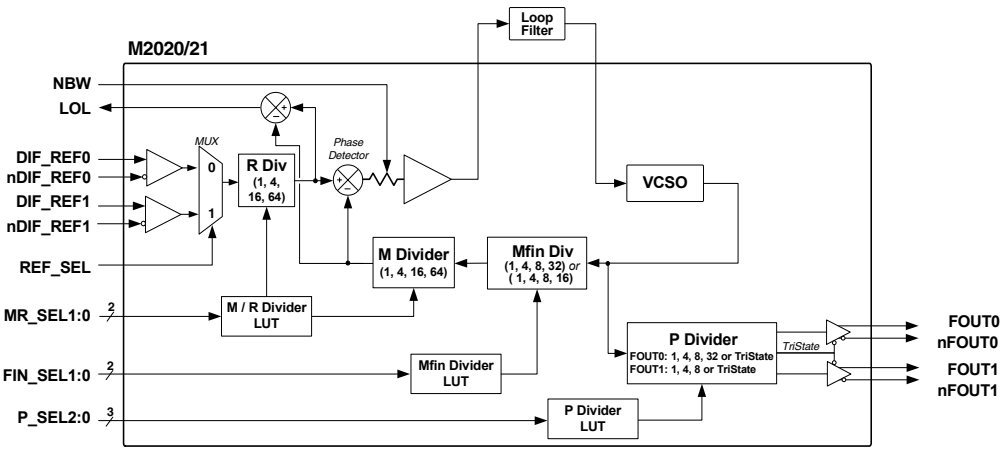


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 6.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output pair 1. Differential LVPECL.
15 16	FOUT0 nFOUT0	Output	No internal terminator	Clock output pair 0. Differential LVPECL.
17 18 25	P_SEL1 P_SEL0 P_SEL2	Input	Internal pull-down resistor[1]	Post-PLL , P divider selection. LVCMOS/LVTTL. See Table 5, P Divider Look-Up Table (LUT), on pg. 3.
20	nDIF_REF1	Input	Biased to Vcc/2 [2]	Reference clock input pair 1. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
21	DIF_REF1		Internal pull-down resistor[1]	
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23	nDIF_REF0	Input	Biased to Vcc/2 [2]	Reference clock input pair 0. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
24	DIF_REF0		Internal pull-down resistor [1]	
27 28	FIN_SEL1 FIN_SEL0	Input	Internal pull-down resistor[1]	Input clock frequency selection. LVCMOS/LVTTL. See Table 3, Mfin Divider Look-Up Table (LUT) on pg. 3.
29 30	MR_SEL0 MR_SEL1	Input	Internal pull-down resistor[1]	M and R divider value selection. LVCMOS/ LVTTL. See Table 4, M and R Divider Look-Up Table (LUT) on pg. 3.
31	LOL	Output		Loss of Lock indicator output. Asserted when internal PLL is not tracking the input reference for frequency and phase. [3] Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} = 2100kΩ Logic 0 - Wide bandwidth, R_{IN} = 100kΩ
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-UP resistors, see **DC Characteristics** on pg. 8.
Note 2: Biased toVcc/2, with 50kΩ to Vcc and 50kΩ to ground. See **Differential Inputs Biased to VCC/2** on pg. 8.
Note 3: See **LVCMOS Output** in DC Characteristics on pg. 8.

DETAILED BLOCK DIAGRAM

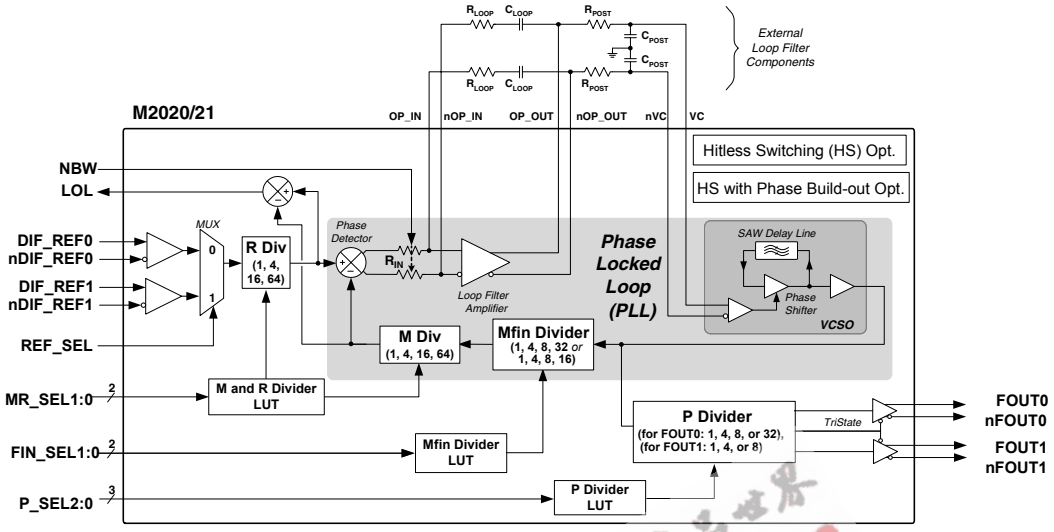


Figure 3: Detailed Block Diagram

DIVIDER SELECTION TABLES

Mfin Divider Look-Up Table (LUT)

The FIN_SEL1:0 pins select the Mfin divider value, which establishes the PLL clock multiplication ratio. Since the VCSO frequency is fixed, this allows input reference selection.

FIN_SEL1:0	Mfin Value	Input Ref. Freq. (MHz) [1] M2020-yz-622.0800 or M2021-yz-622.0800
0 0	(M2020) (M2021) 32 or 16	19.44 or 38.88
0 1	8	77.76
1 0	4	155.52
1 1	1	622.08

Table 3: Mfin Divider Look-Up Table (LUT)

Note 1: Example with **M2020-yz-622.0800 or M2021-yz-622.0800**

M and R Divider Look-Up Table (LUT)

The MR_SEL1:0 pins select the M and R divider values, which establish phase detector frequency. A lower phase detector frequency improves jitter tolerance and lowers loop bandwidth.

MR_SEL1:0	M	R	Description
0 0 [1]	1	1	Four sets of divider values to enable adjustment of bandwidth and jitter tolerance
0 1	4	4	
1 0	16	16	
1 1	64	64	

Table 4: M and R Divider Look-Up Table (LUT)

Note 1: Do not use with FIN_SEL1:0=11; Maximum Phase Detector Frequency=175MHz

P Divider Look-Up Table (LUT)

The P_SEL2:0 pins select the P divider values, which set the output clock frequencies. A P divider of value of 1 will provide a 622.08MHz output when using a 622.08MHz VCSO, for example. P divider values of 4, 8, or 32 are also available, plus a TriState mode. The outputs can be placed into the valid state combinations as listed in Table 5. (The outputs cannot each be placed into any of the five available states independently.)

P_SEL2:0	P Value for FOUT0	P Value for FOUT1	M2020-yz-622.0800 or M2021-yz-622.0800 Output Frequency (MHz) FOUT0	FOUT1
0 0 0	32	1	19.44	622.08
0 0 1	32	4	19.44	155.52
0 1 0	1	1	622.08	622.08
0 1 1	4	1	155.52	622.08
1 0 0	8	8	77.76	77.76
1 0 1	4	4	155.52	155.52
1 1 0	8	4	77.76	155.52
1 1 1	TriState	TriState	N/A	N/A

Table 5: P Divider Look-Up Table (LUT)

General Guidelines for M and R Divider Selection

- A lower phase detector frequency should be used for loop timing applications to assure PLL tracking, especially during GR-253 jitter tolerance testing. The recommended maximum phase detector frequency for loop timing mode is 19.44MHz.
- When LOL is to be used for system health monitoring, the phase detector frequency should be 5MHz or greater. Low phase detector frequencies make LOL overly sensitive, and higher phase detector frequencies make LOL less sensitive. The LOL pin should not be used during loop timing mode.

FUNCTIONAL DESCRIPTION

The M2020/21 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW delay line provides low jitter signal performance and establishes the output frequency of the VCSO (Voltage Controlled SAW Oscillator). In a given M2020/21 device, the VCSO center frequency is fixed. A common center frequency is 622.08MHz, for SONET for SDH optical network applications. The VCSO center frequency is specified at time of order (see “Ordering Information” on pg. 10). The VCSO has a guaranteed tuning range of ±120 ppm (commercial temperature grade).

Pin selectable dividers are used within the PLL and for the output clock. This enables tailoring of device functionality and performance. The Mfin divider controls the overall PLL multiplication ratio and thus determines the input reference clock (see Table 3, on pg. 3). The M and R dividers control the phase detector frequency (see Table 4). The P divider scales the VCSO output enabling lower output frequency selections (Table 5).

The M2020/21 includes a Loss of Lock (LOL) indicator, which provides status information to system management software. A Narrow Bandwidth (NBW) control pin is provided as an additional mechanism for adjusting PLL loop bandwidth without affecting the phase detector frequency.

Options are available for Hitless Switching (HS) with or without Phase Build-out (PBO). They provide SONET/SDH MTIE and TDEV compliance during a reference clock reselection.

Allowance for a single-ended input has been facilitated by a unique input resistor bias scheme, which is described next and shown in Figure 4.

Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTL on the non-inverting input).

A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.

Configuration of a single-ended input has been facilitated by biasing nDIF_REF0 and nDEF_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. The input clock structure, and how it is used with either LVCMOS/LVTTL inputs or a DC- coupled LVPECL clock, is shown in Figure 4.

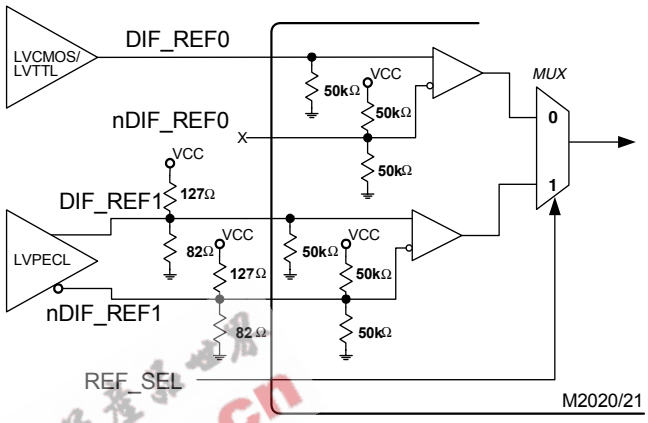


Figure 4: Input Reference Clocks

Differential Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) is ideally suited for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the V_{TT} bias voltage.

Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTL) are connected to the non-inverting reference input pin (DIF_REF0 or DIF_REF1). The inverting reference input pin (nDIF_REF0 or nDIF_REF1) must be left unconnected.

In single-ended operation, when the unused inverting input pin (nDIF_REF0 or nDEF_REF1) is left floating (not connected), the input will self-bias at VCC/2.

PLL Operation

The M2020/21 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The PLL will work correctly, meaning it will phase-lock the VCSO output to the input reference clock, when the internal phase detector inputs are able to run at the same frequency. This means the PLL dividers must be set appropriately and a suitable reference frequency must be chosen for the intended output frequency. When the PLL is not set up appropriately, the VCSO is forced to its upper or lower operating limit which is typically about 250 ppm above or below the VCSO center frequency (no more than 500 ppm above or below).

In normal phase-locked condition, the instantaneous phase error is measured by the phase detector and is converted to charge pump current pulses. These current pulses are then integrated by the external loop filter to create a VCSO control voltage. The loop filter acts as a low pass filter to remove unwanted reference clock jitter above a determined frequency or PLL bandwidth. For reference phase jitter frequencies within the loop bandwidth, phase jitter amplitude is passed on to the output clock according to the PLL loop frequency response curve.

The relationship between the nominal VCSO center frequency (Fvcso), the M divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times Mfin \times \frac{M}{R}$$

Example Frequency and Divider Combinations Using M2021-yz-622.0800

Fvcso =	Fin x	Mfin x M/R
622.08	38.88	16 x (1/1, 4/4, etc.)
	77.76	8 x (1/1, 4/4, etc.)
	155.52	4 x (1/1, 4/4, etc.)
	622.08	1 x (1/1, 4/4, etc.)

Table 6: Example I/O Clock Frequency Combinations

The M, R, and Mfin dividers can be set by pin configuration using the input pins MR_SEL1, MR_SEL0, FIN_SEL1, and FIN_SEL0.

Post-PLL Divider

The M2020/21 also features a post-PLL (P) divider.

Through use of the P divider, the device's output frequency (Fout) can be that of the VCSO (such as 622.08MHz) or the VCSO frequency divided by 4, 8 or 32 (common optical reference clocks in SONET and SDH systems).

The P_SEL2:0 pins select the value for the P divider. (See Table 5 on pg. 3.)

Accounting for the P divider, the complete relationship between the input clock reference frequency (Fin) and output clock frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{P} = Fin \times \frac{M \times Mfin}{R \times P}$$

Due to the narrow tuning range of the VCSO (±120ppm guaranteed), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

TriState

The TriState feature puts the LVPECL output driver into a high impedance state, effectively disconnecting the driver from the FOUT and nFOUT pins of the device. A logic 0 is then present on the clock net. The impedance of the clock net is then set to 50Ω by the external circuit resistors. (This is in distinction to a CMOS output in TriState, in which case the net goes to a high impedance and the logic value floats.) The 50Ω impedance level of the LVPECL TriState allows manufacturing In-circuit Test to drive the clock net with an external 50Ω generator to validate the integrity of clock net and the clock load.

Any unused output (single-ended or differential) should be left unconnected (floating) in system application. This minimizes output switching current and therefore minimizes noise modulation of the VCSO.

Narrow Bandwidth (NBW) Control Pin

A Narrow Loop Bandwidth control pin (NBW pin) is included to enable adjustment of the PLL loop bandwidth. In wide bandwidth mode (NBW=0), the internal resistor Rin is 100kΩ. With the NBW pin asserted (NBW=1), the internal resistor Rin is changed to 2100kΩ. This lowers the loop bandwidth by a factor of about 21 (2100 / 100) and lowers the damping factor by about 4.6 (the square root of 21), assuming the same external loop filter component values.

Loss of Lock Indicator (LOL) Output Pin

Under normal device operation, when the PLL is locked, the LOL Phase Detector drives LOL to logic 0. Under circumstances when the VCSO cannot fully phase lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the LOL Phase Detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current LVCMOS output.

Guidelines for Using LOL

In a given application, the magnitude of peak-to-peak jitter at the phase detector will usually increase as the R divider is increased. If the LOL pin will be used to detect an unusual clock condition, or a clock fault, the MR_SEL1:0 pins should be set to provide a phase detector frequency of 5MHz or greater (the phase detector frequency is equal to Fin divided by the R divider). Otherwise, false LOL indications may result. A phase detector frequency of 10MHz or greater is desirable when reference jitter is over 500ps, or when the device is used within a noisy system environment. LOL should not be used when the device is used in a loop timing application.

Optional Hitless Switching and Phase Build-out

The M2020/21 is available with a Hitless Switching feature that is enabled during device manufacturing. In addition, a Phase Build-out feature is also offered. These features are offered as device options and are specified by device order code. Refer to “Ordering Information” on pg. 10.

The Hitless Switching feature (with or without Phase Build-out) is designed for applications where switching occurs between two stable system reference clocks. It should not be used in loop timing applications, or when reference clock jitter is greater than 1 ns pk-pk. The Hitless Switching sequence is triggered by the LOL circuit, which is activated by a 4 ns phase transient. This magnitude of phase transient can generated by the CDR (Clock & Data Recovery unit) in loop timing mode, especially during a system jitter tolerance test. It can also be generated by some types of Stratum clock DPLLs (digital PLL), especially those that do not include a post de-jitter APLL (analog PLL).

When the M2020/21 is operating in wide bandwidth mode (NBW=0), the optional Hitless Switching function puts the device into narrow bandwidth mode during the Hitless Switching sequence. This allows the PLL to lock the new input clock phase gradually. With proper configuration of the external loop filter, the output clock phase change complies with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The optional proprietary Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock during reference switching. The PBO function selects a new VCSO clock edge for the PLL Phase Detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

The Hitless Switching and Phase Build-out functions are triggered by the LOL circuit. For proper operation, a low phase detector frequency must be avoided. See “Guidelines for Using LOL” on pg. 5 for information regarding the phase detector frequency.

HS/PBO Sequence Trigger Mechanism

The HS function (or the combined HS/PBO function) is armed after the device locks to the input clock reference. Once armed, HS is triggered by the occurance of a Loss of Lock condition. This would typically occur as a consequence of a clock reference failure, a clock failure upstream to the M2020/21, or a M2020/21 clock reference mux reselection.

HS/PBO Operation

Once triggered, the following HS/PBO sequence occurs:

1. The HS function disables the PLL Phase Detector and puts the device into NBW (narrow bandwidth) mode. The internal resistor Rin is changed to 2100kΩ. See External Loop Filter on pg. 6.
2. If included, the PBO function adds to (builds out) the phase in the clock feedback path (in VCSO clock cycle increments) to align the feedback clock with the (new) reference clock input phase.
3. The PLL Phase Detector is enabled, allowing the PLL to re-lock.
4. Once the PLL Phase Detector feedback and input clocks are locked to within 2 ns for eight consecutive cycles, a timer (WBW timer) for resuming wide bandwidth (in 175 ns) is started.
5. When the WBW timer times out, the device reverts to wide loop bandwidth mode (*i.e.,* Rin is returned to 100kΩ) and the HS/PBO function is re-armed.

The LOL pin will indicate lock status on a cycle-to-cycle basis and may be intermittent until PLL phase lock has fully stabilized.

External Loop Filter

To provide stable PLL operation, the M2020/21 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5). The loop filter is implemented as a differential circuit to minimize system noise interference. .

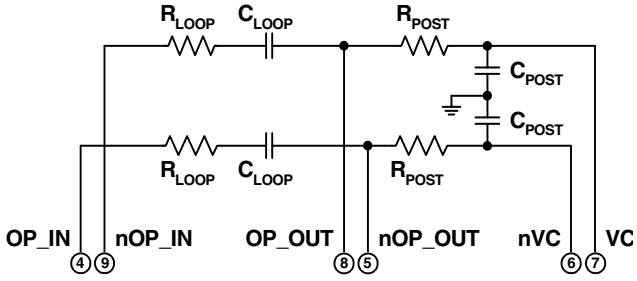


Figure 5: External Loop Filter

PLL bandwidth is affected by loop filter component values, “M” and “Mfin” values, and the “PLL Loop Constants” listed in AC Characteristics on pg. 9.

The MR_SEL1 and MR_SEL0 settings can be used to actively change PLL loop bandwidth in a given application. See “M and R Divider Look-Up Table (LUT)” on pg. 3.

See Table 7, Example Values for Loop Filter External Components, on pg. 7.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the M2020/21 product web page at www.icst.com/products/summary/m2020-2021.htm for additional product information.

Example Values for Loop Filter External Components [1] for M2020-yz-622.0800 and M2021-yz-622.0800

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Purpose	Device Configuration				Example External Component Values				Nominal Performance With These Values		
	F_{Ref} (MHz)	F_{VCSO} (MHz)	FIN_SEL 1:0	MRSEL 1:0	R loop	C loop	R post	C post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
Frequency Translation, General Usage	155.52	622.08	1 0	0 1	11.5kΩ	2.2µF	32.4kΩ	470p	1kHz	6.0	0.05
	77.76	622.08	0 1	0 1	23.2kΩ	1.0µF	32.4kΩ	470p	1kHz	6.5	0.06
	38.88 [2]	622.08	0 0 [2]	0 0	11.5kΩ	2.2µF	32.4kΩ	470p	1kHz	6.7	0.05
	19.44 [3]	622.08	0 0 [3]	0 0	23.2kΩ	1.0µF	32.4kΩ	470p	1kHz	6.5	0.06
Jitter Attenuation, Narrow Bandwidth	622.08	622.08	1 1	1 0	5.6kΩ	10µF	68kΩ	470p	500Hz	6.3	0.05
	77.76	622.08	0 1	0 1	8.2kΩ	10µF	100kΩ	470p	360Hz	6.5	0.05
	38.88 [2]	622.08	0 0 [2]	0 1	12.0kΩ	10µF	100kΩ	470p	260Hz	6.7	0.05
	19.44 [3]	622.08	0 0 [3]	0 0	8.2kΩ	10µF	100kΩ	470p	360Hz	6.5	0.05

Table 7: Example Values for Loop Filter External Components

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.
Note 2: M2021 only.
Note 3: M2020 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 8: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 9: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
All Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{cc} - .85	V	
	C_{IN}	Input Capacitance				4	pF	
Differential Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	DIF_REF0, DIF_REF1			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
Differential Inputs Biased to VCC/2	I_{IH}	Input High Current (Biased)	nDIF_REF0, nDIF_REF1			150	µA	V_{IN} = 0 to 3.456V
	I_{IL}	Input Low Current (Biased)		-150			µA	
	R_{bias}	Biased to Vcc/2			See Figure 4		kΩ	
All LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_SEL, FIN_SEL1, FIN_SEL0, MR_SEL1, MR_SEL0, P_SEL2, P_SEL1, P_SEL0, NBW	2		V_{cc} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
LVCMOS / LVTTL Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	REF_SEL, FIN_SEL1, FIN_SEL0, MR_SEL1, MR_SEL0, P_SEL2, P_SEL1, P_SEL0			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
LVCMOS / LVTTL Inputs with Pull-UP	I_{IH}	Input High Current (Pull-UP)	NBW			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current (Pull-UP)		-150			µA	
	R_{pullup}	Internal Pull-UP Resistance			50		kΩ	
Differential Outputs	V_{OH}	Output High Voltage	FOUT0, nFOUT0, FOUT1, nFOUT1	V_{cc} - 1.4		V_{cc} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{cc} - 2.0		V_{cc} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	
LVCMOS Output	V_{OH}	Output High Voltage	LOL	2.4		V_{CC}	V	I_{OH}= 1mA
	V_{OL}	Output Low Voltage		GND		0.4	V	I_{OL}= 1mA

Note 1: Single-ended measurement. See Figure 6, Output Rise and Fall Time, on pg. 9.

Table 10: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), $F_{VCSO} = F_{OUT}$ = 622-675MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	10		700	MHz	
	F_{OUT}	Output Frequency	FOUT0, nFOUT0, FOUT1, nFOUT1	15		700	MHz	
	APR	VCSO Absolute Pull-Range	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor	Wide Bandwidth		100		kΩ	
			Narrow Bandwidth		2100		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-73		dBc/Hz	Fin=19.44 or 38.88 MHz Mfin=32 or 16, M=1, R=1
			10kHz Offset		-103		dBc/Hz	
			100kHz Offset		-126		dBc/Hz	
	J(t)	Jitter (rms) @622.08MHz	12kHz to 20MHz		0.25	0.5	ps	
			50kHz to 80MHz		0.25	0.5	ps	
	odc	Output Duty Cycle [2]	P = 4, 8, or 32	45	50	55	%	
			P = 1	40	50	60	%	
	t_R	Output Rise Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		200	450	500	ps	20% to 80%
	t_F	Output Fall Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		200	450	500	ps	20% to 80%

Table 11: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 7, Example Values for Loop Filter External Components, on pg. 7.
Note 2: See Parameter Measurement Information on pg. 9.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

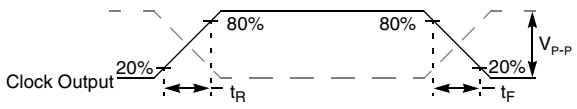


Figure 6: Output Rise and Fall Time

Output Duty Cycle

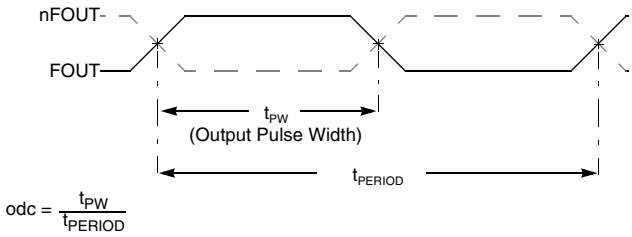
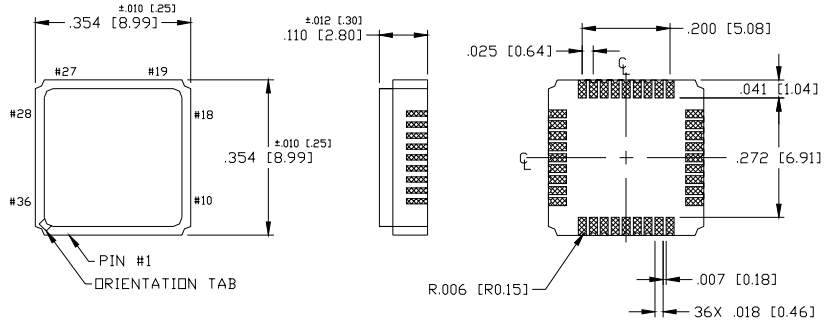


Figure 7: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the M2020/21 product web page at www.icst.com/products/summary/m2020-2021.htm for recommended PCB footprint, solder mask, furnace profile, and related information.

NOTES:
1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 8: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

Part Number: **M202x-yz-xxx.xxxx**

- Frequency Input Divider Option
  - 0 = Mfin Divider selections of: 32, 8, 4, or 1
  - 1 = Mfin Divider selections of: 16, 8, 4, or 1
- Output type
  - 1 = LVPECL
  - (For CML or LVDS clock output, consult factory)
- Hitless Switching / Phase Build-out Options
  - 1 = none
  - 2 = Hitless Switching
  - 3 = Hitless Switching with Phase Build-out
- Temperature
  - "-" = 0 to +70 °C (commercial)
  - I = - 40 to +85 °C (industrial)
- VCSO Frequency (MHz)
  - *See Table 12, right. Consult ICS for other frequencies.*

Figure 9: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*

622.0800	669.3120
625.0000	669.3266
627.3296	670.8386
644.5313	672.1600
666.5143	690.5692
669.1281	669.3120

Table 12: Standard VCSO Output Frequencies

Note *: Fout can equal Fvcso divided by: 1, 4, 8, or 32

Consult ICS for the availability of other VCSO frequencies.

Example Part Numbers

VCSO Frequency (MHz)	Temperature	Order Part Number
622.08	commercial	**M2020-11-622.0800** or **M2021-11-622.0800**
	industrial	**M2020-11I622.0800** or **M2021-11I622.0800**
625.00	commercial	**M2020-11-625.0000** or **M2021-11-625.0000**
	industrial	**M2020-11I625.0000** or **M2021-11I625.0000**

Table 13: Example Part Numbers